# Very High Resolution Analog-to-Digital Converter at 1 kHz for Space Applications

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## *Abstract*

We present a monolithic, very high resolution Analog-to-Digital Converter (ADC) suitable for high precision space applications. The converter is a low-noise, low sampling rate, radiation hardened device optimized to operate in a frequency range from 0.1 mHz to 1 kHz with nominal output sampling frequency of 6 kHz. System architecture is based on a 2nd order, discrete-time Sigma-Delta (ΣΔ) modulator with 1-bit quantizer and oversampling ratio (OSR) of 64 to 2048. The modulator employs Correlated Double Sampling (CDS) to defeat flicker noise (1/f) and to perform auto-zeroing function. Sampling rates of up to 96 kHz are possible thanks to the selectable OSR feature. The ASIC is implemented in a radiation tolerant 0.15μm CMOS process of Atmel, using a well established and rigorous mixed-signal design flow. An SFDR of 110 dB has been demonstrated with simulations.

## I. Introduction

The commercial availability of high resolution hardened ADCs is rather limited. A market search for high-performance and high reliability converters reveals devices of up to 16 bit resolution, with the majority of the devices offering accuracy between 12 and 14 bits. The power consumption of the available devices is relatively high, and in many cases exceeds 100mW. On the other hand, modern space electronic platforms are becoming lighter, more compact and consume less power. As the scope of the planned space missions becomes ever more challenging, there is a constant need for low power, high-reliability and high-performance signal processing blocks. Apart from the high speed data converters operating at speeds of Msps to Gsps serving the telecommunication applications, there are certain on-board functions that demand low sampling rate and low noise signal processing. Such applications include instrumentation and measurement of slowly changing physical parameters, as well as the accurate monitoring of system parameters for the implementation of reliable spacecraft housekeeping functions. The provision of input for the calibration of current sources or other onboard voltage reference circuits, as well as the implementation of high accuracy control servo-loops, are among the application possibilities. Although the majority of modern microcontrollers feature embedded ADCs, these are low to medium resolution devices. The functions requiring high resolution necessitate the use of an external component.

Based on the aforementioned motivational aspects, we are targeting the very high resolution end of the space ADC market, by proposing an ADC design capable of offering an effective resolution of more than 16 bits over its entire operating bandwidth. Since the device is intended to support low frequency functions, the upper frequency limit of 1 kHz is considered more than adequate. The lower frequency limit is set to the remarkably low value of 0.1 mHz, aiming to serve as a dual specification for a complementary DAC, which was designed and developed under an ESA contract in the past [1], [2].

## II. System Architecture

### *A. Overview*

The very high resolution and low frequency operation of the ADC implies the use of a ΣΔ based oversampling architecture. Oversampling architectures with noise shaping of quantization error are suitable for low and medium speed applications when there is a trade off between accuracy and speed [3], [4], [5].

One fundamental characteristic of the ADC design is that the implementation of the ΣΔ modulator (SDM) is realized in the analog domain. In the literature, as well as in the market, we find that Switched Capacitors (SC) discrete time circuit implementations are preferred to Continuous Time (CT) ones due to a number of advantages. Firstly, the discrete time circuits offer the advantage of loop filter scalability with respect to the modulator sampling frequency. This feature allows the use of the same ADC across several applications requiring different sampling rates with minimum modifications (within a limited range). Secondly, the ability of implementing several sampling techniques has the advantage for reducing the typical non ideal effects of active and passive components and especially flicker (1/f) noise. Furthermore, they offer increased robustness in process variations and insensitivity to clock jitter.

In practice CT circuits are implemented as mixed topology architectures, having a first CT amplifier followed by SC amplifiers. The evaluation of mixed-mode CT/SC ΣΔ modulators was performed in [6]. Although they can significantly reduce the anti-aliasing requirements and also be designed for very low levels of thermal noise power, they are

very sensitive to clock transition uncertainties. For these reasons, SC architecture was chosen for the implementation of the SDM.

### B. *Block diagram*

The system consists of a 2nd order, SDM, followed by a digital decimation filter. The latter, reduces the sampling frequency by a factor of the OSR, to the nominal output sampling frequency of 6 kHz. Note that the Nyquist frequency is three times the signal bandwidth by specification.

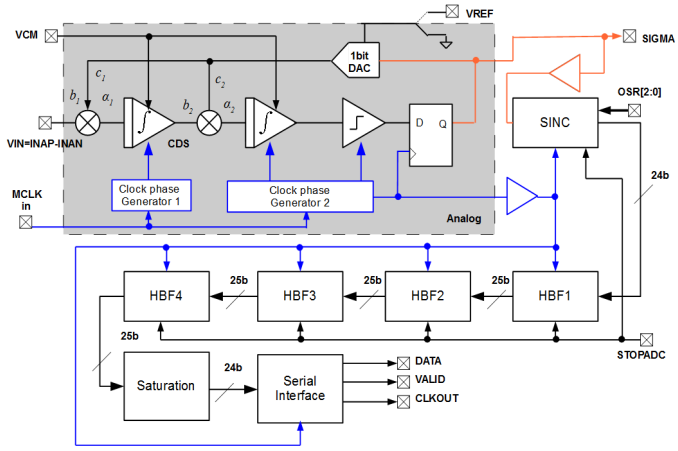


Figure 1: ADC block diagram

The analog voltage to be sampled is applied as a differential signal at the INAP, INAN inputs and is modulated in 1-bit ΣΔ modulation by the SDM block. The discrete-time SDM requires two reference voltages. VCM sets the output common mode voltage of the amplifiers implementing the integrators to obtain a balanced swing and maximize their dynamic range. The 1-bit DAC uses VREF to generate the feedback signals for the integrators.

Two embedded clock generators generate all the required phases for the modulator using an externally provided clock, while the output D Flip-Flop latches the result of the dynamic comparator and drives the ΣΔ modulated signal to the digital part along with the clock. The on-chip decimator can be bypassed using the SIGMA output with different, off-chip filters implemented inside an FPGA or DSP processor for example. This might be useful for mating the modulator with differently tuned filters better suited to the needs of a particular application. The decimator is implemented as a 4th order SINC filter offering selectable oversampling ratios in the range of 64 to 2048, followed by 4 Half-Band Filters (HBF). Each digitized sample is transmitted in 24 bit words over a simple serial output interface along with the clock. The operation of the decimator can be suspended through the STOPADC input to save power, if needed.

## III. ASIC Description

### A. *ΣΔ modulator*

The modulator is a single-stage, 2nd order topology with 1-bit quantizer (Figure 2). It follows the model introduced in [3], and consists of two delayed integrators, each within a gain of 0.5, followed by a comparator acting as a two level quantizer.

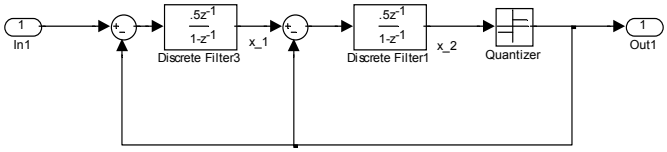


Figure 2: Modulator loop block diagram

The low output sampling frequency of 6 kHz allows the use of an OSR as high as 2048, since it leads to a modulator sampling frequency of 12.288 MHz which is acceptable. Such an OSR with the modulator of Figure 2 was shown to achieve 141 dB of SQNR with regards to quantization noise, with Noise Transfer Function (NTF) given by Eq. 1 and graphically represented in Figure 3.

$$NTF(z) = \left(1 - z^{-1}\right)^2 \quad (1)$$

Note that the formula predicting the SQNR assuming a linear noise model is 154 dB. The toolbox of Schreier [7], however, takes into account the nonlinear nature of the quantizer and results in a realistic prediction of the SNR.

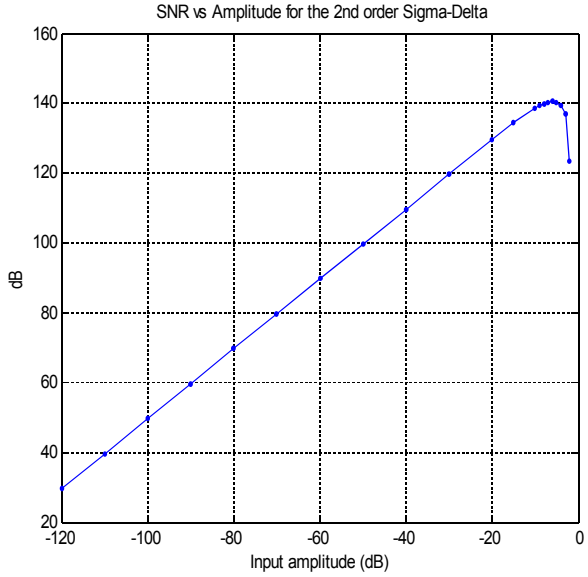


Figure 3: SNR vs. amplitude for a 2nd order modulator based on the describing function approach

Note that the magnitude of the gain of the second integrator is irrelevant as it is followed by a 1-bit quantizer whose output only depends on the sign of the integrator output. The same behaviour would have been obtained by a gain of 2, which leads to an NTF = $(1\text{-}z^{-1})^2$. The effective gain of the quantizer is actually amplitude dependent. This fact is taken into account by the result of Figure 3.

Stability can be guaranteed for second order modulators, while tonal behaviour is not expected to be a problem for this high an OSR.

The ΣΔ output signal is fed back to both integrators using a 1-bit DAC. The feedback and feed-forward scaling coefficients $\alpha_i$, $b_i$, $c_i$ depicted in Figure 1 are implemented as inter-stage capacitance ratios. The applied values are shown in Table 1, where $Cs_x$, $Ci_x$ and $Cf_x$ correspond to the sampling, the integrating and feedback capacitances of each SC integrator, and x $\in\{1,2\}$ denoting the first and second integrator respectively. The values are normalized to the feedback gains $c_1$, $c_2$.

Table 1: SDM coefficients

| | | |
|---|---|---|
| $\alpha_1$ | $Cf_1/Ci_1$ | 1/7 |
| $\alpha_2$ | $Cf_2/Ci_2$ | 0.222 |
| $b_1$ | $Cs_1/Cf_1$ | 1 |
| $b_2$ | $Cs_2/Cf_2$ | 5/2 |
| $c_1$ | 1 | -1 |
| $c_2$ | 1 | -1 |

The schematic topology of the modulator is based on the circuit presented in [8]. That implementation uses a single voltage reference +Vref in contrast with most existing implementations utilizing a symmetrical ±Vref. This simplification, which benefits the component integration at system level, is done at the expense of additional switches to manage the ΣΔ feedback signal. The nominal Vref level equals the supply voltage and is provided externally. To avoid conversion errors, the voltage reference should not be allowed to drop more than ½ LSB. The maximum allowed output impedance corresponding to 18 bit resolution is 86 mΩ.

The implementation of the SC modulator requires two identical non-overlapping clock generators, one level quantizer and two fully differential Operational Transcoductance Amplifiers (OTAs) for the realization of integrators. All the analog switches are implemented as passgates. The 1-bit feedback DAC is realized as combination of switches with respect to Vref. SC integrators and the OTA cell

The SC integrators are based on a fully differential stray insensitive topology for improved CMRR and dynamic range [9]. The simplified schematic is shown in Figure 4.

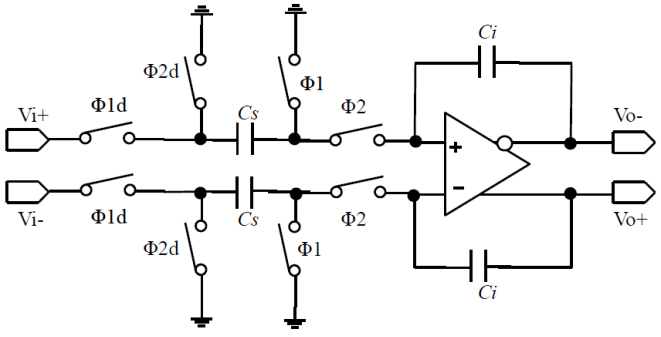


Figure 4: Differential switched capacitor integrator

Each SC integrator requires at least a two phase non-overlapping clock Φ1, Φ2 as shown in Figure 5. However, clock feedthrough from the switches can cause undesired offsets in the form of charge injection, which may distort the original sampled signal. Although the charge injected offset appears as a common mode signal at the amplifier inputs and is largely suppressed by the input differential stage, sensitivity to clock-feedthrough can be further reduced by using two additional clock phases as shown in Figure 5 [10]. The delay at the trailing edge of each clock pulse $t_d$ aids in sinking the stray charge towards the input and ground, during the sampling and integrating phases respectively. The amount of delay was set to 3ns.

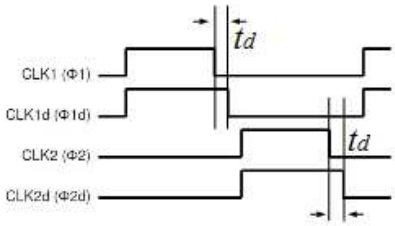


Figure 5: 4-phase clock

The amplifier of each integrator is implemented as a rail-to-rail two stage OTA (Figure 6). The first stage consists of a differential amplifier with current source active loads, followed by a common source stage. The necessary bias voltages are generated internally by a voltage bias network using a fixed current of 5μA generated by a current reference cell. To ensure proper operation of the amplifier a transistor based Common-Mode Feedback Circuit (CMFB) is added to the output to regulate the output common-mode voltage irrespective of the output voltage swing. The entire cell operates from a single 3.3V power supply and dissipates around 2mW. The RC network consisting of X1/X7 and X2/X0 attenuates the feedback signal at high frequencies to prevent oscillations and improve the stability.

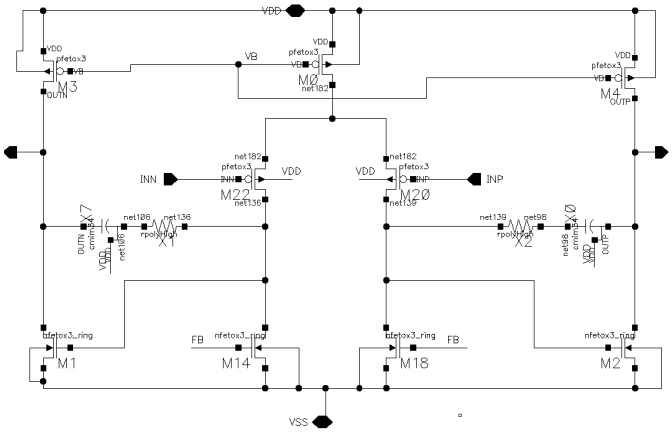


Figure 6: OTA schematic

Despite the relatively high GPBW of the amplifier, which measures 146 MHz and its output slew-rate reaching 225V/μs, the overall performance of the modulator is significantly degraded at switching frequencies higher than 7 MHz. Consequently, the circuit was optimized for operation at half the theoretical modulator frequency, which equals 6.144 MHz. This practically limits the maximum OSR at 1024, which in turn reduces the SNR from 141dB to 125dB.

## *B. Sampling capacitor*

Apart from the non linear nature of the modulator, another limiting factor is the sampling capacitance value.

It can be shown that the minimum value of sampling capacitance which is required in order to achieve a certain SNR figure for a given OSR, is provided by Eq. 2 [4].

$$C_{\min} = \frac{8kT\,SNR^2}{V_{IN}^2 OSR} \qquad (2)$$

where, the SNR is in linear scale of value $10^{125/20}$, $k$ is the Boltzmann constant 1.38 x $10^{-23}$ $JK^{-1}$, $T$ the maximum temperature for full performance in K and $V_{IN}$ the full scale input voltage for maximum SNR in V. The factor of 8 accounts for the two paths through which thermal noise is sampled during each phase (Φ1 and Φ2) and the fully differential topology of the circuit.

Thus in our case:

$$C_{\min} = \frac{8\times 1.38\times 10^{-23}\times(273+50)\times 10^{12.5}}{3.3^2\times 1024} = 10\,pF \qquad (3)$$

This value of capacitance was proven to be large for the actual circuit, after the entire schematic was initially simulated. Due to that limitation, a capacitance of 0.7pF was eventually realized, which further limits the achievable SNR to 113dB.

## C. Low frequency noise reduction

The reduction of flicker (1/f) noise is an important consideration, since the ADC is required to operate well below the sub-Hz region. Two effective techniques exist in the literature, which offer significant amplifier flicker noise reduction, the Chopper Stabilization Method (CHS) and the Correlated Double Sampling (CDS). Both techniques can be applied quite easily in SC circuits because of their inherent sampling process.

The CDS technique can be treated as a particular case of auto-zeroing (AZ), where the amplifier noise and offset are sampled twice in each clock period and stored in an extra capacitor [11]. The stored noise plus the offset are then subtracted from the input sample. The CDS technique can be readily applied to SC amplifiers to reduce amplifier's offset and noise as well as to lower the effect of the finite amplifier gain [11]. Due to the sensitivity of CHS to the switching signal shape as well as layout parasitics [12], CDS was the low frequency noise reduction technique selected for the ADC. In terms of implementation, CDS requires one additional switch and one capacitor per polarity in the first integrator only. The addition of CDS to the second stage is not necessary, since the noise and offset of the second amplifier are noise shaped by the modulation process, and their effect on the overall performance is considered as minimal.

## D. 1-bit quantizer

The 1 bit quantizer is implemented as a regenerative latched comparator followed by a D flip-flop (Figure 7). The topology is based on the work performed in [13] and was selected because of its high-speed and high-sensitivity operation.

The block consists of two stages; the circuit consisting of M10, M6 and M9 comprise an amplifier, which amplifies the voltage difference between inputs INP and INM as $V_D=V_{INP}-V_{INM}$. The second stage consisting of M1-M4 forms a regenerative latch that compares $V_D$ to the ground potential (0V). The two possible output states of the comparator depend on the magnitude of $V_D$ with respect to the zero potential; if $V_D>0$ the output goes to VDD (logic high), and when $V_D<0$ the output goes to 0 (logic low).. Transistors M0, M7 and M8 operate as switches enabling the comparison process only when CLK is High. In fact, M7, M8 isolate the amplifier stage from the regeneration stage while M0 clears the previous latched state and initializes the output for a new comparison cycle. The comparator is biased from an external reference at the gate of M9, which sets the tail current of differential pair M10, M6 and consequently the gain of the amplifier stage. The achieved sensitivity is less than 10 μV.

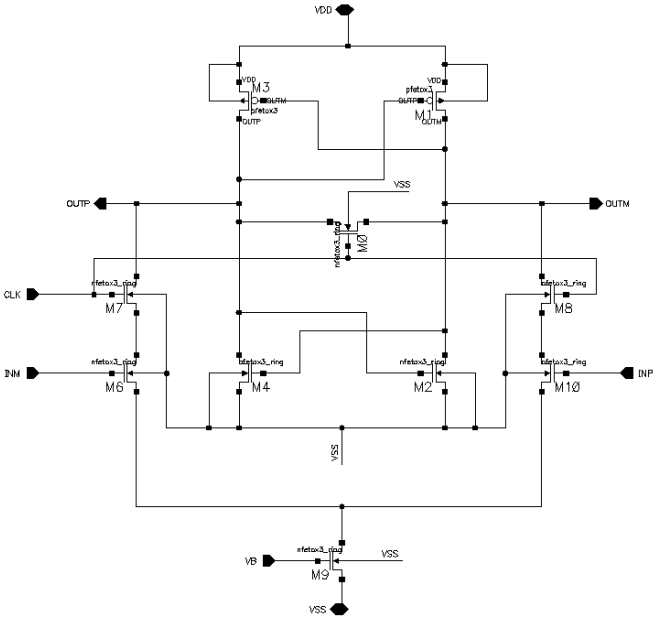

Figure 7: Comparator schematic

## E. Clock phase generator

Since all of the switches are implemented as pass gates, complementary clock phases are also required. The embedded clock generator of Figure 8 generates eight non-overlapping clocks synchronized with the modulator clock. The circuit is instantiated twice (one per integrator stage). This is to obtain a symmetrical and simplified layout and to minimize the trace length, thus avoiding synchronization problems between the different stages.

## F. Decimator Filter

The Decimator filter consists of two main sections: (i) the SINC decimation stage and (ii) the multiple Half-Band decimation stages. Since the nominal OSR is 2048 we had a factor of 128 implemented by a 4$^{th}$ order SINC followed by four stages of HBF realizing a factor of 16, so that 128 * 16 = 2048.

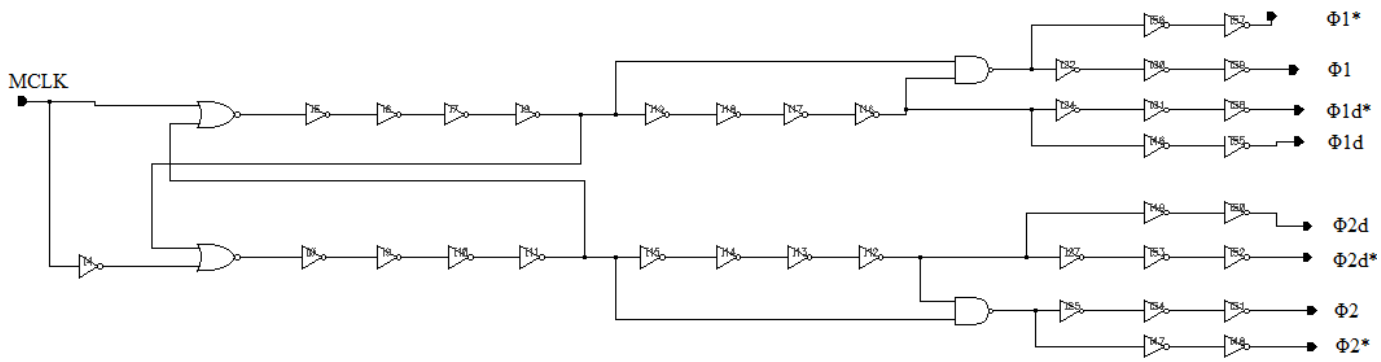


Figure 8: Clock phase generator schematic

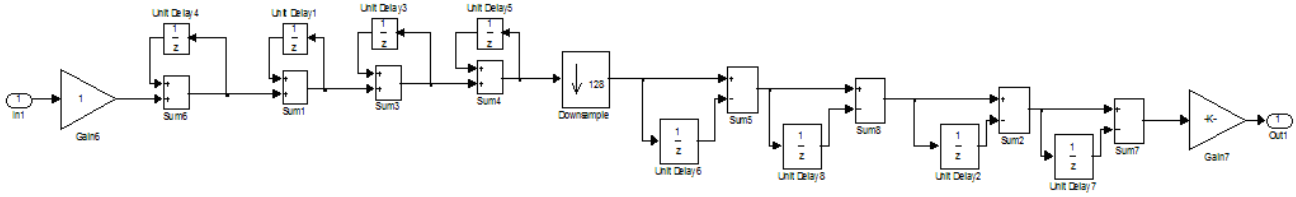


Figure 9: CIC SINC block diagram

*1) SINC filter*

The fourth order SINC is equivalent to a cascade of four rectangular moving average filters. A Cascaded Integrator-Comb (CIC) implementation is chosen as shown in Figure 9. The CIC implementation is very efficient both in terms of arithmetic computation and in terms of required memory elements. The input comes from the quantizer and it is a +1 or a -1 which may be described by two bits. Following is a cascade of four integrators/accumulators. Following the accumulators there is a decimator by $2^7$=128 and following that is a cascade of four difference filters. All the arithmetic is implemented by 30 bit wide accumulators and differentiators. Any scaling is performed at the end of the chain. The accumulators do actually overflow, however the result is correct, provided the bit width is at least 30. The group delay of the SINC filter is 4x (128/2) = 256 taps of the input frequency or 1/8 sample at 6 kHz which is 0.02 ms.

*2) Half Band Filters*

Four half band filters (HBF) are used each realizing a decimation by a factor of two starting from a frequency of 16 * 6 kHz = 96 kHz. All filters have pass-band of 1 kHz and stop band of Nyquist frequency minus 1 kHz. These are equiripple filters that result in all even order coefficients being zero apart from the center one. These filters may be determined by their order and their pass-band frequency normalized by the Nyquist frequency at the input of their filter stage: $F_O = F_p / (F_s/2)$. The design parameters of each HBF are summarized in Table 2.

Table 2: HBF design parameters

| Filter ID | Order | Normalized pass-band frequency (Fo) | Sampling frequency (kHz) |
|---|---|---|---|
| HBF1 | 6 | 1/48 | 96 |
| HBF2 | 10 | 1/24 | 48 |
| HBF3 | 14 | 1/12 | 24 |
| HBF4 | 22 | 1/6 | 12 |

The group delay of the combined HBF is: 129 / 96 = 1.344 ms. The low-frequency end of the overall decimator magnitude frequency response is plotted in Figure 10.

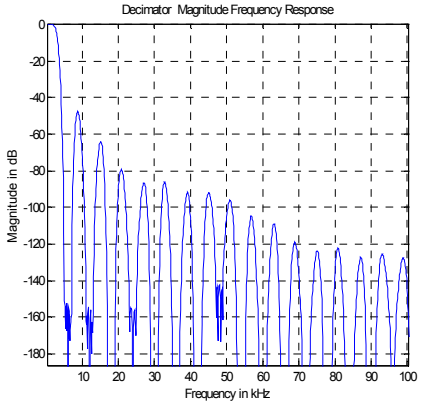


Figure 10: Magnitude response of decimation filter up to 100 kHz

All the frequency regions that will be aliased onto the pass-band (0 to 1 kHz) after decimation are suppressed to at least -140dB. These frequency regions are centred around integer multiples of the output sampling frequency of 6 kHz plus-minus the pass-band frequency $F_p$ = 1 kHz. The in-between bands are not suppressed and are used as transition zones to help reduce the order of the filters.

Note that the first (lowest frequency) zero pair from SINC comes at 96 kHz. The SINC order is chosen so that from 95 to 97 kHz the response lies below -140 dB. The stop-bands at frequencies below 96 kHz are contributed by the HBF.

## IV. Radiation Hardening

The ADC is implemented in a single-poly, 5-metal, 0.15µm CMOS on SOI radiation hardened process of Atmel. The digital part is synthesized using the robust cells from the library, including latches and flip-flops with increased area. Triple Modular Redundancy (TMR) is used for every flip-flop and finite state machine along with voting scheme, as a highly effective fault tolerance technique in masking Single Event Effects (SEE). As an added measure, the reset is synchronized with the clock.

The analog part is hardened using relaxed layout rules, guard rings and extensive use of enclosed layout NMOS transistors (ELT). ELT transistors can greatly improve the analog degradation due to TID effects, which can be caused by radiation induced charge trapping in the oxides or at the Si interface [14]. The layout is almost totally immune to Single Event Latch-up (SEL) thanks to the deep trench isolation option (DTI). Each CMOS structure is isolated using a deep trench extending down to the buried oxide of the SOI, as shown in Figure 11. This arrangement cuts away the parasitic SCR devices inherently present in the CMOS structure that may trigger SEL events. The target LET for SEL immunity is greater than 70 MeV/mg/cm$^2$. The target figure for TID tolerance is 100 krad (Si).

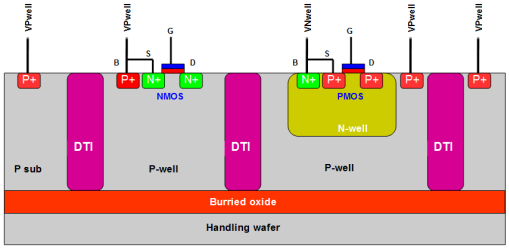


Figure 11: layout cross-section

## V. Simulation Results

Due to the small size of the analog core compared to the digital one, the chip layout is pad limited as shown in Figure 12. The total area including the core and the I/O pads measures 9.0mm$^2$. All the capacitors in the signal path are of MIM type.

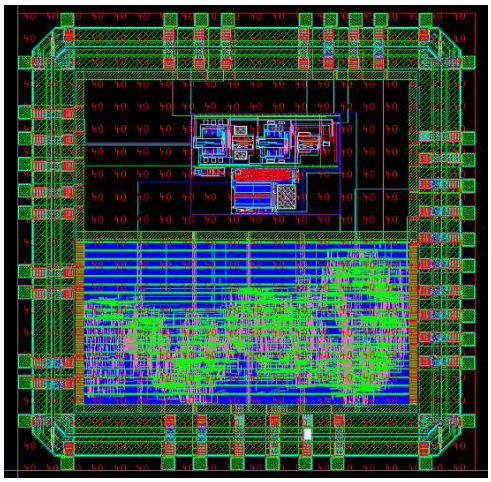

Figure 12: ADC chip floorplan

The dynamic performance of the SDM was evaluated by running post layout transient simulations in Spectre$^{TM}$, followed by FFT analysis. The block is driven with a 750Hz sine wave signal and amplitude 3.2Vpp differential. Then a transient simulation is run for two complete sine wave cycles and the ΣΔ modulated output is obtained at the time domain. Due to the very long simulation times, it is not practical to acquire more cycles. The frequency spectrum is then generated by performing post FFT analysis on the simulation data using Matlab$^{TM}$. Note that the ΣΔ signal is partially filtered before the FFT by passing it through the first stage of the decimator SINC.

The output spectrum of the ADC and the reconstructed output waveform at 25°C are shown in Figure 13 and Figure 14 respectively. The obtained performances of the ADC are summarized in Table 3.

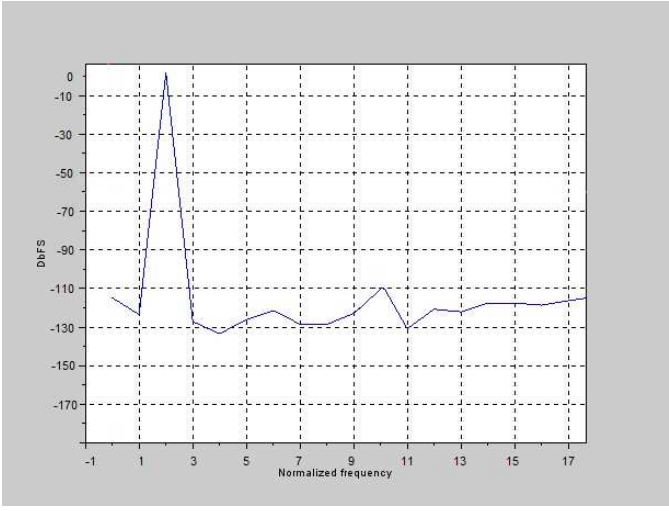


Figure 13: FFT sine 750Hz 0dBFS at 25°C

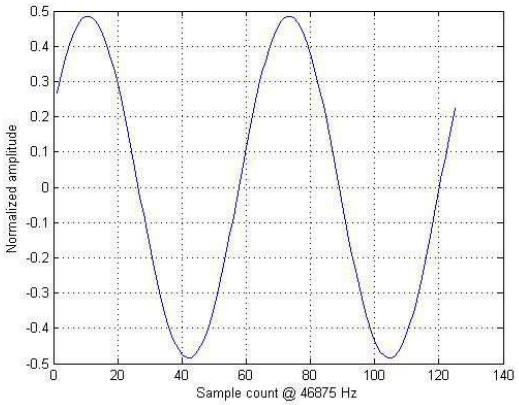


Figure 14: reconstructed signal at the output of the decimator

Table 3: ADC Performance Summary

| | |
|---|---|
| Sampling Rate | 6ksps to 96ksps |
| Rated bandwidth | 0.1 mHz – 1 kHz |
| Practical bandwidth | DC to 16kHz |
| Clock frequency, nominal | 6.144 MHz |
| Differential input swing | ± 1.6Vpp |
| SFDR | 110 dB |
| Digital power supply | 1.8 V |
| Analog power supply | 3.3 V |
| Power Consumption (modulator only) | 2.2mA |
| Area (core & I/O) | 9.0 $mm^2$ |

## VI. Conclusion

A low speed, very high resolution, radiation hardened ADC was designed in CMOS. Simulation demonstrated a resolution of 18 bits while the analysis indicated the capability of the selected architecture to exceed 22 bits. The detailed design process reveals that the ΣΔ modulator is the most critical part of the design, yet the most challenging to optimize for low noise and high-speed operation. The chip validation in silicon will demonstrate how closely the theoretical performance limit could be reached by this ADC.

## VII. References

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