Development of a high-speed and high-resolution ADC for image processing applications

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Abstract

The abstract will present the ESA project for developing a high-speed and high-resolution ADC, performed by SPACE ASICS together with Kayser-Threde GmbH. The built-in analog front-end is discussed as well as the key performance requirements and functional requirements of such an ADC. Because verification of such an ADC is very challenging a previous test setup is shown and verification methods and algorithms are presented. Conclusions for testing of the ADC are drawn from the results and evaluation of the previously acquired data.

Additionally, the abstract will address potential ADC users and will request their feedback regarding the functional and performance requirements of the ADC.

I. Introduction

Today there is no space suitable solution in Europe for high-speed (e.g. 20 Msps) and high-resolution (16-bit) Analog-to-Digital Converters (ADC) to process and digitise analog output signals from image sensors or other high resolution instruments. Such devices would enable new applications with higher performance. In addition, it would guarantee European independence and reduce the dependence on COTS devices and their associated screening costs and time.

Therefore, ESA has initiated a program for developing such a high-speed and high-resolution ADC. In the framework of this program SPACE ASICS (Greek) will develop such an ADC together with Kayser-Threde GmbH (Germany) and others.

As the ADC application is targeted to image processing with CMOS and CCD sensors an analog front-end is also implemented in the ADC providing typical analog processing as used for readout of imaging sensors.

Verifying the characteristics of an ADC with such high dynamic performance can prove very challenging as the evaluation environment has to be designed such that it provides even better performance than the device-under-test (DUT). Eliminating any kind of noise caused by signal generators or external circuitry is a key aspect designing the test environment. Additionally, the choice of suitable measurement techniques and test conditions is important for an accurate determination of the performance characteristics and demanded test equipment.

II. Requirements

Modern CMOS and CCD imaging applications call for high-speed ADCs with sampling rates of about 20 Msps. Currently, space qualified ADCs are only available with a sampling rate of about 4 Msps with appropriate resolution. This small sampling rate is a restriction for many applications, therefore, a high sampling rate of 20 MHz is required in the framework of this project. In addition, high precision data acquisition is also required for such type of application, which results in an ADC resolution of 16-bit. This high-speed and high-precision performance shall be reached with a quite low DC power consumption of about 100 mW, at a maximum sampling rate, which is very challenging because the process selection is limited to space suitable SiGe processes only. Table 1 lists the key performance requirements to be considered for the development of the ADC.

Table 1: Converter performance parameters

Parameter	Value
No. of bits	16
Max. sampling rate	20 Msps
Full scale input voltage (diff.)	max. 4 Vpp
INL (integral nonlinearity)	±5 LSB
DNL (differential nonlinearity)	±1 LSB
SNR (signal-to-noise ratio)	> 92 dB
ENOB (effective number of bits, SNR based)	15 Bit
Power consumption	<100 mW (@ 20 Msps and serial output)
Temperature range	-55 °C to 125 °C
Radiation tolerance	TID: 100 krad(Si) SEE: 70 MeV-cm^2/mg

It can be seen that also a very challenging noise requirement of signal-to-noise ratio (SNR) of 92 dB exists. This can be directly converted to an SNR-based effective-number-of-bits (ENOB) of 15 bits.

III. Architecture

After an investigation and evaluation of typical imaging space applications on the basis of CCD or CMOS sensors, a preliminary block diagram of the ADC is consolidated in the

first phase of the activity. This preliminary block diagram is shown in Figure 1. A high degree of user configuration capability is considered for this design as well as appropriate testing capabilities, realized by analog in- and outputs or user configurable switches.

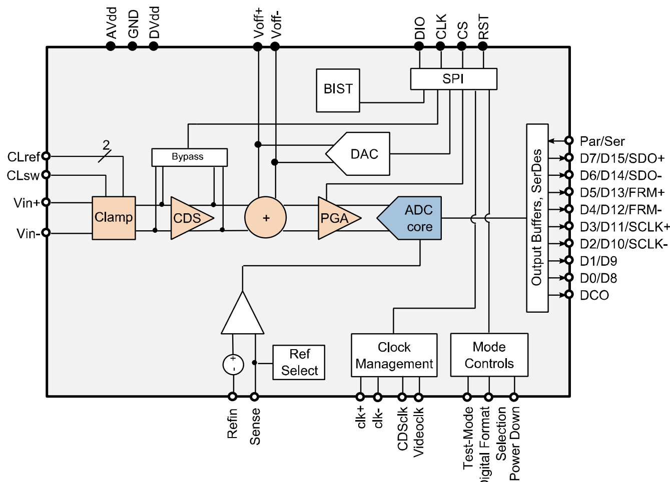

Figure 1: Simplified converter architecture

A. *Key features*

Besides the ADC core building block a complete analog front-end is integrated inside the chip for easy sensor readout without the need for additional and complex discrete electronics before the ADC chip. Some applications may require just a small line driver close to the sensor. The built-in analog front-end consists of .

- Analog adjustable and switchable clamping circuit
- Correlated double sampling with switchable bypass
- Offset correction, adjustable by analog input or by digital configuration interface
- Gain amplifier, programmable via digital configuration interface.

Besides the analog front-end functionalities the ADC will provide the following features in order to enable a user friendly configuration:

- Integrated and configurable clock management
- SPI configuration interface
- Digital output interface, switchable by hardware pin to 2x8 bit parallel output (CMOS) or serial LVDS output.

IV. Test Environment

The measurement setup for the analog-to-digital converter, including the evaluation board and the test equipment, must offer high performance, so the specified parameters can be verified. The requirements for the test setup are derived in such a manner that these specifications are still measurable considering the measurement techniques based on the descriptions made in the IEEE Standard for Terminology and Test Methods for Analog-to-Digital Converters [1].

Figure 2 gives an overview of a general ADC measurement setup with sine-wave input signals. The evaluation board can be split into the following sub-circuits which are

- Analog front-end
- Clock distribution
- Power distribution
- Digital interface.

A close-up figure of the evaluation board is shown in Figure 3 corresponding to those parts.

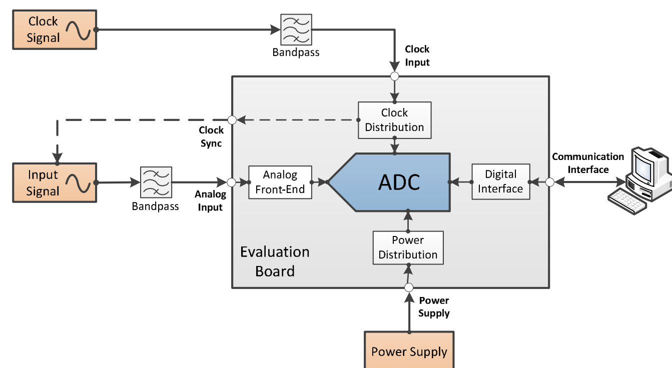

Figure 2: Block diagram of the test setup

Apart from the ASIC, the measurement setup includes the external power supply, a sine wave signal source followed by a bandpass filter which is used as the analog input signal and another sine wave source as clock input. The clock source is fed back to the input signal source as a reference signal to achieve phase synchronization between these instruments.

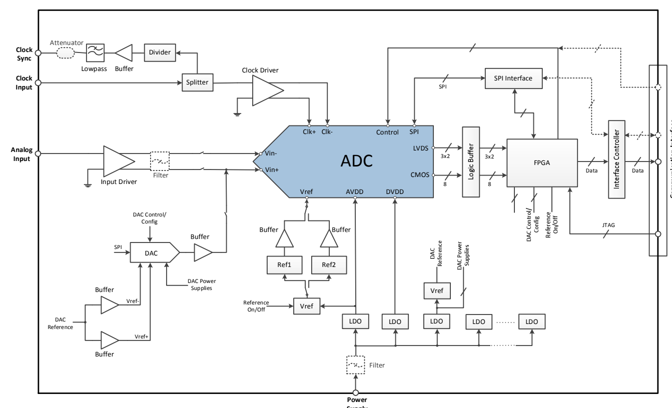

Figure 3: Detailed view of the test environment

A. *Static parameters testing*

The key static parameters include the integral nonlinearity (INL) and differential non-linearity (DNL) as well as the offset and gain error.

There are several methods available to test linearity of ADCs such as feedback loop, static code transition measurement or statistical approaches. Statistical analysis is simple and easy to apply so that it is one of the most typical test methodologies. The basic idea of this method is to count the number of times one of the 2N output value bins of the converter is hit. This number has to correlate to the input in a

certain way depending on the input signal form. The deviation from the ideal distribution of the output values is represented in the static parameters.

Accurate narrow-band test signals are generated with a high spectral purity. Consequently, the sine wave stimuli have gained increasing interest as the input signal to be used when estimates are needed of the converter non-linearities. Nevertheless, the setup is built in a way that we can use a high precision digital-to-analog-converter (DAC) to measure the monotony of the device-under-test (DUT) which makes it also possible to verify the static parameter using different approaches (for example feedback loop).

B. Dynamic parameters testing

The dynamic parameters include the total harmonic distortion (THD), spurious-free dynamic range (SFDR), signal-to-noise ratio (SNR), signal-to-noise-and-distortion (SINAD) and the effective number of bits (ENOB).

Few general test setups can be used testing the ADC parameters. Sine wave, arbitrary waveforms, and pulse signals are commonly used evaluating the mentioned parameters. The architecture of the proposed test environment is designed to allow testing with all mentioned stimuli sources.

V. ACKNOWLEDGMENT

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VI. REFERENCES

[1] IEEE Standard for Terminology and Test Methods for Analog-to-Digital Converters," IEEE Std 1241-2010 (Revision of IEEE Std 1241-2000) , vol., no., pp.1,139, Jan. 14 2011.