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Development of an High Speed and High Resolution ADC for Image Processing Applications

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Today there is no space suitable solution in Europe for high speed (e.g. 20Msps) and high resolution (16 bit) Analogue-to-Digital Converters (ADC) to process and digitise analogue output signals from image sensors or other high resolution instruments. Such devices would enable new applications with higher performance. In addition it would guarantee European independence and it would reduce the dependence on COTS devices and their associated screening costs and time.

Therefore ESA has initiated a program for developing such an high-speed and high resolution ADC. In the framework of this program SPACE ASICS (Greek) will develop such an ADC together with Kayser-Threde GmbH (Germany) and others.

The paper will present the project objectives, planning and will define and present the key performance requirements for the ADC under development. Because the ADC application is targeted to image processing with CMOS and CCD sensors an analogue front end is also implemented in the ADC providing typical analogue processing as used for readout of imaging sensors. The paper will present and discuss this analogue front end, including clamping, correlated double sampling and adjustable offset and gain correction. Furthermore all other functional requirements are presented and discussed.

Verifying the characteristics of an ADC with such high dynamic performance can prove very challenging as the evaluation environment has to be designed such that it provides even better performance than the device-under-test (DUT). Eliminating any kind of noise caused by signal generators or external circuitry is a key aspect designing the test environment. Additionally, the choice of suitable measurement techniques and test conditions is important for an accurate determination of the performance characteristics and demanded test equipment. The abstract will present verification methods and algorithms and will show previous test results, performed for evaluation of the test environment. Conclusions for testing of the ADC are drawn from the results and evaluation of the acquired data. For each sub-part of the evaluation board including the corresponding signal generators that generates the input signal, solutions are presented how the necessary performance and functionality can be achieved. Furthermore, selected measurement techniques will be presented that have proven to be suitable to verify and characterize the 16-bit analog-to-digital converter and provide a good basis for the development of the final evaluation environment once the prototypes of the ADC are realized.

Furthermore the paper shall address potential users of the ADC and shall present the procedure of a market survey to be performed in the framework of the project. Potential users shall be identified and appropriate feedback about performance and functionality of the ADC shall be requested.

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