

Analog FTU Hardware Debugging System

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Abstract

What is AFTU?

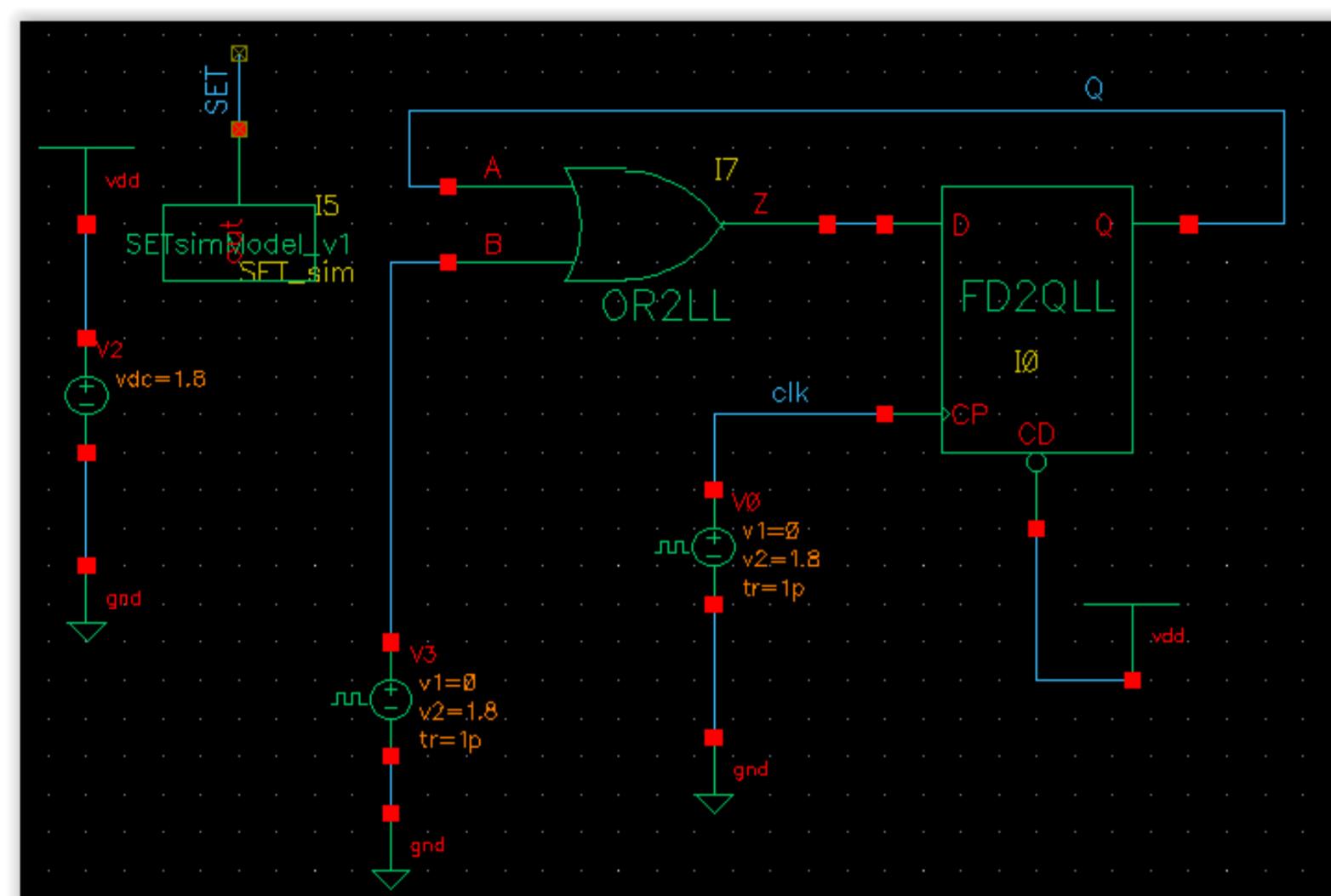
AFTU is a tool to evaluate the SEE sensitivity of analog/mixed signal circuits at transistor level

What can AFTU offer?

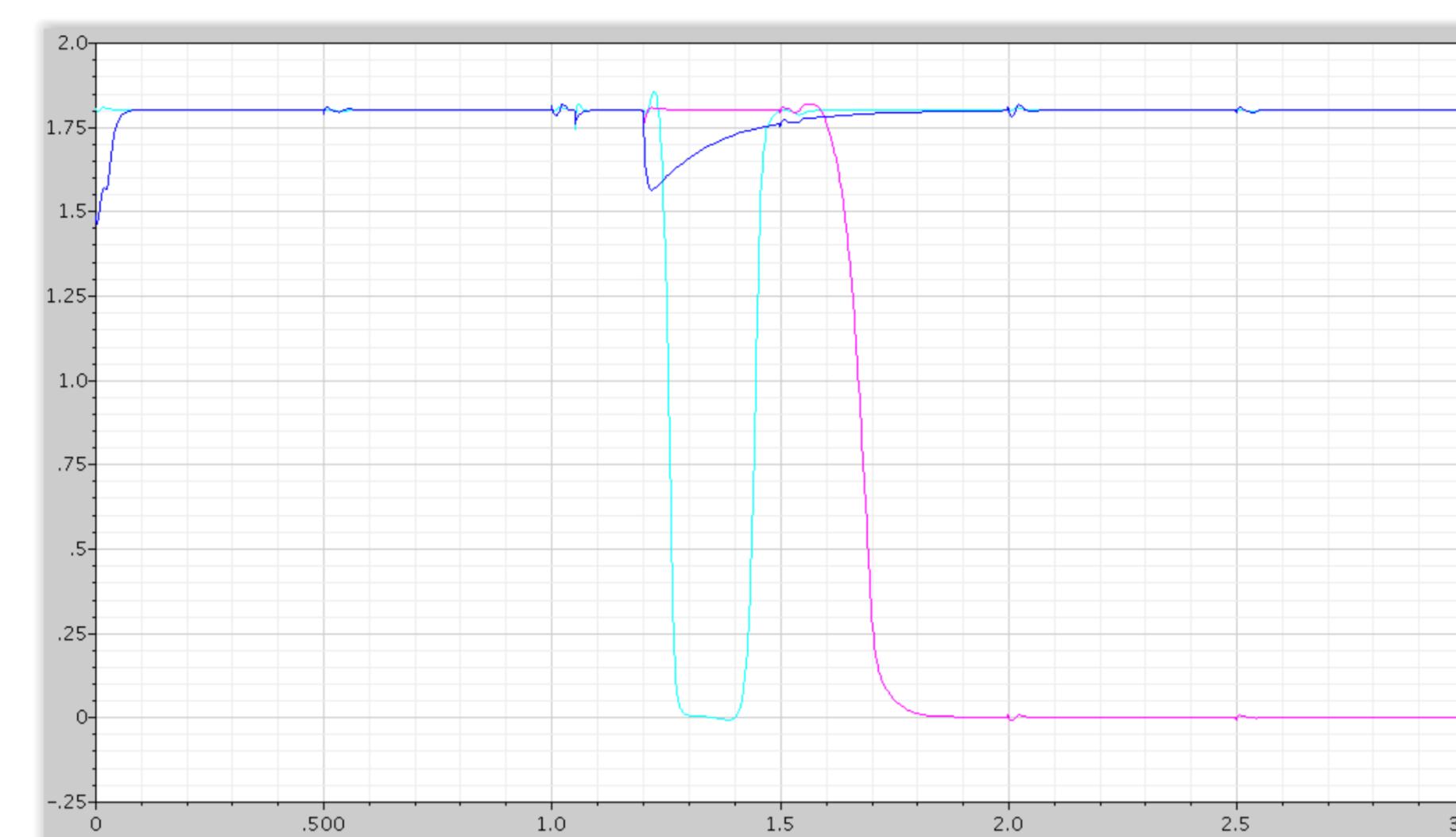
The capability of performing a rapid diagnostic over circuits for radiation-hardened systems in early stages of the design to strengthen their robustness

How Does AFTU Work?

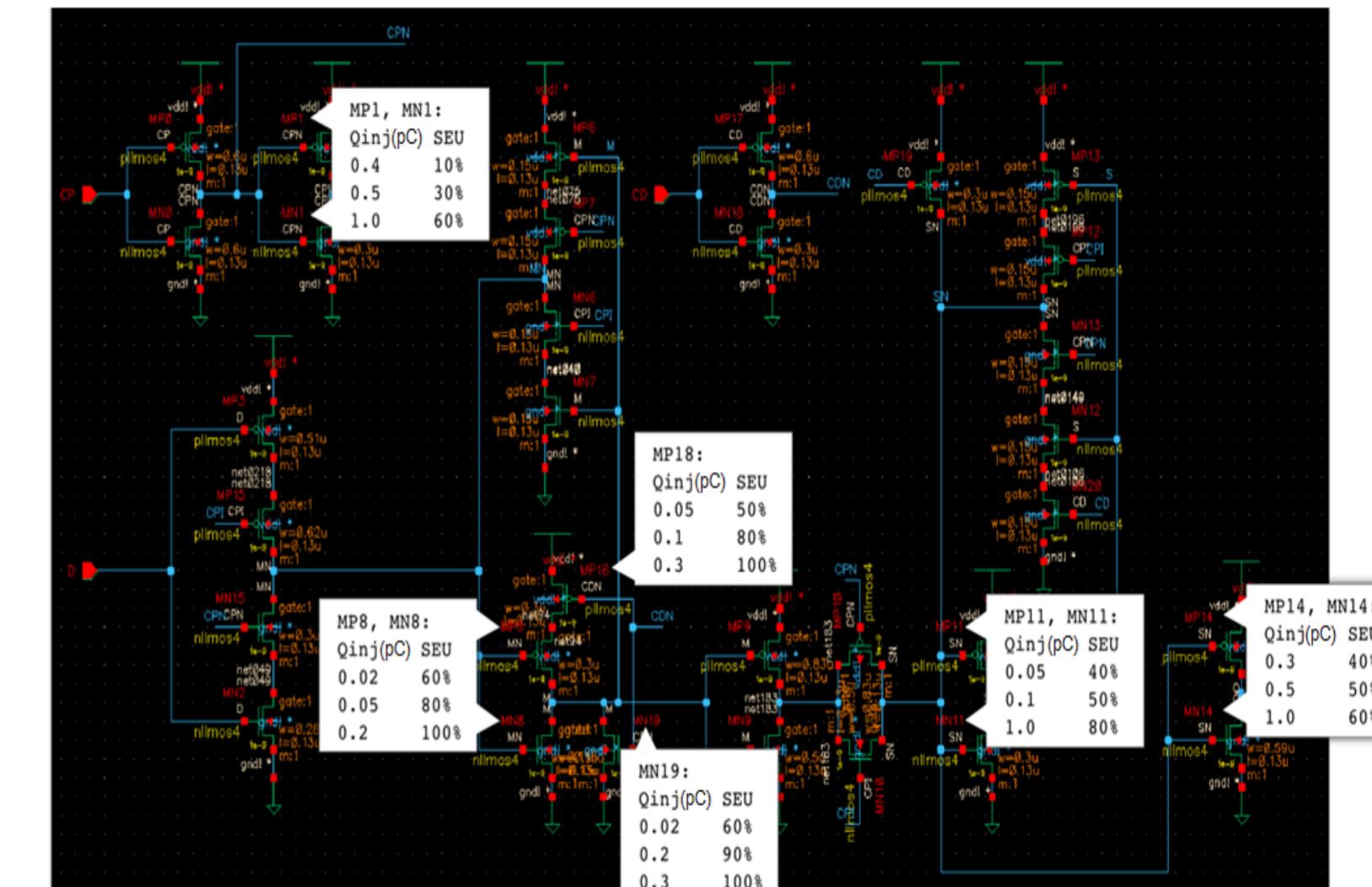
AFTU takes a Spectre design



Emulates radiation conditions



And evaluates SEE sensitivities



AFTU Toolchain

Before using AFTU

The user designs a circuit with Cadence as usual
The design is simulated through a testbench
Of all files generated by Cadence, we pick the netlist

The instrumentalizer implements a parser for the SPECTRE language

Replaces the netlist with a functionally identical one allowing radiation emulation
netlist.nodes lists all observable circuit nodes
netlist.sources lists all transistors where an impact can be emulated

AFTU projects are flexible and give the user many options for analysis

config contains paths, times, heuristics, initial values...
watch defines all elements in the circuit to be observed during simulation
inject defines where, when and how much charge we inject (radiation emulation)

From all this data, a simulation script is produced

including all paths and required data
describing the way to perform the user defined test campaign
defining how to analyze the results of the campaign
The provided script is ran by Cadence, generating a CSV file with the desired statistics
This uncovers radiation vulnerabilities in the circuit

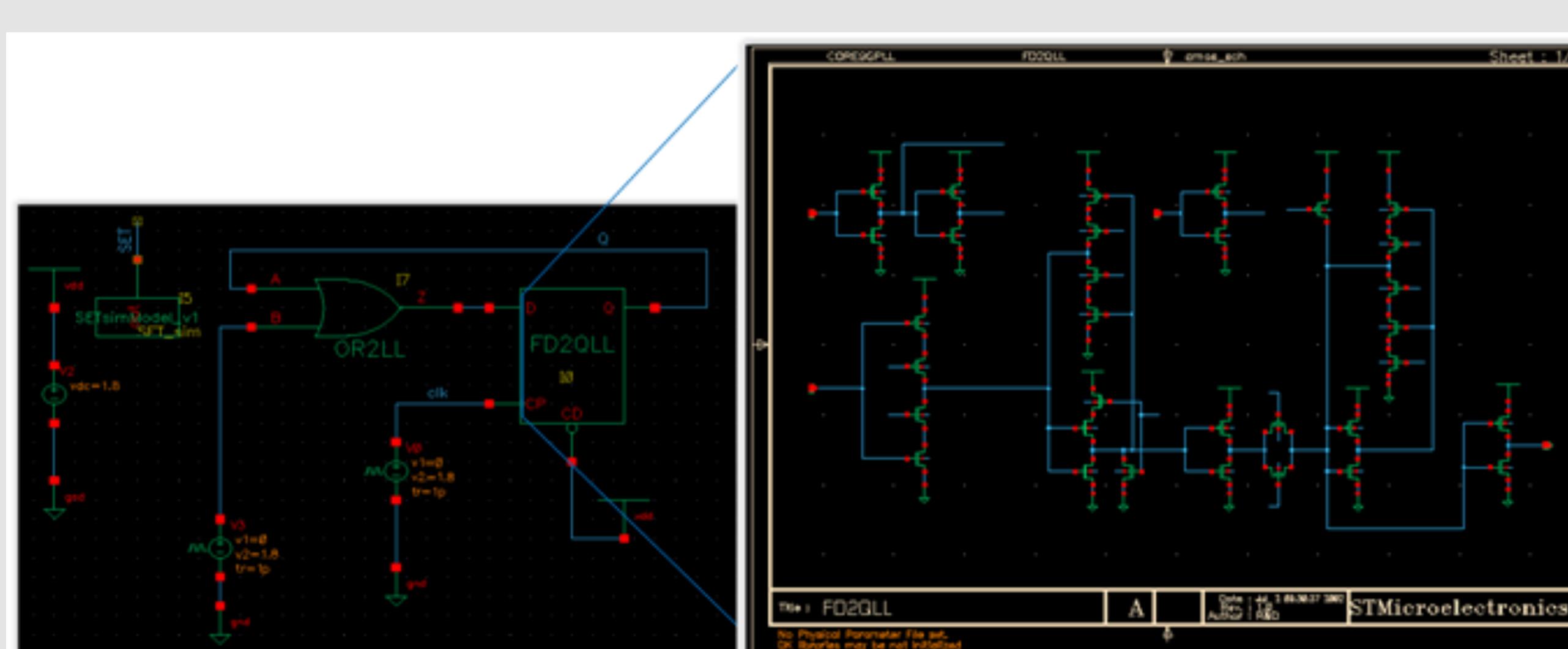
Conclusions

A tool for automatic analysis of SEE sensitivity in analog/mixed signal circuits has been developed

Allows impact emulation, based in current injection models, in every transistor of a given design by means of configuration files (config, inject, watch)

Implements different heuristics for results classification and allows the analysis of every node of the circuit or composed signals defined by the user

Several technologies (ST Microelectronics 130nm CMOS, IHP 250 SIGE BiCMOS, UMC 180nm CMOS) are supported



Determine the critical charge that generates a Single Event Upset in a latch for a ST 130nm CMOS technology

Inject

```
inject I0_MP19:
  Q = .025p, .05p, .1p, .2p, .5p,
  .75p, 1p;
  t = 1.0n : 1.9n : 0.1n;
inject I0_MN19:
  Q = .025p, .05p, .1p, .2p, .5p,
  .75p, 1p;
  t = 1.0n : 1.9n : 0.1n;
inject I0_MP18:
  Q = .025p, .05p, .1p, .2p, .5p,
  .75p, 1p;
  t = 1.0n : 1.9n : 0.1n;
```

Watch

```
watch Q = /Q :
  threshold = 0.975 ;
```

Results

	Output	ImpactNode	Qinj	Tim	Trec/1ns	Vmax
V_Q	I0_MN11	2.5e-14	1e-09	0.000000	0.006827	
V_Q	I0_MN11	2.5e-14	1.9e-09	0.000000	0.016568	
V_Q	I0_MN11	5e-14	1e-09	0.000000	0.017084	
..						
V_Q	I0_MN11	5e-14	1.3e-09	0.000000	0.005371	
V_Q	I0_MN11	5e-14	1.4e-09	1.610000	1.806680	
V_Q	I0_MN11	5e-14	1.5e-09	1.500000	1.806814	
V_Q	I0_MN11	5e-14	1.6e-09	1.400000	1.805740	
V_Q	I0_MN11	5e-14	1.7e-09	1.300000	1.802925	
V_Q	I0_MN11	5e-14	1.8e-09	0.240000	1.404223	