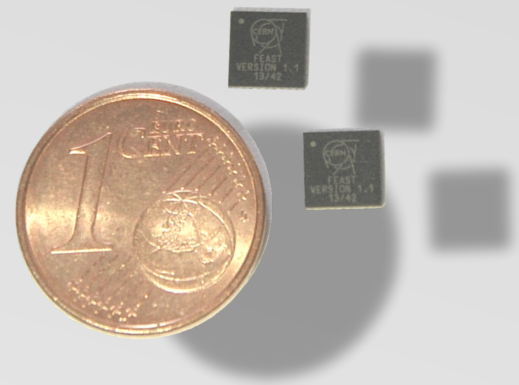

A radiation-tolerant Point-Of-Load buck DC-DC converter ASIC DC-DC for LHC upgrades

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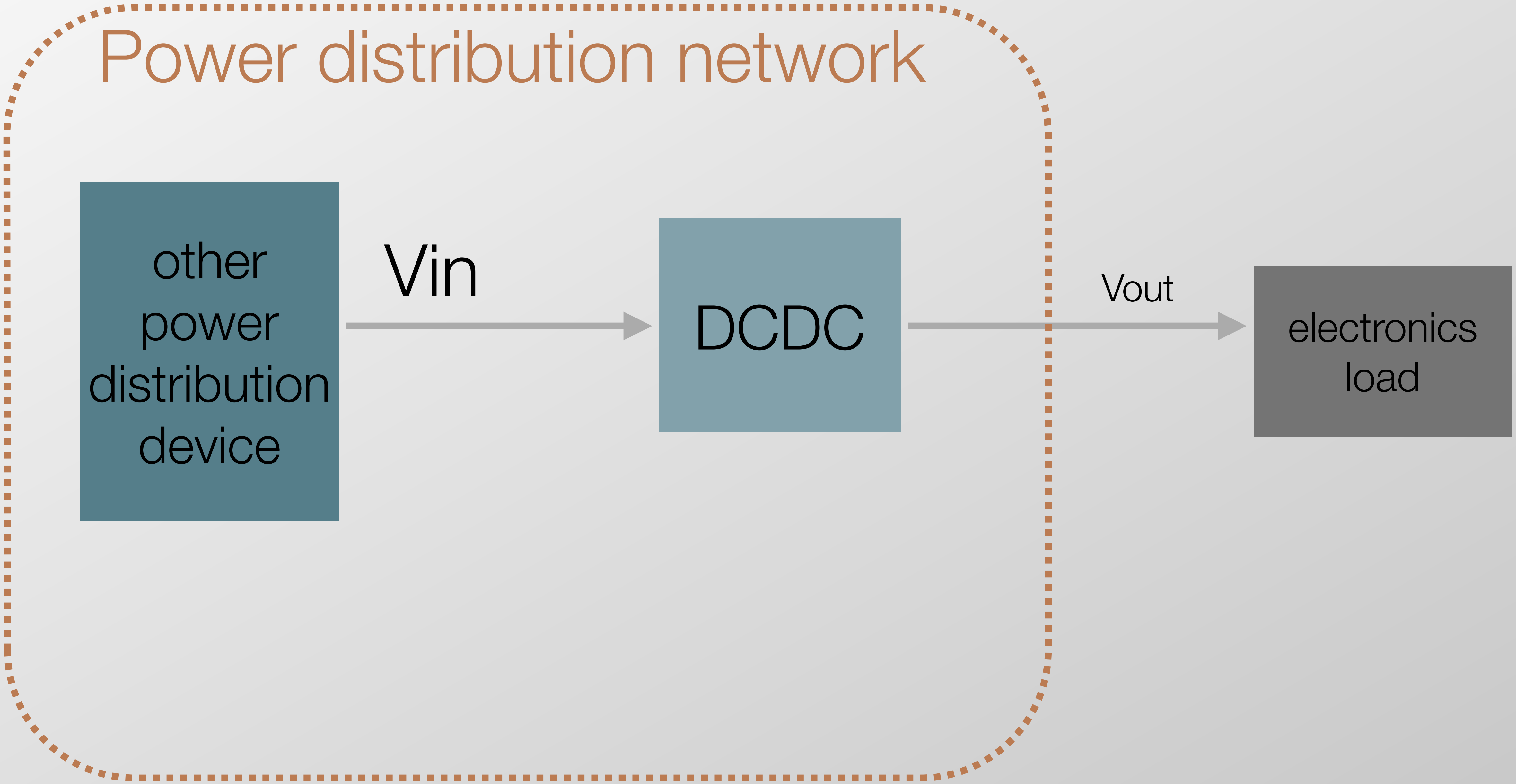
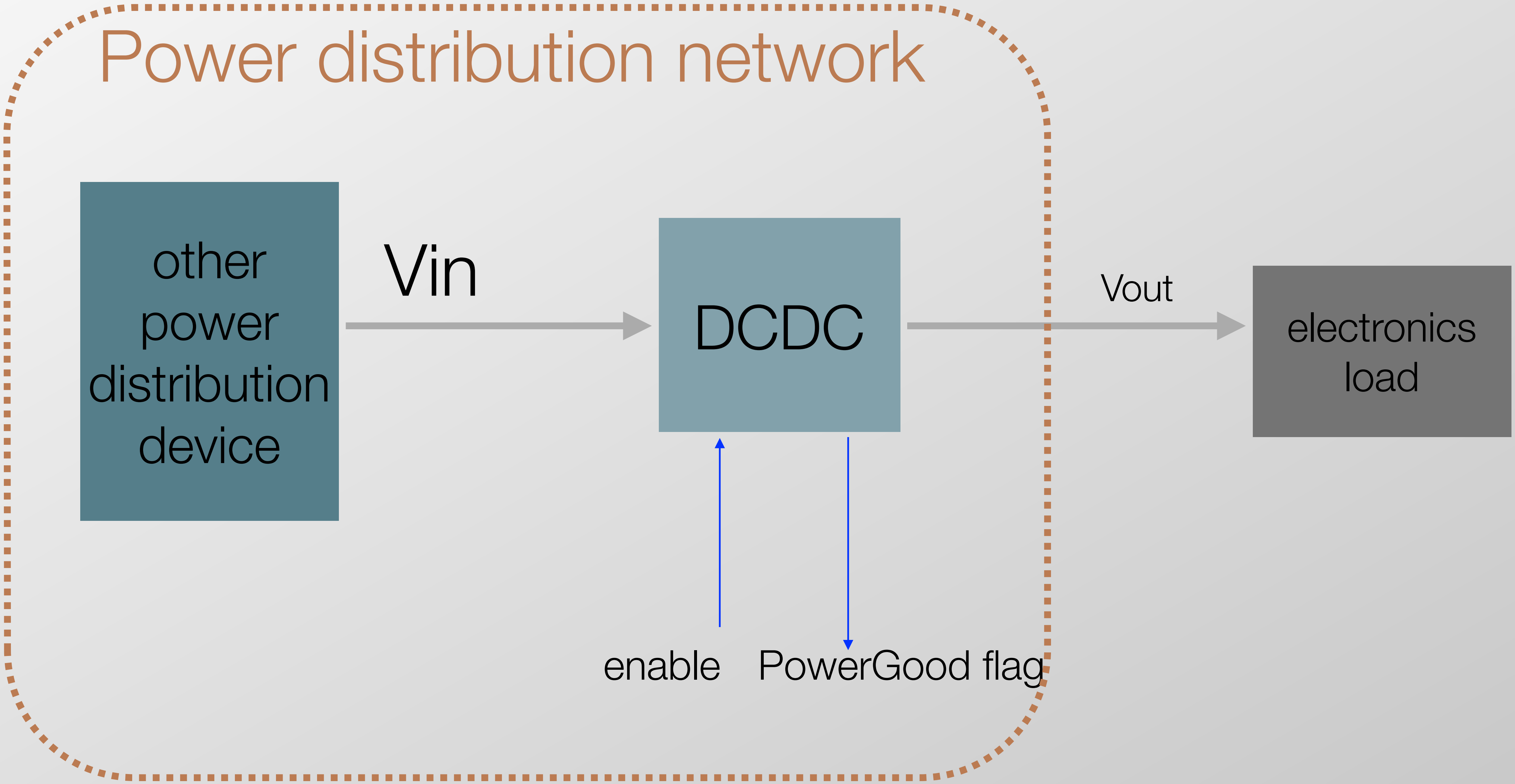
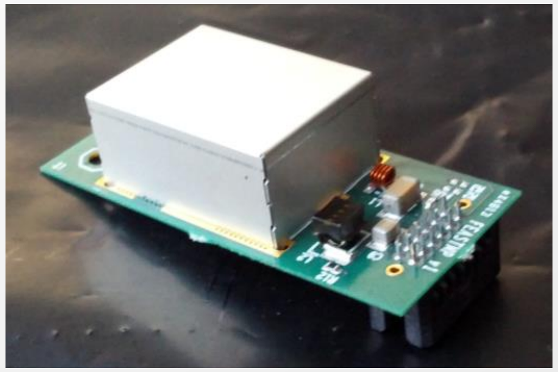
What is a POL DCDC converter



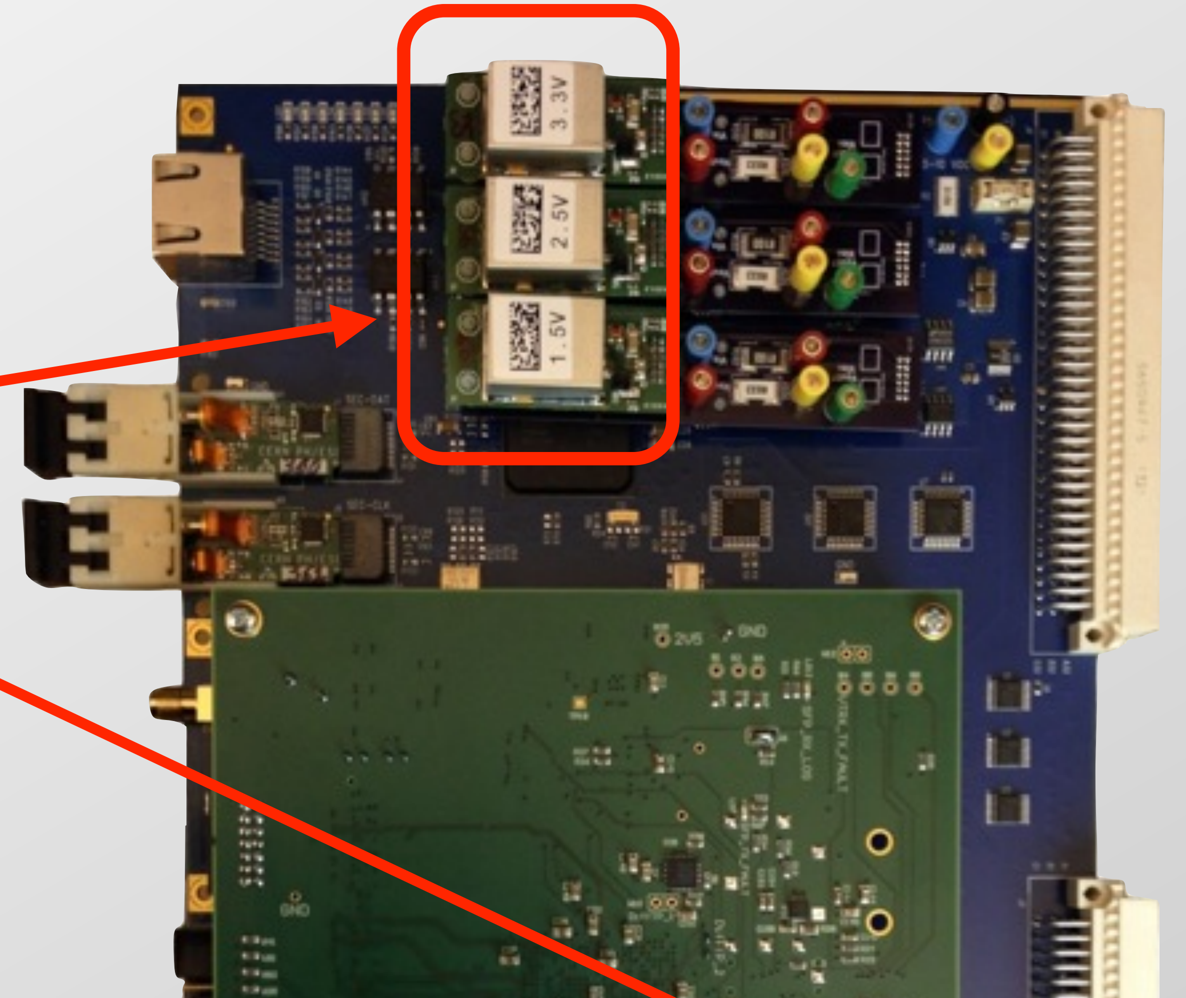
What is a POL DCDC converter

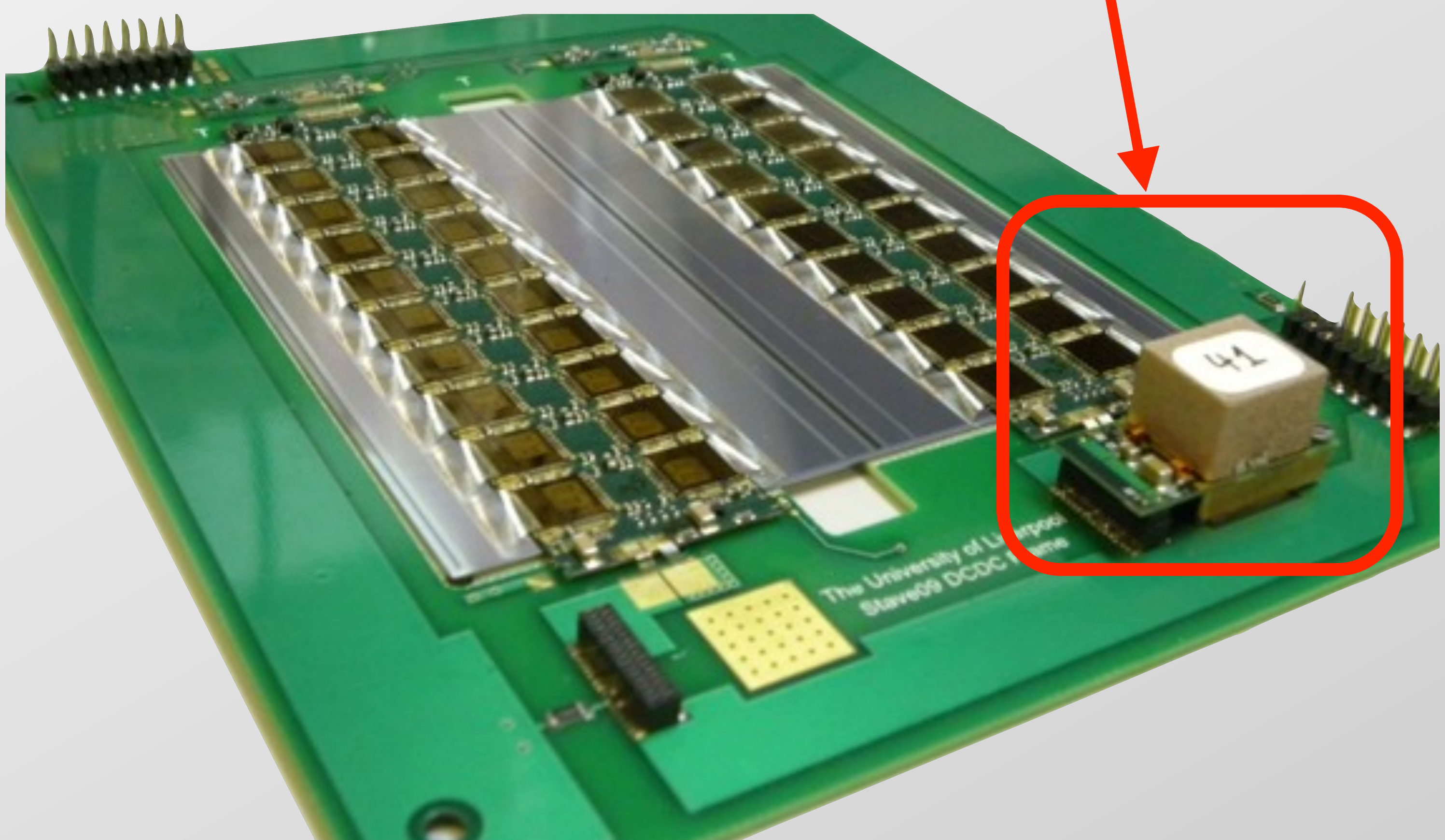


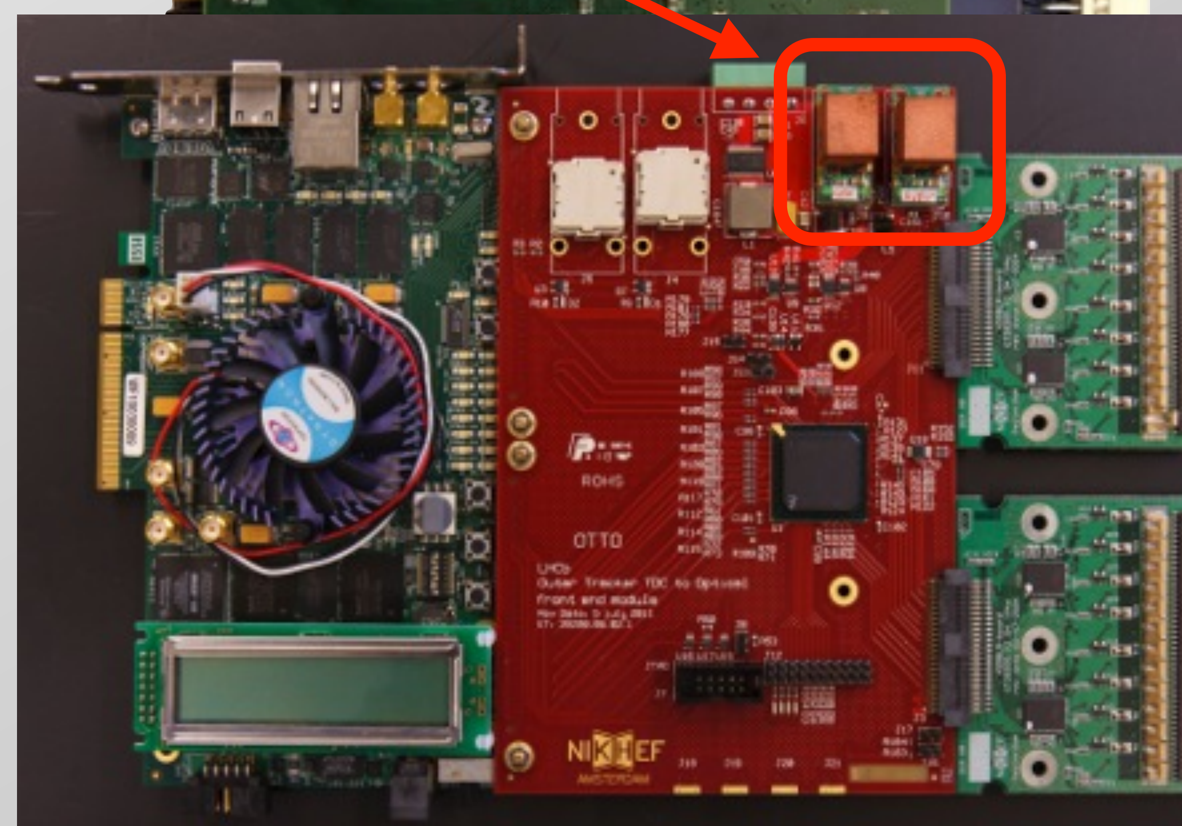
Complete plug-in DCDC module

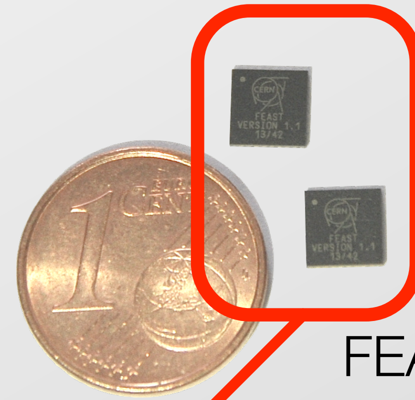


Radiation tolerant
Magnetic field tolerant to 40,000 Gauss
Low noise
Small volume and footprint





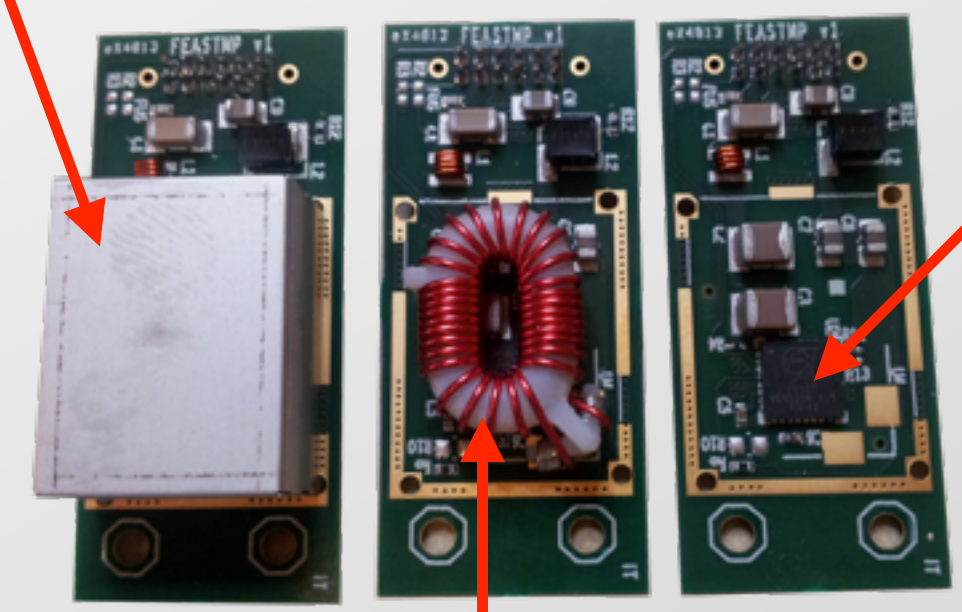




FEAST2 ASIC

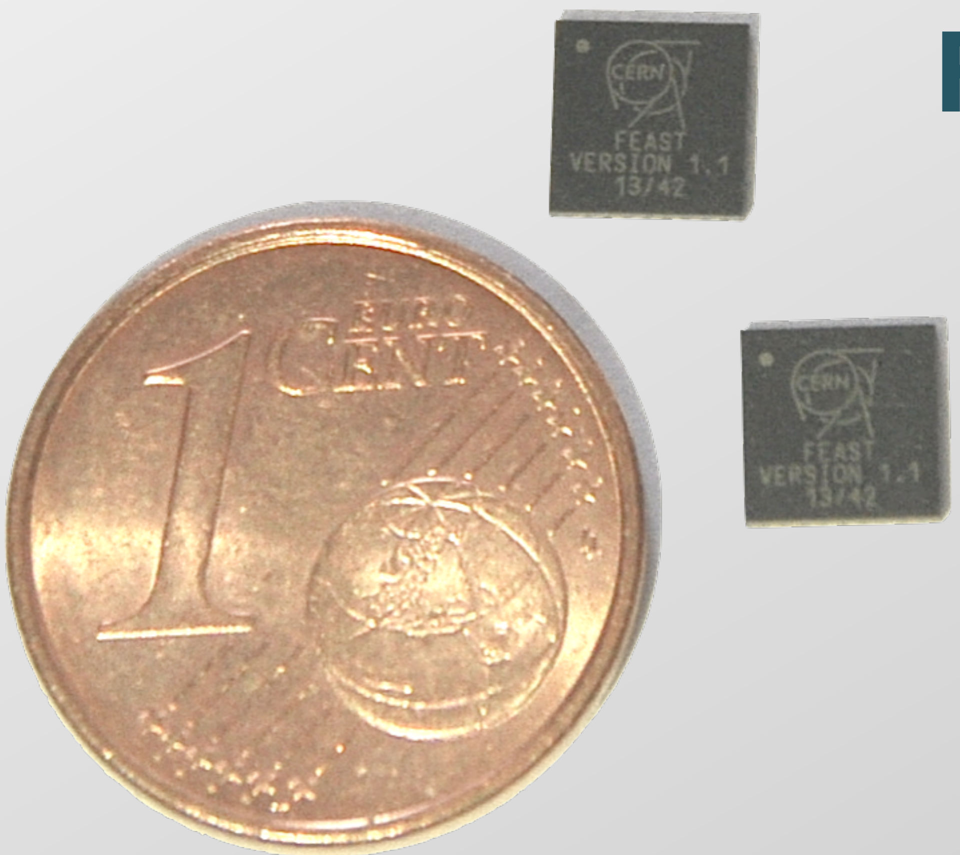
Cu shield

FEASTMP module



Custom air-core toroid inductor, 400nH

FEAST2



Outline: the FEAST2 ASIC

- Requirements
- Approach to achieve radiation tolerance
- Radiation test results

Requirements for the ASIC

- Constraints:
  - air-core inductor → switching frequency of 1-3MHz
  - 12V input voltage → adequate CMOS technology
  - radiation tolerant → adequate CMOS technology and design provisions
  - small → simple architecture, reduced number of passives (maximum integration) BUCK TOPOLOGY
- Relaxed constraints:
  - standby consumption → consumption of control circuits almost irrelevant

FEAST2 in a nutshell

	parameters	value	notes
Main electrical parameters	Input Voltage (V_{in})	5 V - 12 V	
	Output Voltage (V_{out})	0.6 V - 5 V	
	Output current (I_{out})	0 - 4 A	
	Maximum output power (P_{out})	10 W	Cooling required
	Programmable Switching frequency	1-3 MHz	Recommended: 1.8 MHz
	Inductor value	0.15 – 1.5 µH	Optimum: 400-500 nH
	Line regulation, 6 – 12 V range	5 mV	Measured at V_{out} = 1.2V and 2.5V at the output pins of the packaged ASIC
	Load regulation, 1 – 4 A range	5 mV	
Protection features	Over Current protection peak level	6 A	Corresponding to 4.8 A average for 1.8MHz, 400nH
	Over Temperature protection threshold	103 °C	Hysteresis of 40°C
	Under Voltage lockout	4.5 V	Minimum input voltage for operation
	Soft-Start duration	470 us	To limit inrush currents
Control	Enable (input) threshold	815 mV	Compatible with CMOS logic 1 – 3.3 V
	Range around nominal V_{out} for Pgood signal to be asserted	± 6.5%	Open drain output

Approach to achieve radiation tolerance

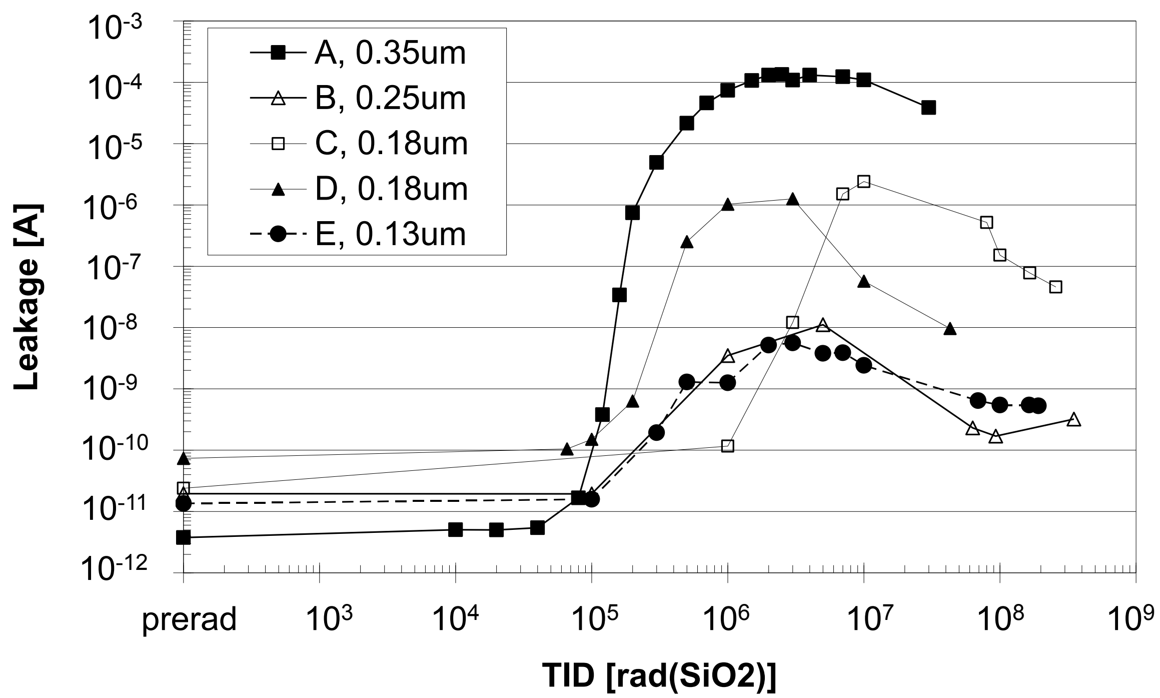
1. CMOS technology with high-voltage module (LDMOS) to be chosen after survey of available technologies and testing for the all radiation effects

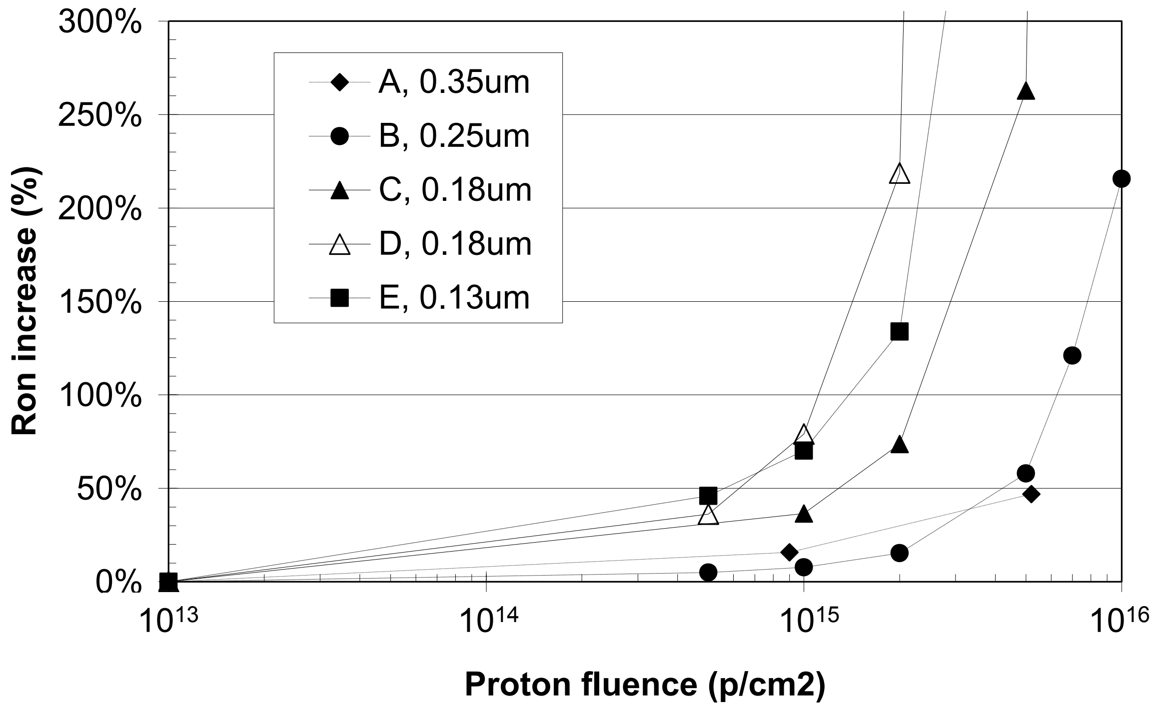
2. Systematic use of Hardness-By-Design (HBD) techniques for TID and SEEs

Technology choice

- 5 suitable technologies selected and radiation tested for TID and DD (technology node range: 0.35-0.13um)
  - ‘high voltage’ LDMOS were critical - no custom layout modification possible
  - the biggest concern came from DD (leakage current in LDMOS can be made irrelevant in the design of the ASIC)

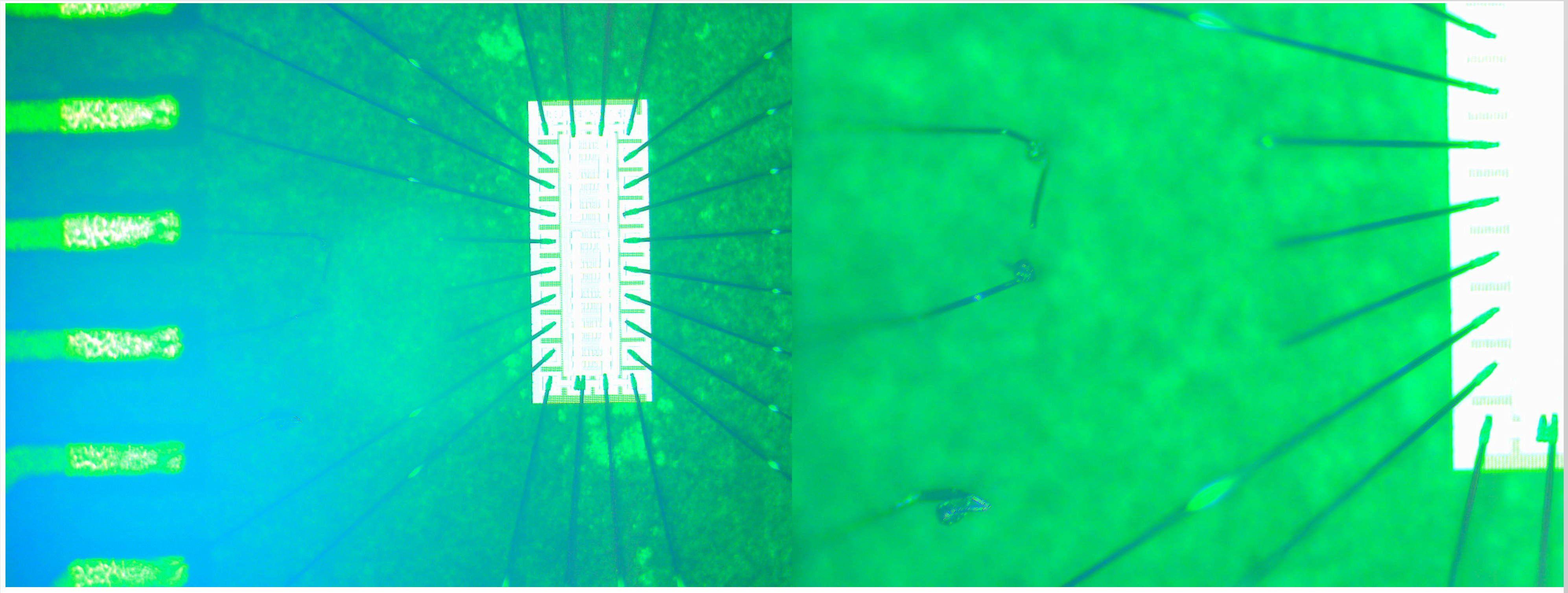
Example TID/DD radiation effects on LDMOS





Example of SEB sensitivity

- LDMOS from 3 technologies also tested for SEB/SEGR sensitivity
  - NMOS in one of them were sensitive to SEB below 10V and below a LET of $10 MeVcm^2mg^{-1}$



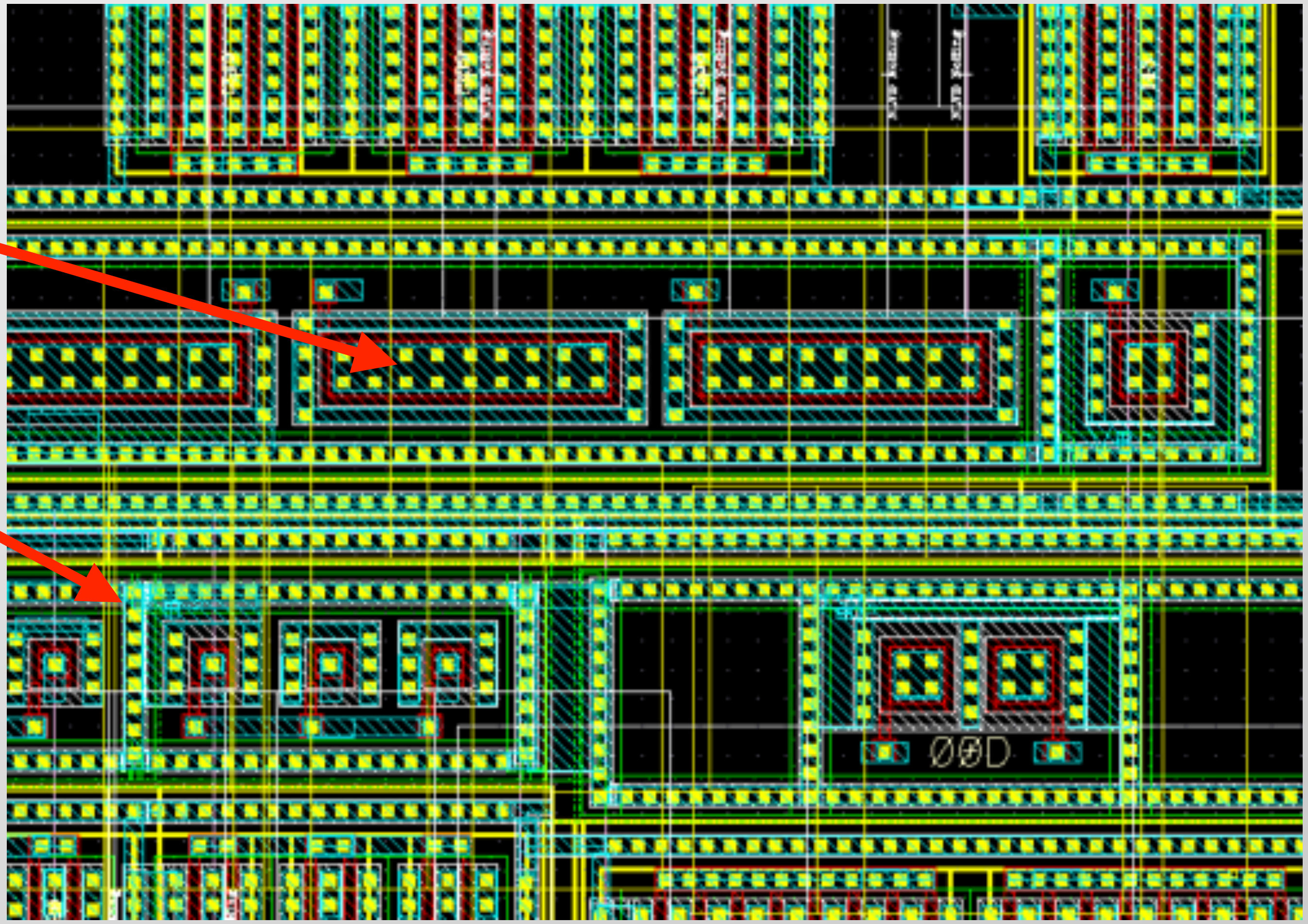
Molten wire-bonds after a SEB

Technology choice

- Combination of TID, DD and SEB/SEGR tests led to the choice of the technology:
  - 0.35um CMOS with high voltage module
    - it offers a good palette of devices for analog design
    - it features a large number of high-voltage transistors, and complete isolation from the substrate up to 80V
    - easily accessible for MPW, engineering and production runs, and reasonable cost

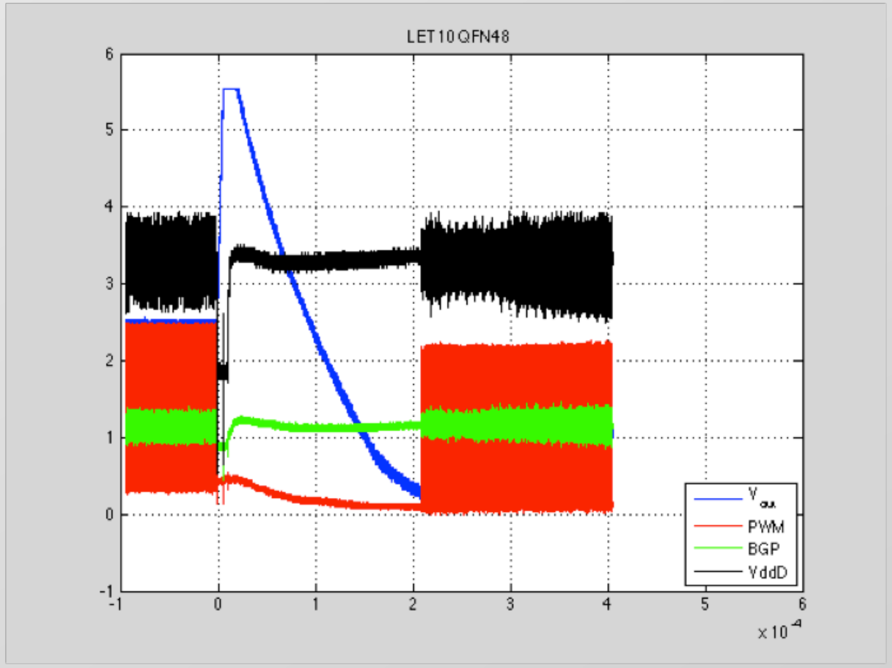
HBD techniques: TID

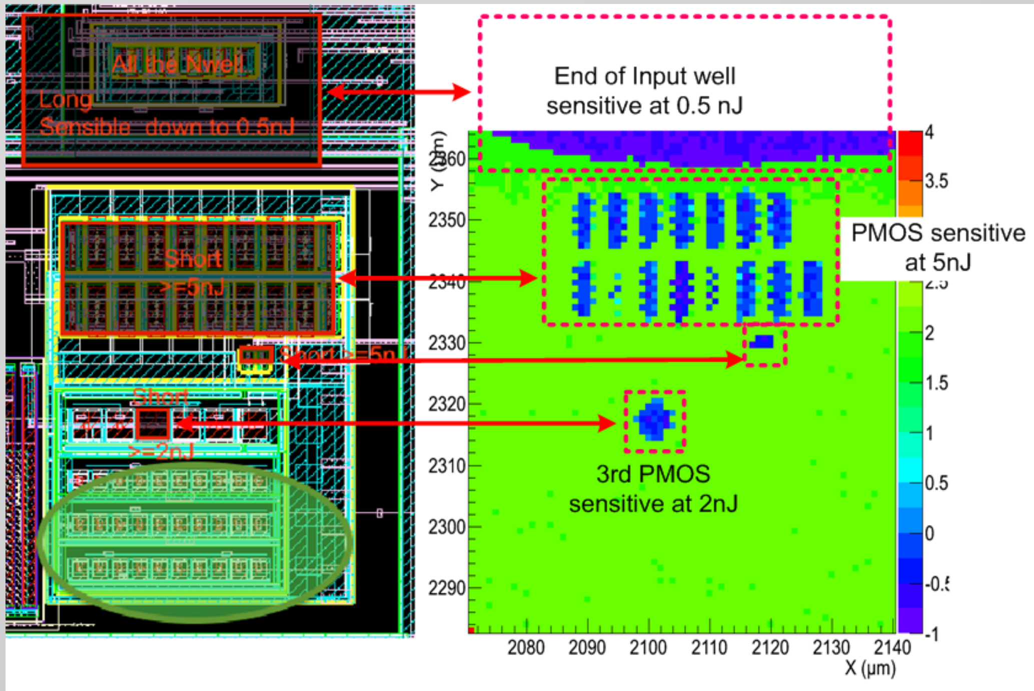
- Enclosed Layout Transistors (ELTs) for all NMOS
- Systematic use of p+ guard-rings
- TID tolerance OK as from first prototype integration



HBD techniques: SEE

- SEE testing performed on several generations of prototypes, with Heavy Ions and protons
  - removal of all sensitivities to SEEs was not easy. Some were difficult to foresee, for others Spice simulations were even misleading
    - observed consequences included the restart of the ASIC or the temporary loss of functionality with a large transient above the nominal output voltage
  - use of pulsed laser to fully map the sensitive points was a very precious tool (test done at Pulscan, Gradignan, France)
- Design techniques systematically used:
  - Triplication & voting used in most sensitive functions
  - Analog nodes protected by increase of currents and load capacitance

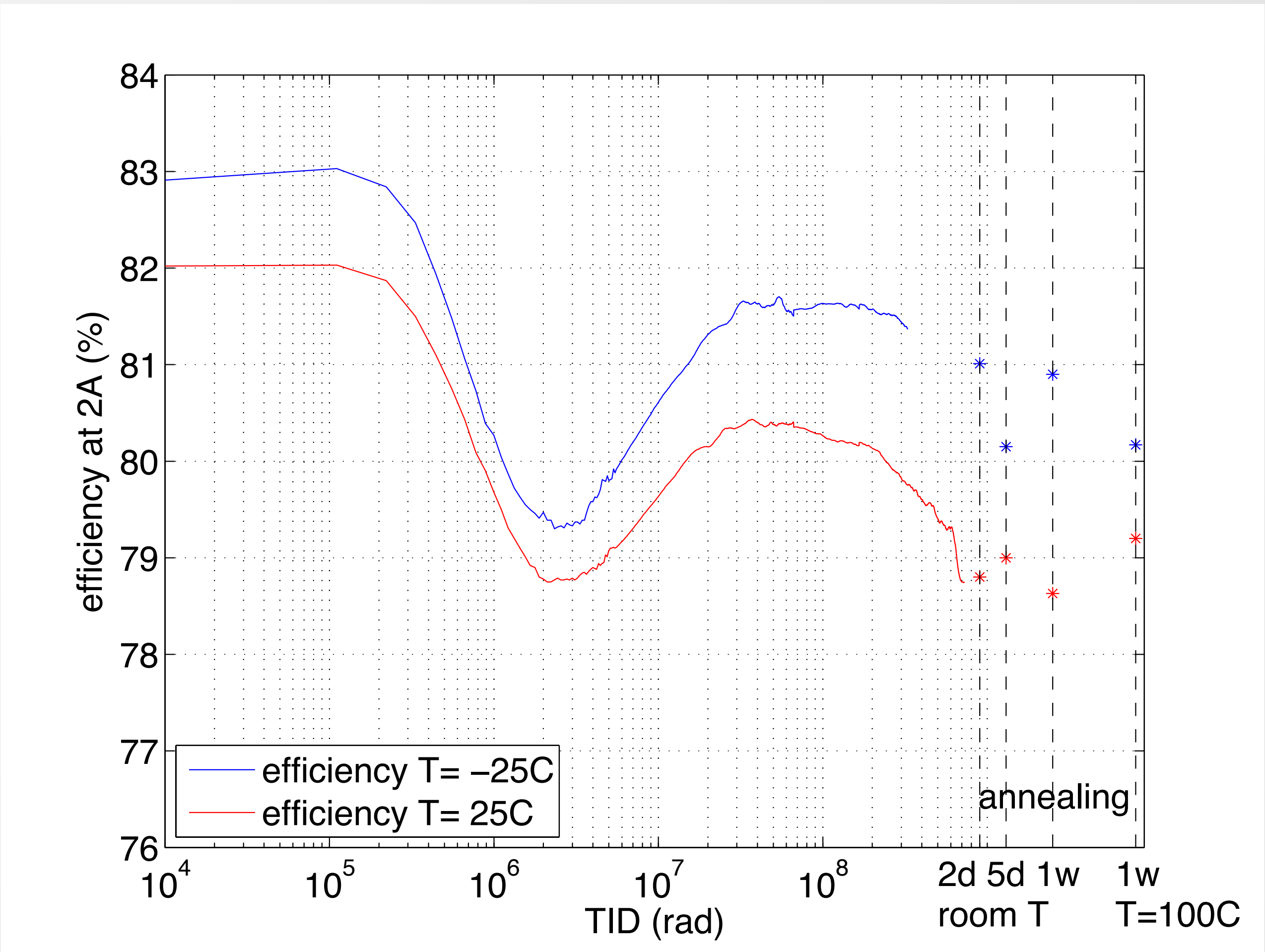


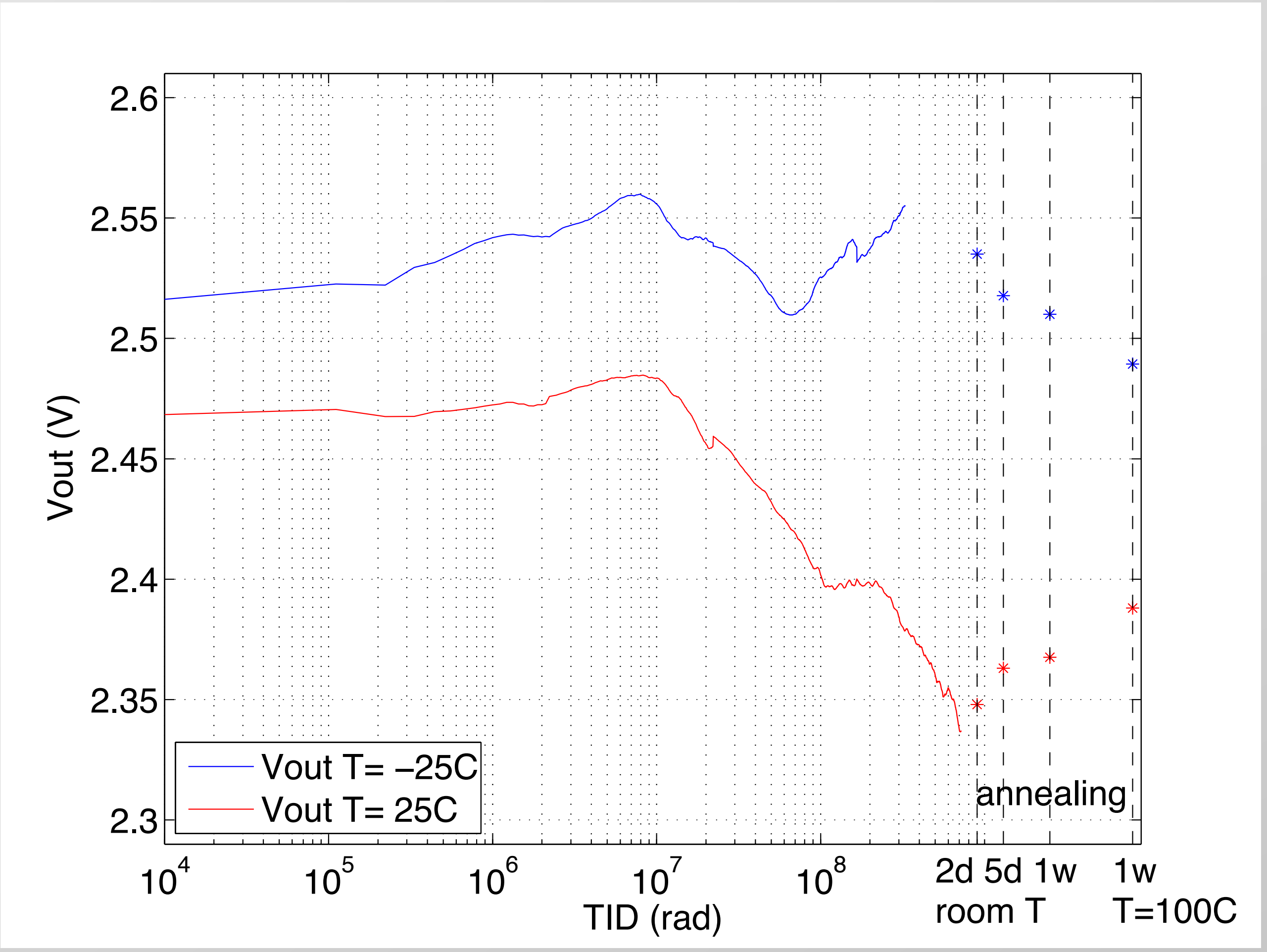


Radiation test results

Radiation test results: TID

- All irradiated samples were constantly functional during irradiation and annealing. Typical maximum TID reached in the test: 200-700Mrad





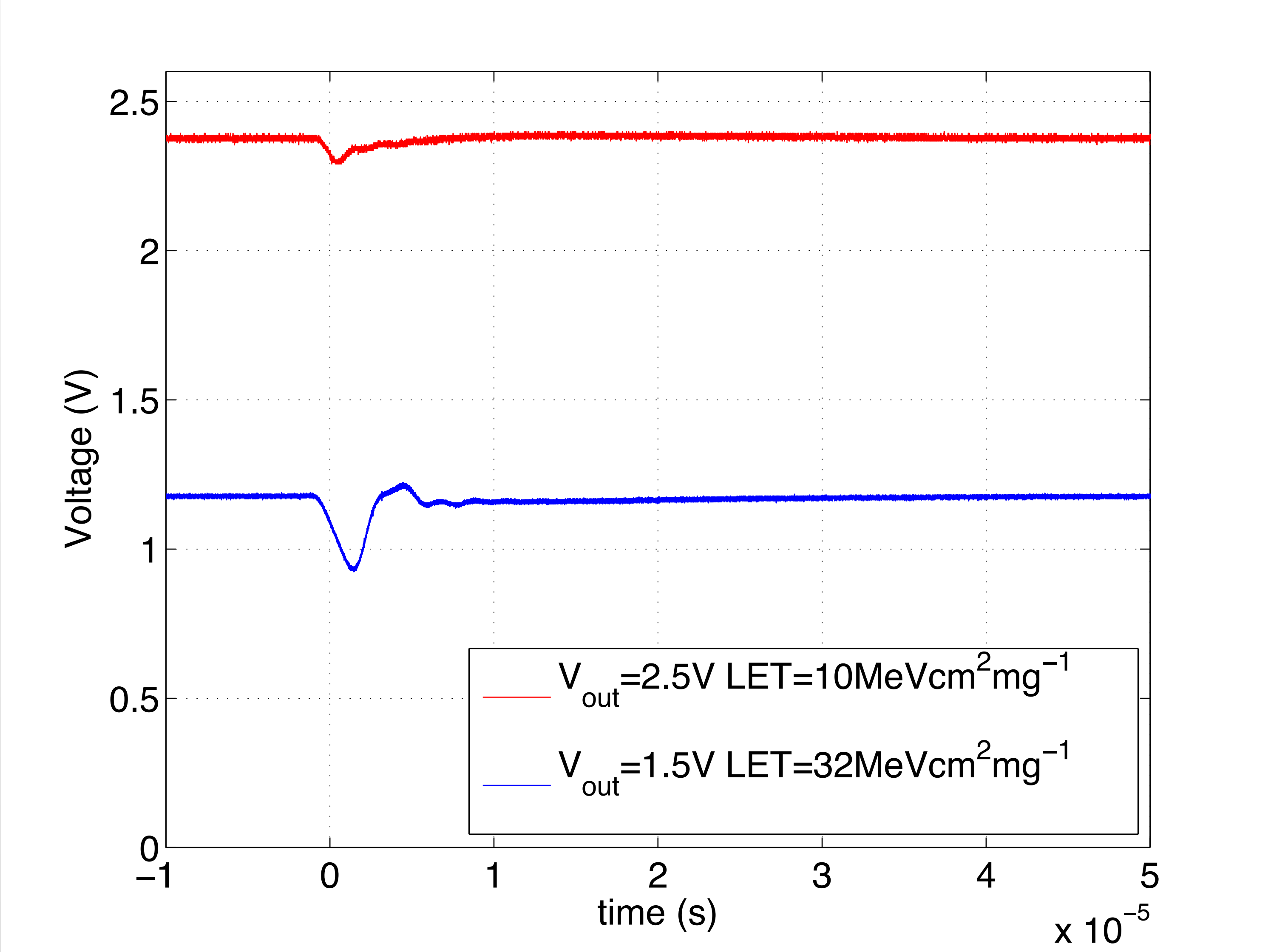
Radiation test results: DD

- Functionality is lost after an integrated flux of $5x10^{14}$ n/cm^2 (1MeV equivalent). This is due to damage to p-channel LDMOS transistors used in the on-chip linear voltage regulators
- The reference voltage generator shifts with the integrated flux, and as a consequence the output voltage increases. This starts to appear at the level of 10^{14} n/cm^2

Radiation test results: SEEs

- Tests performed with the ASIC regulating a voltage (1.5 or 2.5V typically) on a 1-2A load
- Heavy Ions in HIF, CRC, Louvain-la-Neuve
    - FEAST2 continuously provides regulated power to the load during the full test (total integrated flux = 126×10^6 ions/cm^2 at different LET up to 65MeVcm^{2}mg^{-1}). No reset, no SEFI observed
    - Short (<2-3us) and small (<20%) transients on the output are observed. These are irrelevant for the application

SETs observed during HI irradiation



Example SETs observed during HI irradiation. Amplitude increases with the LET of the incident particles, but it is always below 20% of the nominal Vout.

Typical duration is below 2us

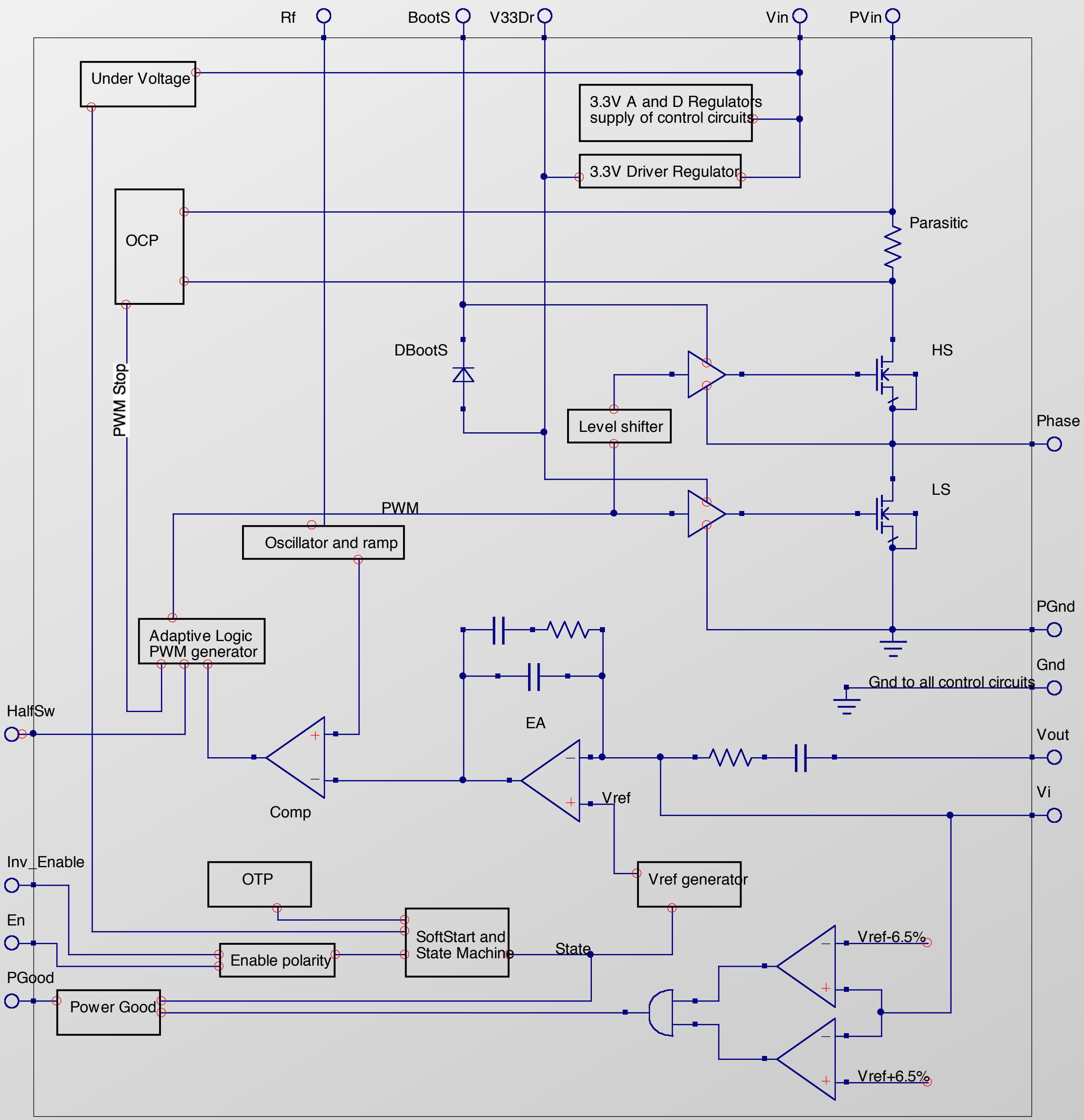
Summary

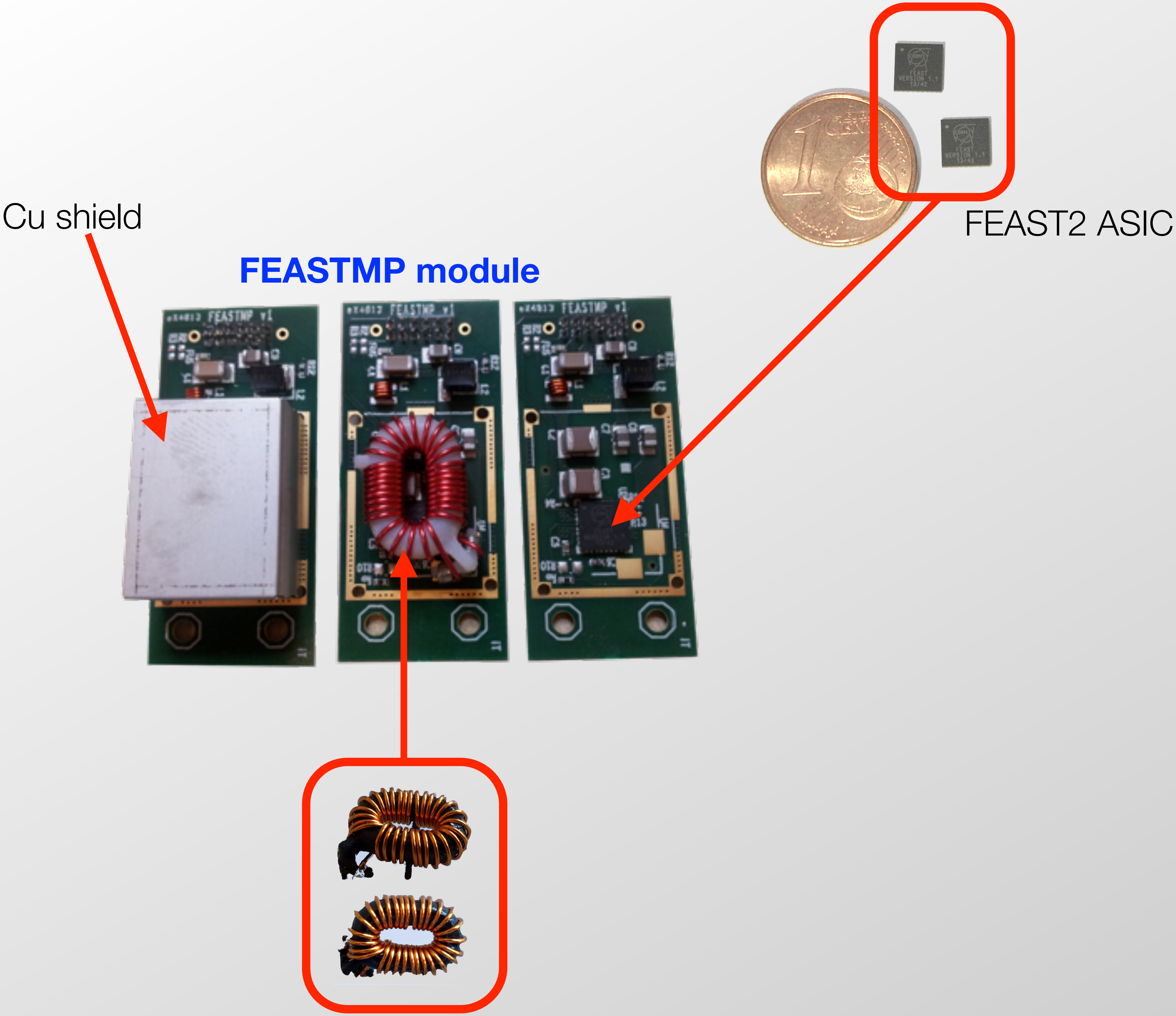
- FEAST2 is the final product of a long R&D effort. It is now qualified for all radiation effects
- The circuit is available in packaged form (QFN32) for LHC experimental groups, and as full plug-in module (FEASTMP). It is in production, with 1000 modules being tested at CERN this week
- Information and datasheet available in our public web page

http://project-dcdc.web.cern.ch

Spare Slides

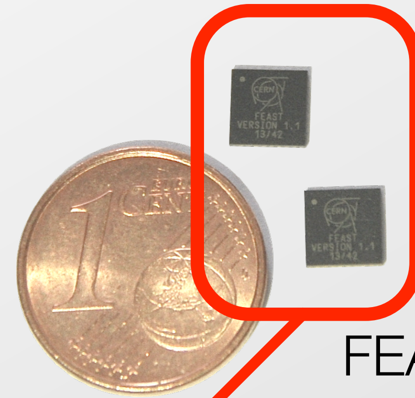
Architecture of FEAST2: buck converter





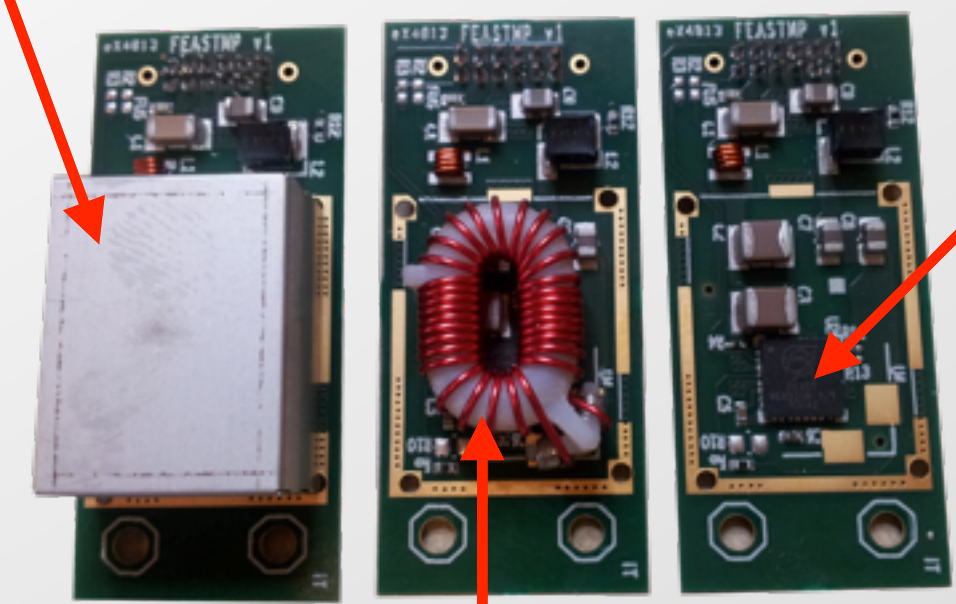
Custom air-core toroid inductor, 400nH

FEAST2 ASIC



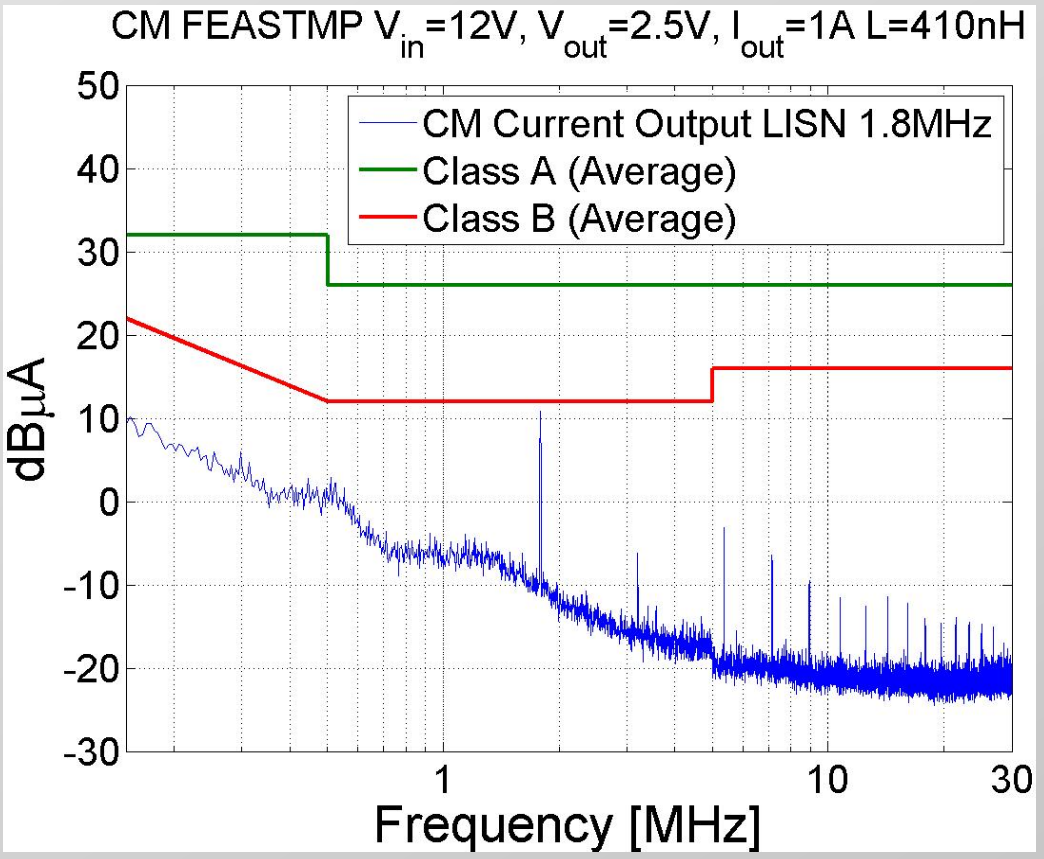
Cu shield

FEASTMP module



Custom air-core toroid inductor, 400nH

EMC: common mode current noise



SETs observed during HI irradiation

LET	Cross-section (cm^2) for SETs below the nominal V_{out}							
	2% bin		6% bin		10% bin		20% bin	
	σ (cm^2) and duration (μs)		σ (cm^2) and duration (μs)		σ (cm^2) and duration (μs)		σ (cm^2) and duration (μs)	
10.2	2.4×10^{-8}	(-)						
12.45	9.9×10^{-7}	(2.4)			9.8×10^{-7}	(-)		
14.42	6.5×10^{-6}	(4.1)	9.4×10^{-8}	(-)				
17.78			3.3×10^{-7}	(-)				
20.4			3.0×10^{-6}	(1.6)	1.3×10^{-6}	(1.4)		
24.9			6.6×10^{-6}	(1.4)	5.0×10^{-6}	(1.4)		
32.6			1.0×10^{-5}	(2.2)	8.0×10^{-6}	(1.5)	1.4E-07	(-)
46.1					9.0×10^{-6}	(1.5)		
65.2					8.1×10^{-6}	(1.5)		

LET	Cross-section (cm^2) for SETs above the nominal V_{out}							
	2% bin		6% bin		10% bin		20% bin	
	σ (cm^2) and duration (μs)		σ (cm^2) and duration (μs)		σ (cm^2) and duration (μs)		σ (cm^2) and duration (μs)	
10.2	3.4×10^{-7}	(0.5)	7.7×10^{-8}	(-)				
12.45	2.7×10^{-6}	(1.3)			1.4×10^{-7}	(-)		
14.42	5.4×10^{-7}	(1.0)	9.4×10^{-8}	(-)				
17.78			3.3×10^{-7}	(-)				
20.4			6.6×10^{-7}	(0.4)	1.4×10^{-7}	(-)		
24.9			3.3×10^{-7}	(0.5)	1.4×10^{-7}	(-)		
32.6			2.3×10^{-6}	(1.2)	1.4×10^{-7}	(-)		
46.1					1.4×10^{-7}	(-)		
65.2					1.4×10^{-7}	(0.4)		

Cross-section of SETs observed during heavy ion irradiation, catalogued in amplitude bins. Within each bin, only SETs above (or below) a fixed threshold are counted in the cross-section, and thresholds are expressed in percentages of the nominal Vout (example: 10% bin thresholds for Vout=2.5V are 2.25 and 2.75V). In parenthesis, the duration of the SET in μs. Blue figures are limit cross-sections: no SETs have been recorded. LETs are in $MeVcm^2mg^{-1}$ and have been obtained using the following ions: Ar at 0, 35, 45 and 55° incidence, Ni at 0 and 35° incidence and Kr at 0, 45 and 65° incidence.