A radiation-tolerant Point-Of-Load buck DC-DC converter ASIC

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Abstract

In view of application in upgraded particles detectors at its LHC accelerator, CERN has developed a radiation and magnetic-field tolerant DC-DC converter based on a radiation-tolerant ASIC, FEAST2. The circuit, designed in a selected commercial CMOS technology with high voltage capabilities, has been designed using 'Hardness-By-Design' (HBD) techniques and has been qualified with different radiation sources. Results of these tests are summarized evidencing that the achieved radiation tolerance satisfies the requirements of the LHC experiments in terms of Total Ionizing Dose (TID), Displacement Damage (DD) and Single Event Effects (SEE), making it also a possible good candidate for applications in Space. FEAST2 is now in production and CERN is using it to supply LHC experiments with full DC-DC plug-in modules.

I. INTRODUCTION

The particle detector systems at the CERN Large Hadron Collider (LHC) accelerator are preparing upgrades to improve their performance, in particular in view of the increased luminosity of the accelerator in the years to come. A serious limitation to the overall detector performance comes from the present distribution scheme, where the on-detector low-voltage electronics is directly powered from back-end supplies positioned tens of meters away, in the experimental cavern. The mass of the cables in such system is rather large, and it will not be possible to increase the supply current as required for improved detector performance without increasing the cables' mass further. This in turn is incompatible with the capacity of the detector to study the desired physics.

An obvious way of solving the problem is the distribution of power at higher voltage, with local (on-detector) conversion and regulation down to the voltage required by the front-end electronics. This task should be performed by a DC-DC converter installed in close proximity of the electronics, on the detector modules. The main specific requirements for this converter are radiation tolerance, compatibility with the magnetic field of (up to) 40,000 Gauss present in the central portion of the detector, low noise and small size (footprint, height) – coupled in some cases with extremely low mass. Since a converter satisfying the above requirements did not exist, CERN started an R&D activity to this purpose a few years ago.

To achieve the highest degree of integration, hence the smallest footprint and mass, we chose to go to an almost monolithic solution where all the active components are embedded in a single microcircuit, an Application Specific Integrated Circuit. The choice of the substrate technology for the design of the ASIC was not a simple affair: while the electrical specifications demanded the availability of high-voltage (above 12V) transistors for the power train and the on-chip regulators, at the same time the radiation tolerance requirements were hard to meet for such transistors. A long characterization phase, where 5 different candidate CMOS technologies were tested for radiation effects, was completed and eventually a suitable 0.35um process – commercially available for custom design – was selected [1].

The choice of the most appropriate converter architecture was driven by efficiency and mass/footprint considerations. The efficiency in principle achievable by different architectures in some of the candidate CMOS technologies was evaluated, and weighted over the number of passive components each of them required – with particular emphasis on the largest and more massive of them, the element storing the energy during switching (inductor or capacitor). At the end, the simplest architecture was chosen: the buck step-down converter that only uses one inductor and a few capacitors [2].

In parallel to the ASIC development, which required several prototyping cycles, extensive effort was dedicated to the integration of the circuit in a compact module reaching the Electromagnetic Compatibility (EMC) performance adequate for installation of a full DC-DC converter in very close proximity to the sensitive read-out electronics of the particle detectors [3]. The aim was the development of a unique and well-characterized plug-in module that would satisfy the requirements (electrical, footprint, height, radiation tolerance) of all detector systems.

After several years of R&D activity, the development has now reached full maturity and both the ASIC and the module are entering series production. The datasheet for both can be found in the public web page of the CERN DC-DC development project [4]. This paper describes the main features of the ASIC and details its radiation tolerance characterization.

II. FEAST2 FEATURES

FEAST2 is the production-grade buck DC-DC ASIC developed within the framework described above. The circuit has a size of 2.8 x 2.88 mm^2, and is manufactured in a commercial 0.35um CMOS process offering LDMOS transistors rated at 12V and above (different transistors are available with different V_{ds} capability). This process was developed mainly for automotive applications and offers a

wide palette of high-voltage devices, together with isolation from the substrate via wells that can also stand high voltage.

The ASIC integrates both the power train and all required control circuits, including the bootstrap diode for the driving of the High-Side power transistor, several linear regulators to derive the on-chip supply rails from the unique 10-12V input voltage, and reference voltage and current generators.

Being targeted for application in a radiation environment, the design makes extensive use of HBD for both TID and SEE tolerance. For TID, n-channel transistors are laid out as enclosed devices to prevent source-drain leakage currents – a design that is often called 'Enclosed Layout Transistors' (ELT) [5]. Also, p+ guardrings are systematically surrounding n+ wells and diffusions at different potential to cut any inter-device leakage path. For SEE hardening, several techniques are used in different circuit blocks. In some cases transistors and currents have been over-sized to increase the charge needed to upset the circuit's node. This same effect was reached in other cases by adding extra capacitance in the form of either metal-metal or MOS capacitors. Equivalent RC filters are used in 'slow' nodes to prevent the propagation of fast glitches (SET). Finally, essential control circuits whose upset could potentially have large impact on the full converter have been triplicated and their output voted.

Electrical specifications of FEAST2 include input voltage up to 12V, output voltage in the range of 0.6-5V, continuous output current up to 4A, maximum output power of 10W. The circuit is optimized to use an about 400-450nH inductor, hence it switches at a frequency of the order of 1-3MHz – the best compromise performance for efficiency and EMC being around 1.8MHz. The high frequency (150kHz) of the feedback loop, whose elements are almost entirely integrated on-chip, ensures a rapid response of the converter in case of load and line transients.

FEAST2 offers a number of safety features. To prevent excessive current in-rush at start-up, a Soft-Start procedure is executed every time the converter is enabled: the output voltage rises gently to the nominal value in about 470us. An Under-Voltage Lock-Out system (UVLO) monitors the input voltage and only allows the circuit to be functional in the presence of a sufficiently large input voltage (about 5V). The output current is monitored on a cycle-by-cycle basis: whenever the peak current during each switching cycle exceeds a pre-determined level the PWM signal keeping the High Side power transistor turned on is interrupted. This is part of the Over-Current Protection system (OCP), and in the event of persistent excessive current the converter practically enters a constant current supply mode with a decrease of the output voltage provided to the load. The junction temperature of the ASIC is monitored by an Over-Temperature Protection system (OTP) that disables the converter whenever it exceeds about 100°C.

In terms of external control features, FEAST2 can be turned on/off via a dedicated enable pad compatible with any CMOS logic level between 1.0 and 3.3V. A Power Good signal is provided to the external world via a dedicated pad, which is connected internally to an open-drain NMOS transistor. With a pull-up connection to the appropriate voltage, this pad can provide valid CMOS logic levels up to 5V. The Power Good is normally asserted (logic 1) when the converter is correctly regulating the output voltage at the nominal value. If the output voltage exits a regulation window of about ±6.5%, or if the OTP detects excessive temperature, the Power Good is negated (logic 0).

FEAST2 is packaged in plastic QFN32 packages with exposed thermal pad to ensure sufficient chip cooling at high output power levels.

III. IRRADIATION RESULTS

The radiation tolerance qualification of the ASIC required the measurement of samples in different radiation environments. Since the circuit needed several prototyping cycles before maturity, each prototype was in fact fully characterized to reveal weaknesses to be corrected in the next iteration. The results reported below refer hence not only to FEAST2, the production-ready version of the converter, but also to its immediate predecessor FEAST. The latter was almost meeting all specifications, but for the sensitivity to SEEs. Since the modifications required to improve the SEE response were minor and most of the circuit was unchanged, irradiation results for TID and DD obtained on FEAST samples are well representative of the final FEAST2 as well.

For TID the X-ray irradiation system installed within the CERN PH-ESE group was used. This system has characteristics very similar to the most widespread Aracor irradiation system [6] and can reach a dose rate of about 9 Mrad(SiO$_2$)/hour. Given the used radiation source for TID, all doses will be expressed in SiO$_2$ in the rest of the paper. For displacement damage, tests were run on different prototypes at either the CERN PS IRRAD1 facility, which provide an intense beam of 23 GeV/c protons, or at the Triga nuclear reactor of the Jozen Stefan Institute (JSI) in Ljubljana, Slovenia. Finally, the irradiation campaigns to study the sensitivity to SEEs took place at the Heavy Ion irradiation facility of the Cyclotron Resource Centre of Louvain-la-Neuve, Belgium.

A. Total Ionizing Dose

Several samples of FEAST2 were exposed to X-rays at either 25 or -30°C. The latter temperature has been chosen to minimize the annealing of defects during irradiation, and because it is the temperature foreseen for the cooling system in some of the detectors planning to use the DC-DC converters. The circuit was mounted on a full DC-DC module and fully functional during irradiation and subsequent annealing: an output voltage of 2.5V was selected for the converters that were providing 1 or 2A to an external active load. Samples were irradiated up to a TID of 200 to 720Mrad and were constantly working during both irradiation and annealing. Testing was pushed to these extreme levels, well above any requirement for Space application, because some of the LHC detectors requiring DC-DC conversion will be exposed to doses of 200Mrad or more, so it was interesting to see if the ASIC had good margin for correct functionality at those levels.

All the main thresholds for the protection systems (UVLO, OCP, OTP) were measured and found not to shift significantly during the full test. The efficiency is rather

marginally affected by the irradiation (Figure 1), its variation being directly related to the radiation-induced leakage current and the increase of the on-resistance in the NMOS transistors of the power train. The peaked decrease of the efficiency, with minimum at around 2Mrad, is determined by the leakage current in the NMOS: some current finds its way from Vin to ground and determines additional losses. The leakage is the same whichever the load current, hence the efficiency drop it induces actually decreases considerably with the output load (it is almost negligible at 3 and 4A). It should be noted also that this leakage current has been found to anneal very quickly even at cryogenic temperature, therefore the efficiency drop in the application, at much lower dose rate, is expected to be considerably milder. To support this hypothesis, a sample has been irradiated at the high dose rate usual of our experiments up to 1.66Mrad (peak of the degradation) at -30ºC. With irradiation stopped, the sample was kept at the same T for 20 hours: the efficiency that had dropped by almost 4% during irradiation increased considerably due to the annealing at low T and was only 1% below the pre-rad value after 20 hours. At TID levels above 300Mrad, the gentle decrease of efficiency is instead traceable to a real degradation of the on-resistance of the power transistors. This is not expected to be subject to anneal (actually, because of the latent evolution of the interface states negatively affecting carriers mobility in the channel, annealing might even induce a further decrease of efficiency).
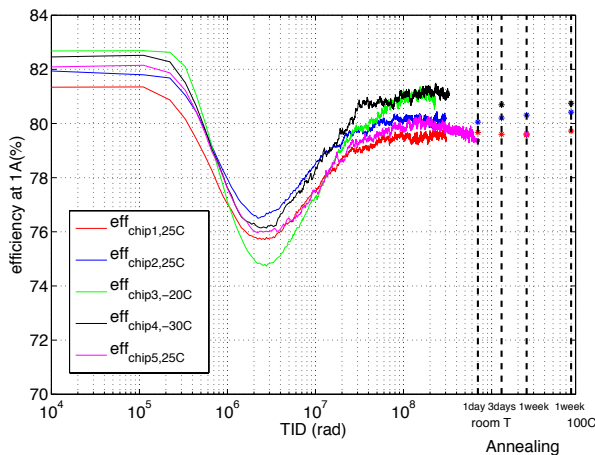

Figure 1: Efficiency evolution with TID for different FEAST2 samples at either 25 or -30ºC and for 1A load current. The drop up to about 2Mrad is due to leakage current independent on the load current: this drop is hence much reduced at larger loads.

Regulation properties like line and load regulation have been measured: line regulation is practically unaffected by even the highest TID levels, while load regulation tend to worsen slightly above some 300Mrad.

The bandgap reference voltage generator integrated in FEAST2 has very good TID performance, and as a consequence the variation of the regulated output voltage with TID is limited to below some 50mV after 200Mrad when regulating 2.5V, which represent a variation of about 2%. The sample irradiated to 720Mrad showed a further decrease of about 3%, for a total shift of 5%. Annealing both at room

temperature and 100ºC does not help bringing the output voltage back to its pre-rad value.

B. Displacement Damage

At the time of writing, samples of FEAST2 are being exposed to neutrons at the JSI reactor. However, results of irradiation of previous prototypes (such as FEAST) are available and are well representative of the displacement damage effects in the production-ready ASIC. There are two relevant effects from displacement damage, which end up being the real limiting factor in the overall radiation tolerance of the converter circuit for HEP applications.

The first and most dramatic effect happens in the on-chip linear regulators providing the 3.3V for the analogue and digital control circuitry, as well as to the drivers of the gate of the power transistors. These regulators make use of p-channel LDMOS transistors rated at 80V in V_{ds}, and these transistors are very sensitive to displacement damage. Their current-voltage characteristics are degraded considerably already at an integrated flux of $1x10^{14}$ n/cm^2 (this and all successive fluences are expressed as 1-MeV neutron equivalent). Above $5x10^{14}$ n/cm^2 their current capability is so small that the regulators fail providing the 3.3V voltage to the power rails, and the full converter stops working. Failure happens between 5 and $7x10^{14}$ n/cm^2 since samples are functional at the first and failing at the second fluence.

The second effect is a sensible increase of the reference voltage from the bandgap voltage generator. This shift can be as large as 10% at $5x10^{14}$ n/cm^2, with a proportional increase of the regulated output voltage, and can be traced to the diodes used as basic elements to generate the reference voltage. A precise relationship between neutron fluence and reference voltage, with particular attention to levels below $3x10^{14}$ n/cm^2, will be obtained from the measurements of the FEAST2 samples currently irradiated at JSI.

C. Single Event Effects

Reaching the required level of tolerance to Single Event Effects was not simple. The first and foremost requirement for the circuit is the absence of destructive events. If latch-up can be avoided with the used HBD approach, where guardrings are systematically used to separate all wells, other destructive events can threaten high voltage technologies – the most notable of which for 12V-compliant devices being Single Event Burnout (SEB). While this destructive event was known to affect transistors and diodes rated above some 100V, recent work has shown that some LDMOS transistors can be sensitive to SEB at applied V_{ds} below 10V [7]. In our work, one of the candidate technologies for the development was discarded only because n-channel LDMOS transistor were found to be prone to SEB at even 8V when irradiated with Heavy Ions of LET below 10MeVcm^{2}mg^{-1} – and with a very large cross-section. Both n-and p-channel LDMOS in the chosen 0.35um technology were instead measured insensitive to this event in dedicated tests run up to an LET of 32MeVcm^{2}mg^{-1} (at normal incidence).

Heavy Ion irradiation of different prototypes of the converter ASIC confirmed the absence of destructive events – even at 60 degrees tilted irradiations for an equivalent LET of 64MeVcm^{2}mg^{-1}. However, different mechanisms for

sensitivity to SET (transients) were found where the circuit would go into a hard-wired reset procedure. In some cases, the circuit could also be stuck for tens of us in a state where the HS power transistor was constantly turned on, with an increase of the output voltage well above nominal. These mechanisms needed to be understood and their origin removed. A powerful tool in that respect was provided by pulsed laser tests at the Pulscan facility in Gradignan (France). Sample ASICs were scanned with the a narrow (1um in diameter) pulsed laser beam, the laser impinging from the back of the silicon die to avoid the shading from the 5 layers of metallization used in the circuit. At the same time, the output voltage and other critical signals were monitored for any sign of sensitivity. In this way, and by changing the laser power, it was possible to map the sensitive points in the full control circuitry and also have a relative indication of their sensitivity. This study was done on the FEAST prototype and guided the design of the revised FEAST2 version of the converter.

Irradiation of FEAST2 with heavy ions confirmed that the SEE tolerance goal has been reached. Exposed to a total integrated flux of 126×10^6 ions of increasing LET at different angles, up to an equivalent LET of $64 \text{MeVcm}^2\text{mg}^{-1}$, the ASIC constantly provided 2.5V (or 1.2V) to an external 1A load: no destructive event or reset (or other large transient at the output) was ever observed. SETs do in fact appear at the output of the converter, but with small amplitude and short duration. These will not affect the load in any application, however they have been carefully recorded by the measurement system. Fast comparators monitored the output voltage, their reference voltage being set above or below the nominal. Whenever the converter's output exceeded any of the pre-determined thresholds, the system recorded the event and measured its time duration. It was hence possible to measure the cross-section for SETs and catalogue them for their percentage amplitude with respect to the nominal (2%, 6%, 10% and 20% thresholds were used). This yield curves as the one shown in Figure 2 for negative SETs (below nominal). Negative SETs were more numerous and larger in value and time duration. It should be pointed out that the time duration of the events (time over threshold) gets shorter for larger amplitude: 2-4us for events with 2% thresholds, 1.5-2us for events with 6%, 1-1.5us for events with 10%. Only one event was recorded during the full test where the threshold was set at 20%, with the highest LET ion at normal incidence, and with duration of only 120ns. A typical SET at the output of the converter is shown in Figure 3.

The HI results above can be interpreted in view of using FEAST2 in the LHC detector systems. Since the LHC particle radiation environment relevant to SEEs is composed only by charged and neutral hadrons, only the HI results for LETs below $15 \text{MeVcm}^2\text{mg}^{-1}$ are relevant (this is the maximum LET from recoils in nuclear interactions of hadrons in silicon). Therefore, SETs will be limited to below 6% of the nominal voltage – only the 2% threshold was exceeded in the HI irradiation test below that LET.
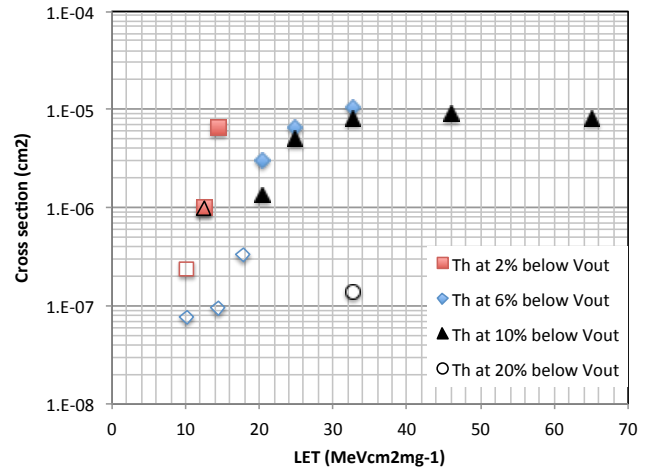

Figure 2: Measured cross-section for SETs at the output of the FEAST2 converter during Heavy Ion irradiation. In this case, the cross-section is for 'negative' glitches (below the nominal V_{out} of 2.5V). Empty points indicate 'limit' cross-sections where no errors were recorded (1 error is used to compute the limit value).
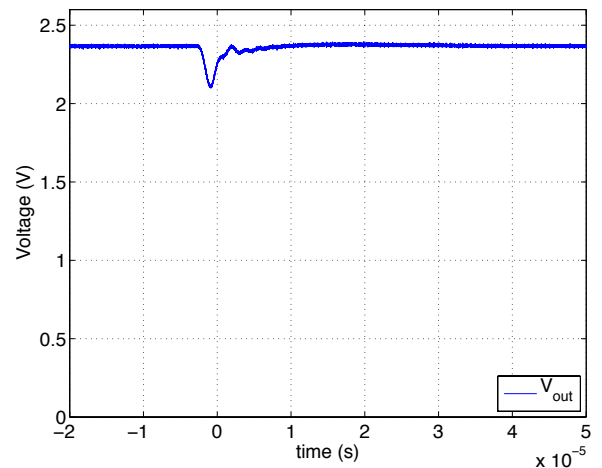

Figure 3: Typical SET at the output of the converter recorded by the oscilloscope constantly monitoring the V_{out} during the Heavy Ion irradiation test. In this case, the ion had an LET of $32 \text{ MeVcm}^2\text{mg}^{-1}$ and was impinging on the ASIC at normal incidence.

IV. CONCLUSION

The CERN R&D project aimed at developing a radiation and magnetic field tolerant DC-DC converter for upgraded LHC detector systems has reached maturity, and CERN is moving to the production phase. FEAST2 is the production-grade ASIC that satisfies electrical and radiation tolerance specifications. Radiation qualification has been done for TID, DD and SEEs using different radiation sources. Functionality has been verified up to more than 700Mrad for TID, up to 5×10^{14} n/cm^2 for DD, and during HI irradiation up to an equivalent LET of $64 \text{MeVcm}^2\text{mg}^{-1}$. SET sensitivity with HI is limited to short (1-4us) and small (below 20% of the nominal in amplitude) glitches at the converter output. Packaged in plastic compact qfn32 packages, the ASIC is used in full DC-DC plug-in modules ready to be integrated in the electronic systems of the LHC detectors. These modules also use a

custom-developed toroid air-core inductor of 400nH that can operate in magnetic fields in excess of 40,000 Gauss. Thanks to an optimized module layout and choice of the passive components, these modules satisfy even the Class B requirements of the CISPR11 standard for EMC, and can hence be used in very close proximity to the sensitive particle detectors and readout electronics. CERN will very likely provide more than 20,000 such modules to the LHC experiments in the next few years.

V. REFERENCES

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