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A radiation-tolerant Point-of-Load buck DCDC converter ASIC

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The High Energy Physics Experiments at the Large Hadron Collider (LHC), the most powerful particle accelerator installed at CERN in Geneva, Switzerland, are in an exciting data taking phase but are also preparing upgrades to improve their performance. Their complex assemblies of detector systems make extensive use of electronics components located in a severe radiation environment and in a magnetic field of up to 40,000 Gauss. Power distribution is a real challenge: other than radiation and magnetic field tolerant, the distribution network components have to be small and light (low mass and footprint) and have EMC performance sufficient not to affect the low noise of the sensitive read-out electronics. For this application, CERN has developed a custom Point-of-Load (POL) DCDC converter satisfying all the above requirements.

The POL converter is a single-phase buck topology built around an ASIC designed by CERN in a commercial CMOS technology with high voltage capabilities. This circuit, named FEAST2, embeds on the same 2.8 x 2.88 mm2 silicon both the power switches, bootstrap diode and the control circuitry. Capable of operating from an input voltage of 5 to 12V, it has a selectable output voltage range between 0.6 and 5V and can provide up to 4A of output current (within the limit of 10W output power). The switching frequency can be selected in the range of 1-3MHz, the best compromise between efficiency and EMC performance being reached at around 1.8MHz. The bandwidth of the feedback loop, at 150kHz, is sufficiently large to ensure excellent transient regulation. The high switching frequency makes it compatible with the use of small air-core inductors of 200-400nH, which are required to enable its use in the 40,000 Gauss magnetic field of the LHC experiments.

In terms of protection features, the circuit integrates a cycle-by-cycle Over-Current Protection (OCP) and an Over-Temperature Protection (OTP), as well as Under-Voltage Lock-Out (UVLO) preventing the converter to turn on in the absence of a sufficient input voltage. Communication with the system embedding the DCDC is ensured by an Enable input (to turn it on/off) and a PowerGood (PG) output flag, both signals being compatible with CMOS logic levels up to 3.3V. The PG is asserted when the output voltage is in the range of +-6.5% around the nominal.

Radiation tolerance is achieved with a careful choice of the used CMOS technology (5 candidate processes were probed for different radiation effects) and with the systematic use of hardness-by-design techniques. Enclosed Layout Transistors (ELTs) have been employed to limit Total Ionising Dose (TID) effects in all the control electronics, while adequate sizing, triplication and other appropriate redundancy mitigate the impact of Single Event Effects (SEE). As a result, the circuit has been qualified for TID levels in excess of 200Mrad(SiO2) and for displacement damage up to 5-8e14 n/cm2 (1MeV-equivalent neutrons). SEE qualification has been performed at the high penetration heavy ion beam of CRC, Louvain-la-Neuve, up to an effective LET of 65 MeVcm2mg-1. No destructive events have been ever observed on any of the successive generations of prototypes exposed, evidencing how the devices available in the technology are free from Single Event Burnout (SEB) or Gate Rupture (SEGR). Actually the high voltage transistors have been also directly tested for SEB sensitivity at the beginning of the development. The last and production-ready revision of the circuit, FEAST2, is also free from any Functional Interrupt (SEFI): the converter continuously provided on-specs output voltage while exposed to a cumulative fluence of 126e6 ions/cm2 in the LET range between 10.2 and 65 MeVcm2mg-1. During the irradiation, occasional transients were observed at the output of the converter, of an average duration below 2us and of amplitude below +10%/-20% of the nominal output voltage. This result was possible after having deeply studied the sensitivity of previous prototypes, in particular using pulsed laser to map the sensitive nodes.

The FEAST2 ASIC is now fully qualified as production-ready, and its production and distribution to the HEP experiments in the form of a full plug-in DCDC module is starting in the second quarter of 2014.

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