180nm CMOS Mixed-Signal Radiation Hard Library as base for a full ASIC supply chain

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IMST

Overview

- Motivation

- Selected Semiconductor Technology

- HARD Library Elements

- SEE and TID test Methodology

- Business Models from ASIC development to qualified IC

Motivation

- Achieving the status of *Capability Approval* for an ASIC supply chain under the ESCC system

    - Providing a Radiation Hard library (HARD) which can be used for mixed-signal ASIC design on a proven semiconductor technology

- Advantage of getting the Capability Approval in addition to QPL/QML status:

    - Only screening and limited evaluation required for a new ASIC

    - No full qualification with radiation tests required for a new ASIC

    - Efficient way of ASIC design:

        - Faster development time

        - lower NRE costs
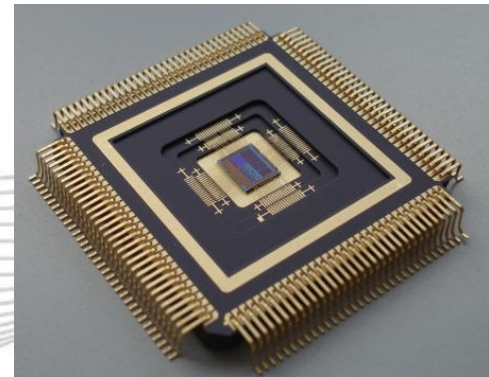
Evaluation of the Semiconductor Technology

- In a former study several technologies have been investigated with respect to

  - Hardness against Radiation

  - Usability for Space ASICs

    - low volume supported via MLM or MLR

    - Location of the FAB (ITAR)

- XH018 from X-Fab has been selected and tested against TID and SEE behaviour with good results

Evaluation of the Semiconductor Technology

- XH018 key features

  - Typical supported supplies 1.8V, 3.3V and 5.0V

  - supporting deep N-well isolation for negative supplies

  - Modular concept

    - LDMOS transistors supports up to 60V of supply voltage

    - High voltage module available supporting 10V supply

    - Bipolar transistors available

    - Thick metal layers optional module

    - OTP cells module / IP

    - RAM compiler

Target for the Library Elements

- Reusability

  - Providing a set of circuit block IP's that can cover a wide range of applications

- Radiation Hardness:

  - Single event latch-up free up to LET of 80 MeV/mg/cm² and 125°C, according to ESCC 25100

  - SEU/SET test, according to ESCC 25100

  - TID test for total dose > 300krads (Si) according to ESCC 22900 Specification

HARD Library IP blocks

IP Block	Main Characteristics	Status
4-Wire SPI Interface	1.8V, 16 registers, 12 bit, each	Silicon/ testing
I/O Cells	3.3V & 5.0V digital + Analog I/O	Silicon/ testing
LVDS Driver	1.8V, Fmax=800MHz	Silicon/ testing
LVDS Receiver	1.8V and 3.3V, Fmax=800MHz	Silicon/ testing
Reconfigurable Multifunctional Operational Amplifier	•Inverting OpAmp with variable gain: -10 dB … +30 dB; 1dB step size • Non inverting OpAmp with variable gain: 0 dB … +30 dB; 1dB step size • LPF 3 different cut off frequencies • I to U • Schmitt Trigger • Voltage buffer	Silicon/ testing
Bandgaps	1.8V & 3.3V trimable	Silicon/ testing
Reference Bias Generators	1.8V & 3.3V with PTAT and constant currents & adjustable voltage references	Silicon/ testing
Temperature sensor	1.8V, temperature range from -40°C…+150°C	Silicon/ testing
POR Generator	POR delay: 5µs	Silicon/ testing
LDO	Input voltage: 3.3V Output Voltage: 1.8V with adjustable short protection	Silicon/ testing

HARD Library IP blocks

IP Block	Main Characteristics	Status
Level shifter High-Low	input signals with 0V…1.8V output signals with -5V…-3.2V	Silicon/ testing
Level shifter Low- High	input signals with -5V…-3.2V output signals with 0V…1.8V	Silicon/ testing
Digital Level shifter High-Low	3.3V to 1.8V	Silicon/ testing
Digital Level shifter Low- High	1.8V to 3.3V	Silicon/ testing
16 bit MUX	Max. signal frequency: 800MHz	Silicon/ testing
11 bit ADC	charge-scaling SAR ADC fast mode: 200KS/s	Silicon/ testing
Memory cell	256x10 bit RAM module Clock frequency: 25MHz.	Silicon/ testing
12 bit DAC	segmented current steering DAC	Silicon/ testing
Memory cell	OTP	Future design
Serializer / Deserializer	Data Rates: 600 Mbps	Future design
Clock PLL with integrated VCO	output clock frequency range: CMOS = 6 MHz … 300 MHz LVDS = 12.25 MHz…600 MHz period jitter: 50ps (PK-PK)	Design
DCXO	Supports 6 MHz … 50 MHz crystals via digital controlled C0	Design

Test Methodology

- Design of 1st test chip
    - Containing all IP's as single circuit to investigate single block behaviour
    - Chain of all IP blocks to investigate interaction of single IP blocks

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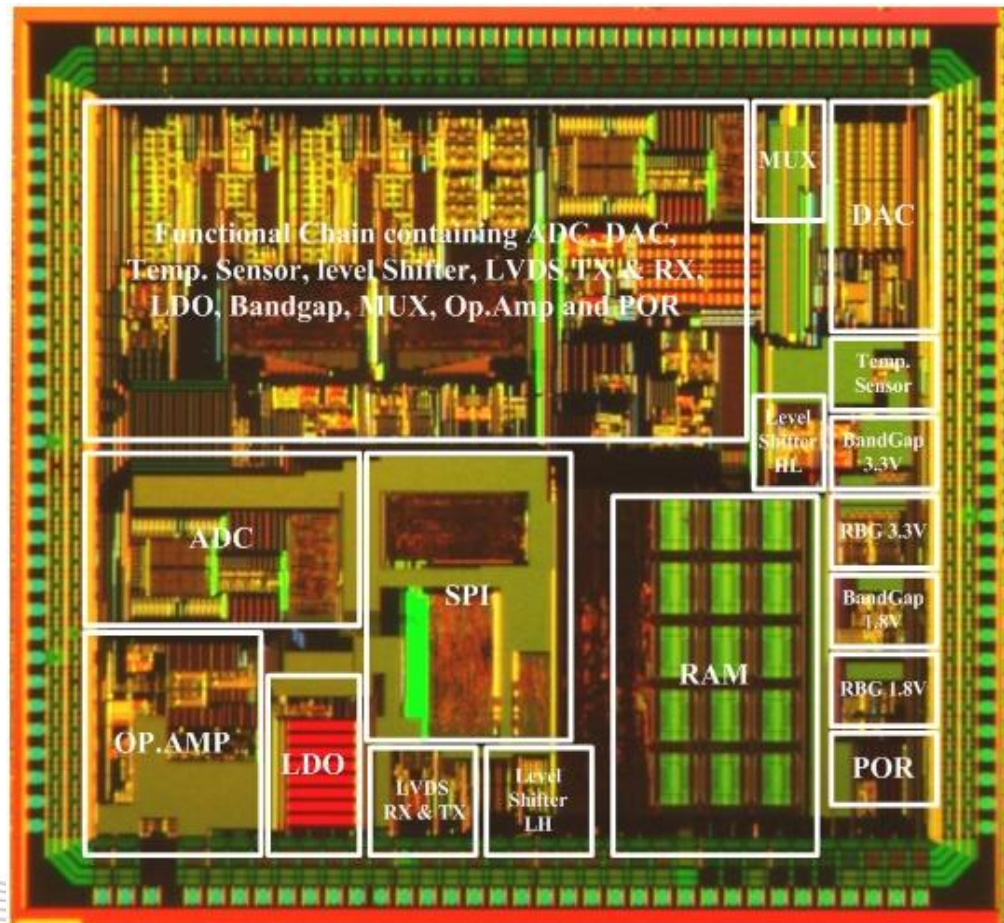
Test Methodology

- ## SEE tests
    - Monitoring all supply and signal currents for Latch-up detection
    - Monitoring and counting SET at all outputs
    - Monitoring SEU on RAM, ADC, DAC and SPI blocks with test routines
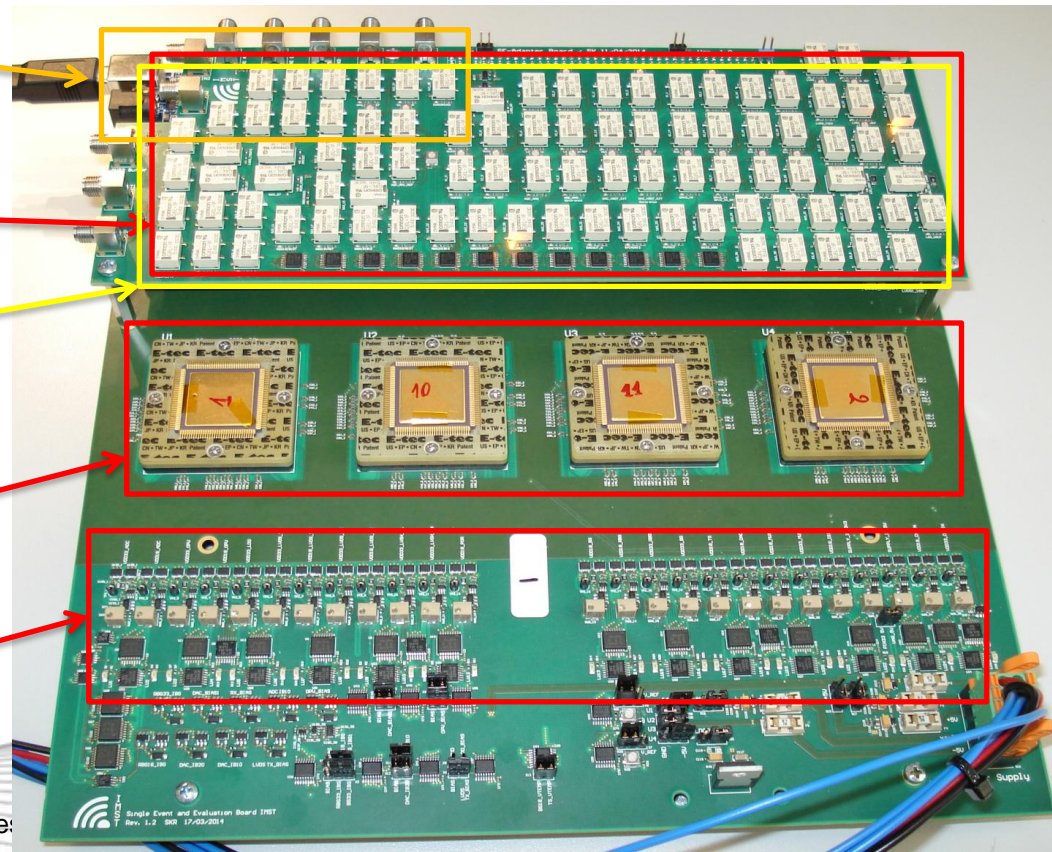   - Will be performed at CYCLONE110 (UCL Belgien)

FPGA Board for
PCB and IC control
(buried under relay board

I/O Multiplexer
with relays

SEE monitoring
with dual comparators
and controllable references
(buried under relay board)

4X DUTs

Latchup protection
and monitoring

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Test Methodology

- SET Monitoring Concept:
    - Circuit block outputs routed to dual comparators
    - SW controlled DAC giving the comparison values e.g. ± 50 mV around DC level of the circuit block output
    - comparator outputs are routed to counters
    - Additionally outputs can be routed to an Oscilloskope to measure signal shape (magnitude, ringing, frequency)

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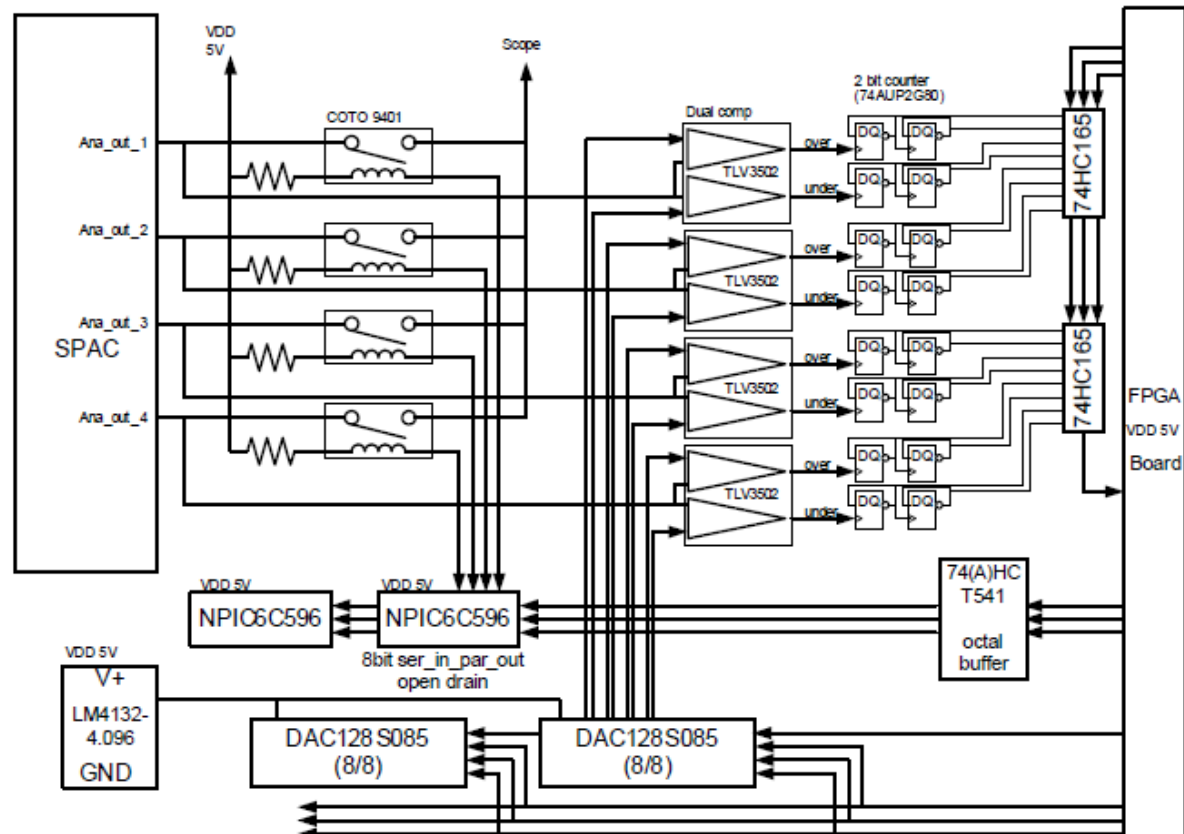
TID and Power Supply Board

- ## TID test
  - Test automation to measure performance of all single blocks vs. exposure dose rate
  - Will be performed at Co-60 Gamma irradiation facility FHG Euskirchen

9X DUTs:
7X biased
2X un-biased
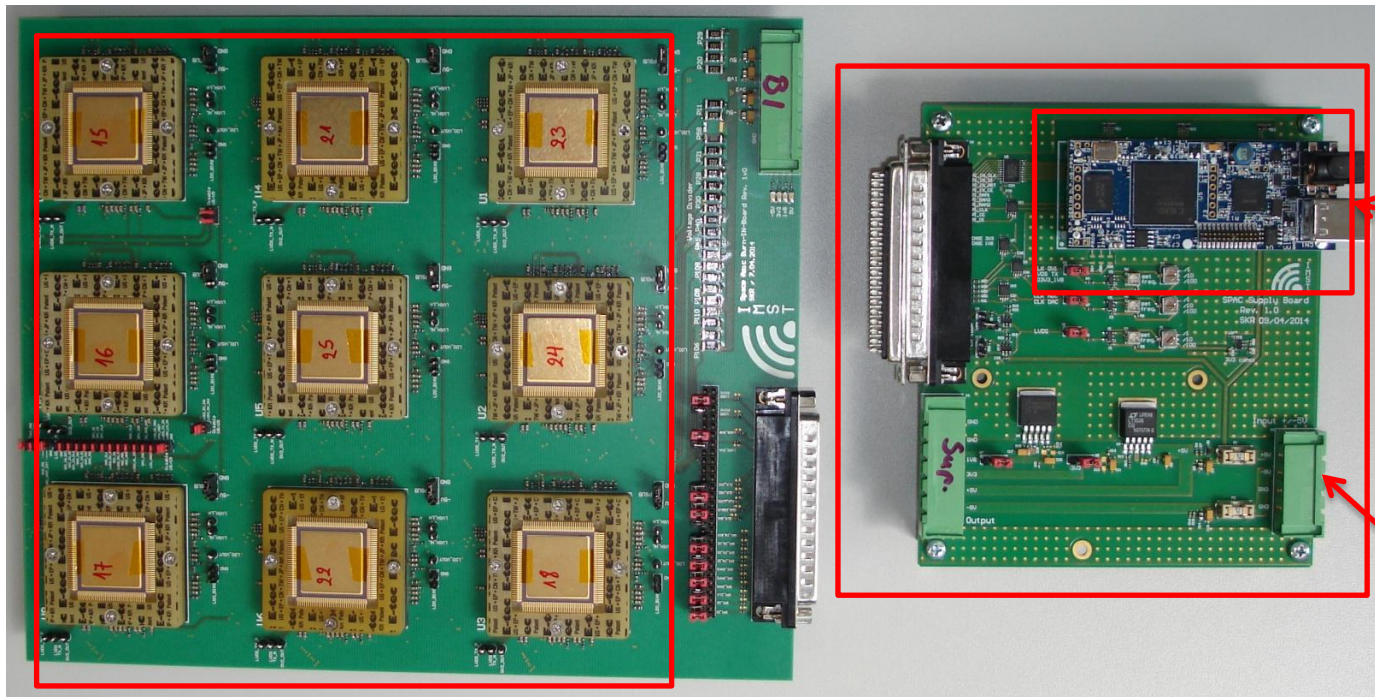
FPGA board for Stimulus signals

Power supply board

Measurement Results

- Project still in progress

- Irradiation test scheduled for July

- At this point Burn – In is beeing performed

Business Model

- Model 1: Turn Key Design $\longrightarrow$ Delivery of tested and qualified ASIC

- Model 2: Interactive Design. Customer is co designing on digital system and / or Top Level. IMST is adding analogue block in case of a mixed signal ASIC and is responsible for the final layout and tape in. $\longrightarrow$ Delivery of tested and qualified ASIC

- Model 3: IMST IP license of dedicated circuit blocks to end-customer. IMST will not produce the tested and qualified RH ASIC. $\longrightarrow$ Only wafers will be delivered.
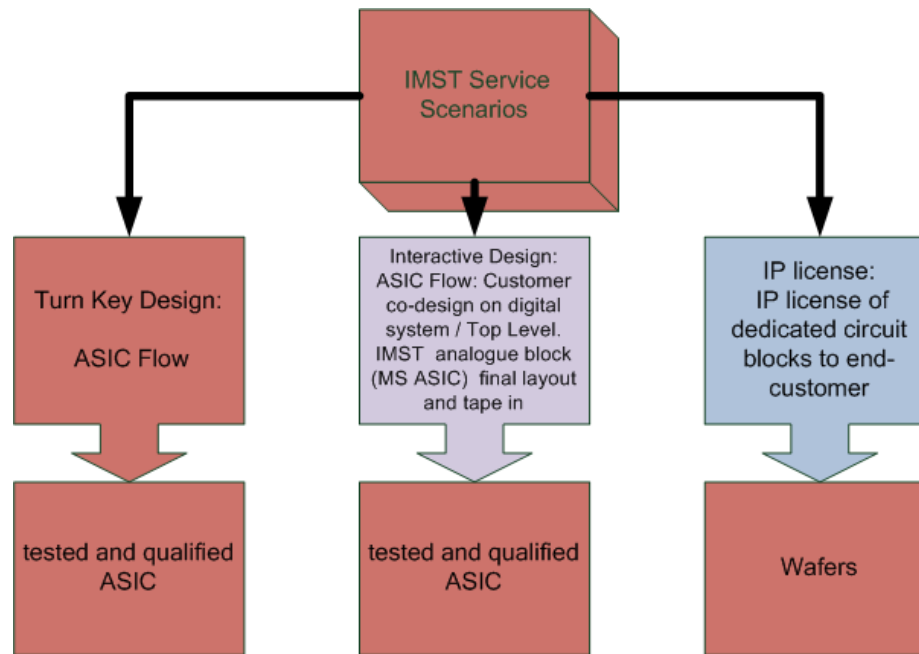
Outlook

- ASIC fabless manufacturer following ESCC rules & specifications

- Having Capability Approval of electronic component technologies for space applications

- Providing a space qualified technology & supply chain for Mixed- Signal ASIC

- Owning a space library

  - Hard Against Radiation by Design Library (HARD Library)

  - Continue work on HARD Library by adding more circuit blocks

Acknowledgement

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