180nm CMOS Mixed-Signal Radiation Hard Library as base for a full ASIC supply chain

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Abstract

In recent years the importance of mixed-signal ASIC supply for Space Applications in Europe has grown. Along with this perception, customers like to see Europe getting more independent from other worldwide sources in obtaining these components on the market. Following the newest trends, IMST is currently working together with TESAT Spacecom towards a mixed-signal library as part of an ESCC qualified ASIC supply chain.

This paper presents the IP blocks of IMST, which are developed using innovative design and radiation hardened techniques. These blocks are going to go through a program of evaluation and qualification tests. The radiation hardened library of IMST, called HARD Library (HARD= Hard Against Radiation Design) is built from I/O cells for 3.3V and 5.0V supply voltages, reconfigurable multifunctional operational amplifier, voltage and current references, memory cells, data converters and other analog and digital IP blocks, which will be described in this paper. The HARD Library is based on the 180nm CMOS technology from XFAB, which is a modular mixed signal high voltage technology. It supports operation by negative supplies, which is one of the characteristics of the HARD Library elements. Another feature of this technology is offering different modules for low power, high temperature, high voltage and non volatile memory all in one platform. XFAB's 180nm CMOS technology is already tested with good results against radiation effects.

Furthermore, in this paper different scenarios of design flows will be presented, about how a customer can use the HARD Library. Since the project is still in progress, evaluation test results are not available yet. Finally the paper will show IMST´s capability to operate as a supplier for full space qualified ASICs to the market, handling the full supply chain in one hand.

I. PREFACE

The development of the radiation hardened library for mixed-signal ASICs is a German Government funded project by DLR. The aim of the project is for IMST to earn the status of capability approval under the ESCC system as a manufacturer for space qualified RadHard ASICs.

In a pre-study TESAT Spacecom commissioned IMST to investigate a proper CMOS semiconductor technology for the following work on the capability approval. In this study the XFAB's XH018 process has been selected as best suited for this purpose. Radiation tests have been performed on components and test circuits to find out SE effect sensitivities and TID behavior. This information has been used for the design of the presented HARD library.

II. HARD LIBRARY ELEMENTS

As the main aim is to develop a "state of the art" Mixed Signal ASIC for space applications, the library elements are selected in such way, that they are able to provide a full set of useful circuit blocks, which are needed to build up a wide range of different ASICs.

For the design radiation hardened IP blocks, several mitigation techniques are considered in the analog designed circuits to minimize SEE and TID effects. One layout technique to reduce SET effects in differential circuits is called "Differential Charge Cancellation" DDC proposed in [2]. The orientation of the transistor arrays is done in that way, that a SE strike affects both paths in the differential signal resulting in a common mode pulse. Due to the common mode rejection of differential circuits the pulse will be suppressed and has minor effects on the differential signal.

Circuit topologies to minimize SET effects in single ended circuit like biasing networks are described in [3]. Sensitive nodes are stabilized against transient signals induced by a SE strike. The technique is called "Sensitive Node Active Charge Cancellation", SNACC. Another mitigation technique is filtering analogue signals, as described in [1]

An example for TID effect reduction is "Dynamic Base Leakage Compensation", DBLC, that can be used in band gap circuits to protect the sensitive bipolar transistors against leakage current variation [4].

For digital designs like SPI controller and the state machine for RAM control radiation hardening has been realized by triple mode redundancy TMR [1].

The following list gives an overview of the library elements with their key features and status of design:

IP Block	Main Characteristics	Status
4-Wire SPI Interface	1.8V, 16 registers, 12 bit, each	Silicon/ testing
I/O Cells	3.3V & 5.0V digital + Analog I/O	Silicon/ testing
LVDS Driver	1.8V, Fmax=800MHz	Silicon/ testing
LVDS Receiver	1.8V and 3.3V, Fmax=800MHz	Silicon/ testing
Reconfigurable Multifunctional Operational Amplifier	•Inverting OpAmp with variable gain: -10 dB … +30 dB; 1dB step size •Non inverting OpAmp with variable gain: -10 dB … +30 dB; 1dB step size •Low Pass Filter (LPF); 3 different cut off frequencies •Current to Voltage Converter with different input ranges •Schmitt Trigger with adjustable hysteresis •Voltage buffer	Silicon/ testing

IP Block	Main Characteristics	Status
Bandgaps	1.8V & 3.3V trimable	Silicon/ testing
Reference Bias Generators	1.8V & 3.3V with PTAT and constant currents & adjustable voltage references	Silicon/ testing
Temperature sensor	1.8V, temperature range from -40°C…+150°C	Silicon/ testing
POR Generator	POR delay: 5µs	Silicon/ testing
LDO	Input voltage: 3.3V Output Voltage: 1.8V with adjustable short protection	Silicon/ testing
Level shifter High-Low	input signals with 0V…1.8V output signals with -5V…-3.2V	Silicon/ testing
Level shifter Low-High	input signals with -5V…-3.2V output signals with 0V…1.8V	Silicon/ testing
Digital Level shifter High-Low	3.3V-1.8V	Silicon/ testing
Digital Level shifter Low- High	1.8V - 3.3V	Silicon/ testing
16bit MUX	Max. signal frequency: 800MHz	Silicon/ testing
11 bit ADC	charge-scaling SAR ADC fast mode: 200KS/s	Silicon/ testing
Memory cell	256x10 bit RAM module Clock frequency: 25MHz.	Silicon/ testing
12 bit DAC	segmented current steering DAC	Silicon/ testing
Memory cell	OTP	Future design
Serializer / Deserializer	Data Rates: 600 Mbps with a reference clock Power: <500 mW	Future design
Clock PLL with integrated VCO	output clock frequency range: CMOS = 6 MHz … 300 MHz LVDS = 12.25 MHz…600 MHz period jitter: 50ps (PK-PK)	Design
DCXO	Supports 6 MHz … 50 MHz crystals	Design

Table 1: Summary of HARD library elements

4-wire SPI interface

The SPI interface consists out of two sub-modules. The serial interface module is the communication interface to the external master. The register module stores the received data from the serial interface and provides readable register content to the serial interface. One serial interface module can be connected to two register modules. This modular approach makes it possible to store 8 or 16 registers with a width of 12 bit.

I/O cells

Several 3.3V digital I/O cells, with different driver capability, are provided by the HARD Library. All of them provide separated supply voltage domains for the 3.3V I/O, the 3.3V intermediate buffer and the 1.8V chip core.

One dedicated 5V digital I/O cell is provided by the HARD Library. It provides separated supply voltage domains for the 5V I/O, the 5V intermediate buffer and the 1.8V chip core

The HARD Library also provides an analog I/O pad with serial low resistances and ESD structures to supply and ground rails

LVDS Interfaces

For digital high speed interfaces outside the chip, LVDS receivers and drivers are designed with a wide range of common mode voltage and supply variations to cover various applications. Both, the LVDS driver and LVDS receiver circuits, contain configurable termination resistors (100Ω) for a maximum flexibility of possible applications.

Analog to Digital Converter

The provided SAR-ADC is a charge-scaling type ADC with binary weighted capacitor arrays as DAC. The ADC is optimized for low-power. Two modes are available: a default low power mode, for slower conversion (up to 100kS/s) and a high-speed mode (up to 200kS/s) where the power is approximately doubled.

Operational Amplifier

The operational amplifier (OpAmp) provided in the HARD Library is an universal circuitry with 3.3V rail to rail input/ output stage. Optionally a negative supply voltage can be applied to the ground node to work on a +/- supply. Reconfigurable circuitry is added to the OpAmp core to obtain an inverting and non-inverting amplifier with a voltage gain range from -10dB up to +30 dB in 1dB steps. A low pass filter with three cut off frequencies at 0.1 MHz, 1 MHz and 10 MHz is another function. Furthermore a I to V converter with different transimpedances, a Schmitt Trigger with controllable hysteresis and a voltage buffer is selectable.

Level shifter

The digital level shifter (LH) element converts digital input signals from the core voltage domain (VDD=1.8V) to output voltages in the 3.3V supply voltage domain and in the other way around (HL) it converts digital input signals from the I/O voltage domain (VDDO=3.3V) to core voltage domain (VDD=1.8V).

LDO

The LDO works in a source follower configuration with a NMOS transistor as pass device. A short circuit protection circuit will switch off the LDO as soon as a selected current range is exceeded.

Analog MUX

The test MUX is a 16 to 1 MUX which is build up using cascaded transmission gates. A logic is included to select one of the 16 inputs to be connected to the output. The internal control voltages of the transmission gates use the 3.3V supply rail and therefore can handle analog voltages from 0V to 3.3V.

Digital to Analog Converter

The provided Digital to Analog Converter is a 12 bit segmented current steering DAC.

The DAC output is a differential voltage, which is proportional to the DAC input voltage. The input voltage can either be provided by the internal band gap or by an external constant voltage. The input voltage is converted into an input current. In order to achieve the 12 bit resolution, this input current is calibrated to set the gain of the DAC within the correct range. The DAC output voltage is buffered by a differential amplifier.

RAM

Aim of the RAMTEST module is to save a 10 Bit width word within any of the 256 addresses and recognise radiation effects on the stored data. Due to the Dual-Port feature of the RAM it is possible to write/read simultaneously two RAM addresses.

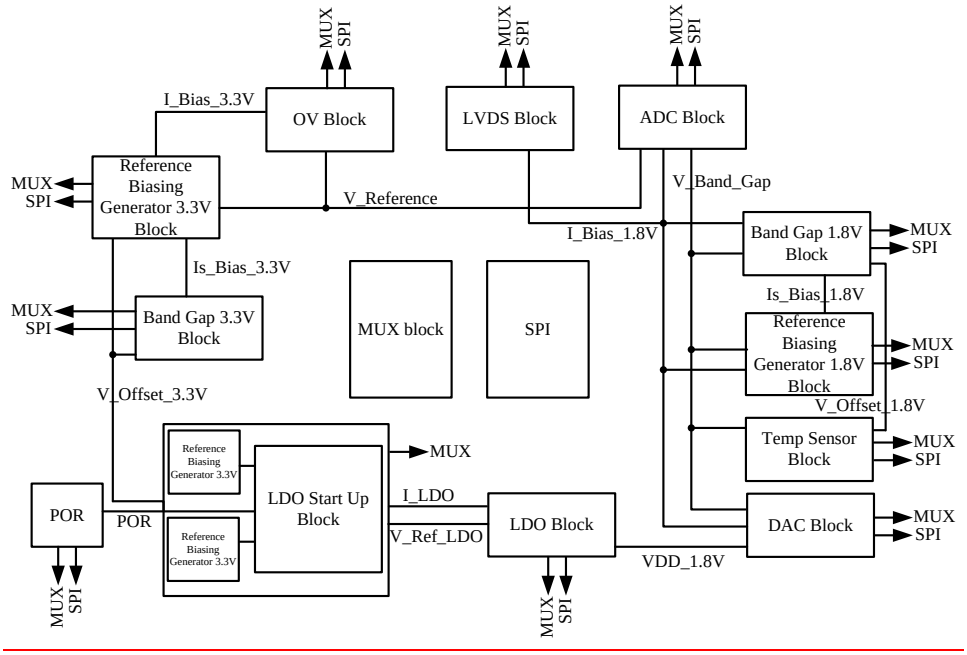

Figure 1: Block diagram of Test Chain

III. SEE AND TID TESTS

A. *Test Chip*

In the current stage of the project, a test chip for evaluation has been designed, containing all library elements for single measurement. In order to investigate the interaction of the circuit blocks with each other, a test chain has also been placed on the test chip with test points on all interfaces. Figure 1 shows the block diagram of this test chain. The 3.3V and 1.8V domains are working with each other with internal level shifter. Figure 2 shows the floor plan of the produced die with markers to identify each of the circuit blocks. The test chip is packaged in a ceramic package with 132 pins.

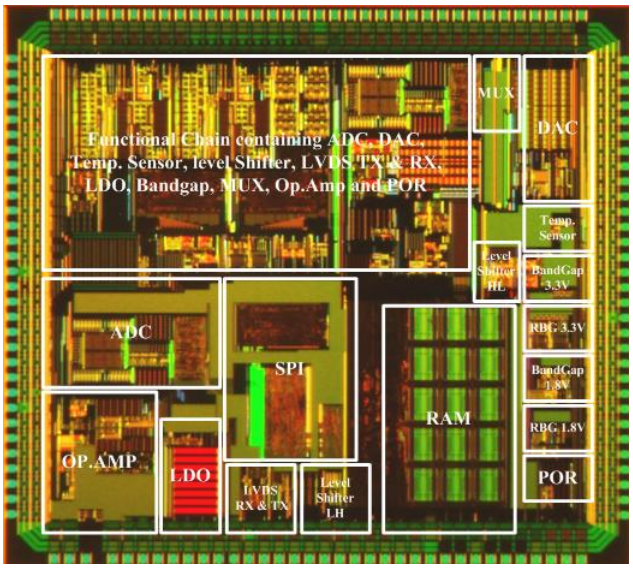

Figure 2: Photo of the Test Chip

B. *SEE test*

The SEE test is taking place at the CYCLONE110 facility on the Cyclon Resource Centre Louvain-la-Neuve. For the SEE testing a PCB has been designed with special ability to monitor SEL, SET and SEU. The board is shown in Figure 3. On the main board 4 DUTs are mounted and in the lower side the latch up protection is to be seen. Hidden under the adapter board, multiple comparators are used to detect and count SET pulses on each analog block. The adapter board has I/O multiplexers with relays to route all chip pins to SMA connectors. A FPGA board is used to control the chip setting and PCB setting during irradiation with heavy ions.

SEL monitoring: The supply current on each circuit block is monitored and can be switched off (Latch Up protection), when reaching a predefined limit, which is set to approx. 100% higher current as typical operating mode current. While switching off the supply, a flag, which corresponds to this SEL, is sent to the FPGA board, that stores the event for later evaluation.

SEU monitoring: Only digital circuits can be tested for SEU. The SPI controller is repeatedly writing a test pattern, which is read back and compared with the original sent pattern. On the ADC test, outputs are continuously written out, without changing the input, in order to monitor any upsets. The RAM model is hardened by TMR techniques. For SEU tests of the RAM block, a special build in self test is designed. The state machine writes consecutively different test patterns into all memory cells and compares the read result directly after it. During erroneous data read several read attempts are done. Therefore the algorithm is able to distinguish between errors in the memory cell and errors during the read/write process. Further on, the algorithm is also able to determine in which TMR line this error occurs.

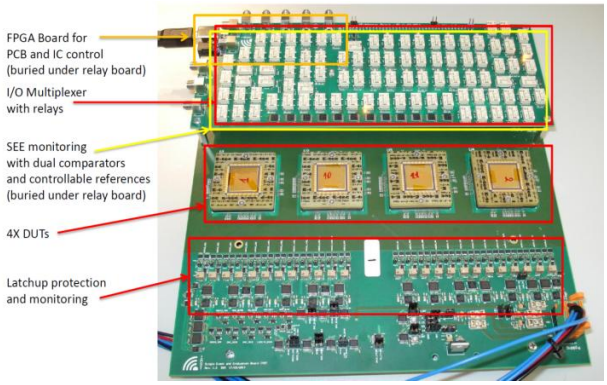

Figure 3: SEE and EV test board

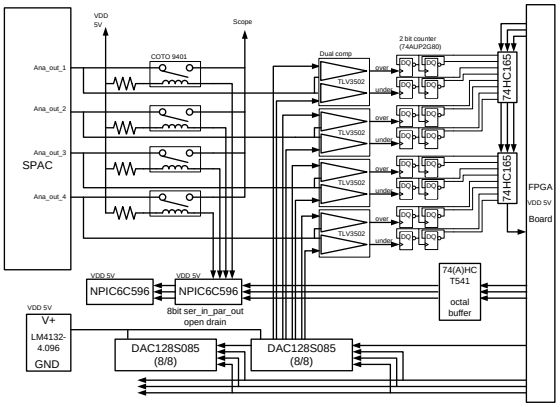

Figure 4: SET test concept

In case of an SEU an error output frame word is sent out with detailed information on the error location and if an error has been corrected or not using the TMR structure.

SET monitoring: Figure 4 shows the concept of monitoring the SET effects. All single circuit blocks have outputs routed to a dual comparator. The reference voltage of the comparator can be controlled in mV steps by a DAC output individually for each comparator. With this approach two threshold levels can be set: One threshold level some mV below the DC signal level and one threshold level some mV above it, in order to detect SET. The comparator outputs are routed to counters and their values are stored into the FPGA. For a qualitative evaluation of the SET signals, each output can be multiplexed to an oscilloscope, that is able to save screenshots, whenever a SET triggers the oscilloscope.

C. TID test

Figure 5 shows the TID test board together with the supply board. The supply board contains a FPGA board to generate stimulus files for the IC during irradiation like clock signals for the data converter or LVDS signals. A special GUI and a test sequence are programmed in MATLAB to set the chip and evaluation board settings, in order to evaluate and measure the test chip before and after the Total Ionizing Dose test as well as during the irradiation breaks.

The same board is used for the screening and burn in.

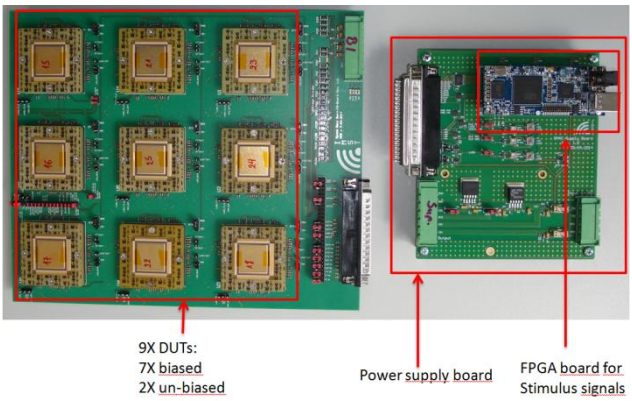

Figure 5: TID test board and supply board

IV. Measurement Results

Since the project is still in progress and the radiation test are scheduled for this year, measurement results of the test chip will be presented at a later point. These results will be used to enhance the performance of the actually space qualified developed ASIC at the end of the project.

V. ASIC Supply Chain and Design Flow

Designing ASICs usually requires a close collaboration between the customer who is using the ASIC in his application and the design house. Having the Capability Approval status, IMST is able to design and deliver space qualified ASICs, without needing for every developed ASIC new, long lasting and expensive evaluating and qualifying test procedures. Having this status, IMST is able to offer variation, inside its defined capability domain, according to the customer's needs and assure a qualified manufacturing procedure and screening of the product. IMST is using its HARD library elements based on a customer's specification and offers different business models for delivering the agreed ASIC, always according to the European standards and rules. Table 2 shows typical design steps from the specification to the RadHard ASIC delivery for three different business cases: Turn-key, Interactive and IP licence case.

In the turn key design, IMST takes over the ASIC Flow and deliver tested and qualified RadHard ASICs based on customer specification.

In the interactive design, IMST and the customer are co-designing the ASIC. IMST is responsible for the final layout and tape in and delivers tested and qualified RadHard ASICs. Table 2 (black path) shows the different interactive steps which can be executed either by IMST or the customer.

For the IP license case, IMST can offer IP license of dedicated circuit blocks to the end-customer. The customer will get simulation models of the IP blocks and X-FAB will place the layouts of the IP's as part of the tape-in procedure. In this case, IMST will not produce the tested and qualified RadHard ASICs. Only wafers will be delivered by X-FAB.

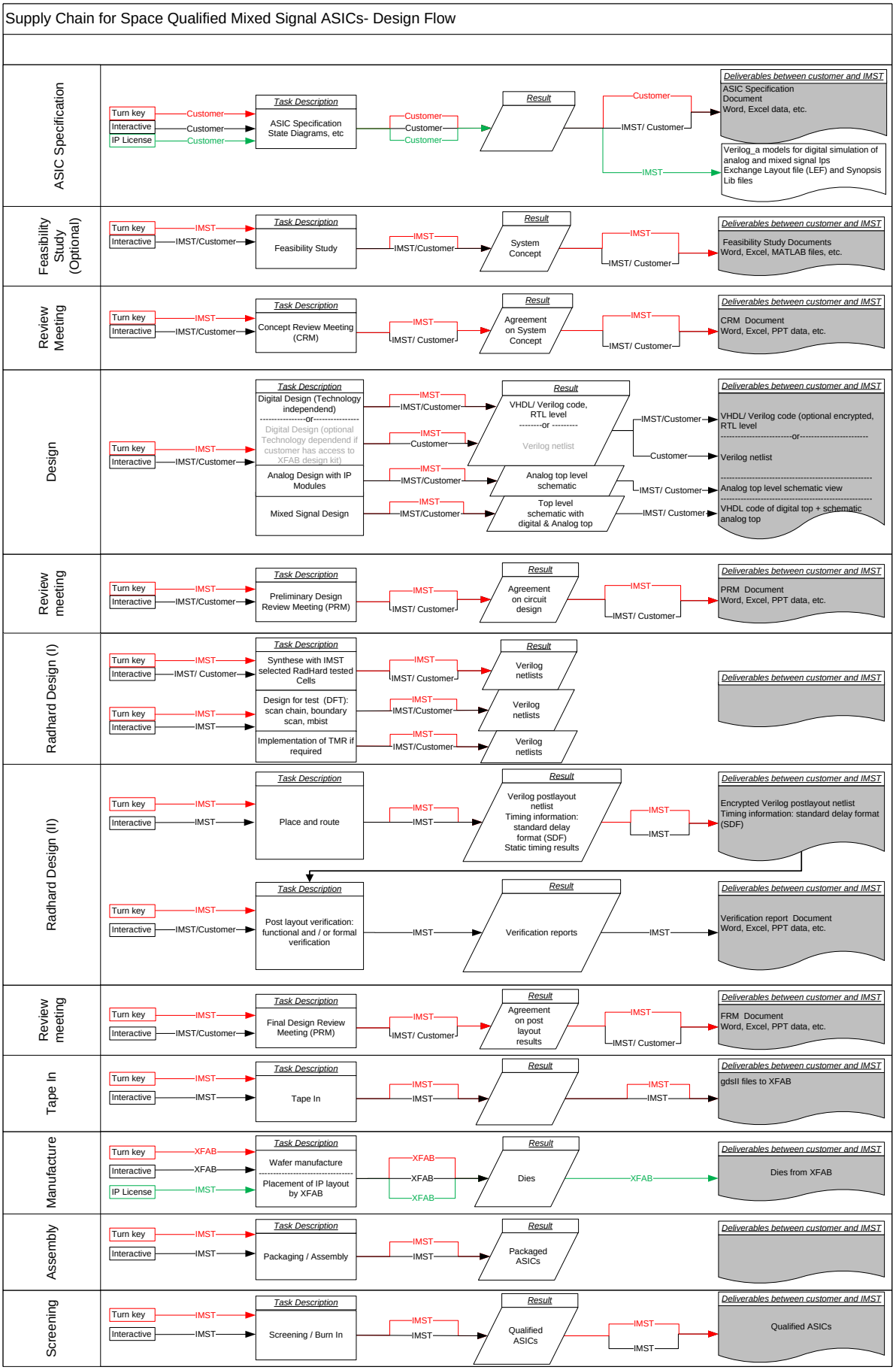

Table 2: Supply Chain Scenarios

VI. CONCLUSION

A set of radiation hardened analog and mixed-signal IP's are presented to be used within an ASIC supply chain. For customers, different scenarios are shown, on how they can interface with IMST and interact in the design of the ASIC. Building up this supply chain, finishing the design and tests of the HARD library and getting the ESCC approval is the aim of the funded project by DLR. The planned finish of the project is in Summer of 2016.

VII. REFERENCES

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