THE DEVELOPMENT OF A RADIATION TOLERANT LOW POWER SRAM COMPILER IN 65NM TECHNOLOGY

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OUTLINE

Introduction

Specifications

Strategies applied

Architecture and subblocks

Layout and compiler

Summary and references

TRIGGER SYSTEM IN LHC EXPERIMENTS

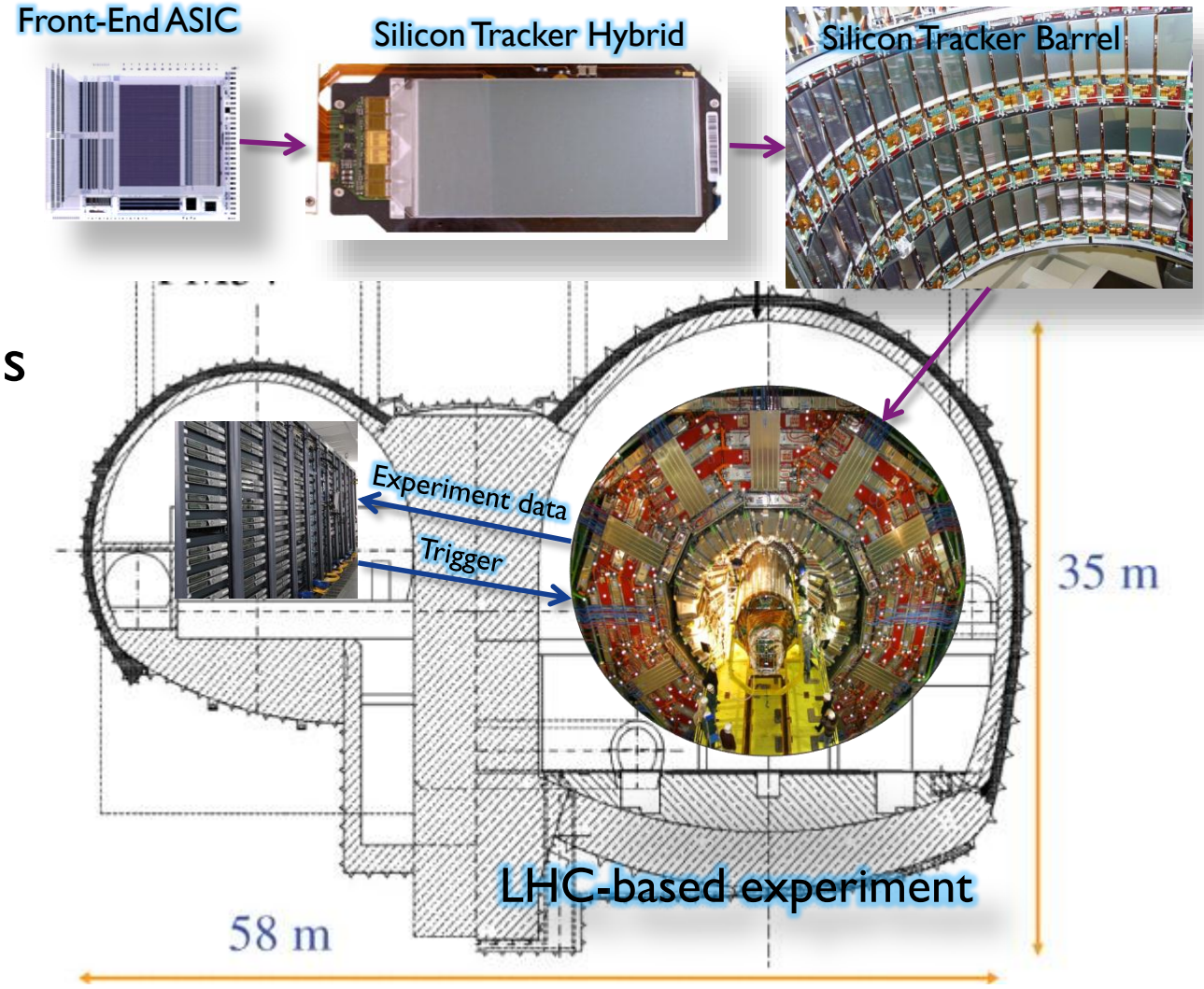
Single event is ~1MB data

Collision rate 40 MHz
~40 TB/s of data

- not all events are interesting for physics

The trigger system selects only interesting events

- reduces data shipped out of the experiments
- Average trigger rate ~100 kHz

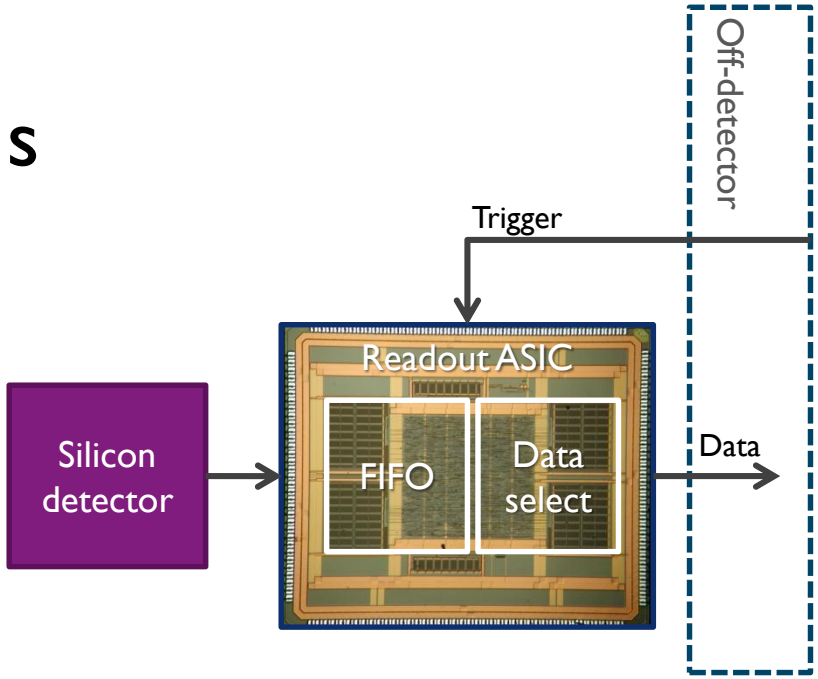


MOTIVATION

Trigger system evaluation time is order of µs

During this time, data is stored in a FIFO

- FIFOs are normally embedded in front-end ASICs as SRAM blocks



The LHC luminosity upgrade imposes stringent constraints to the front-end detector electronics

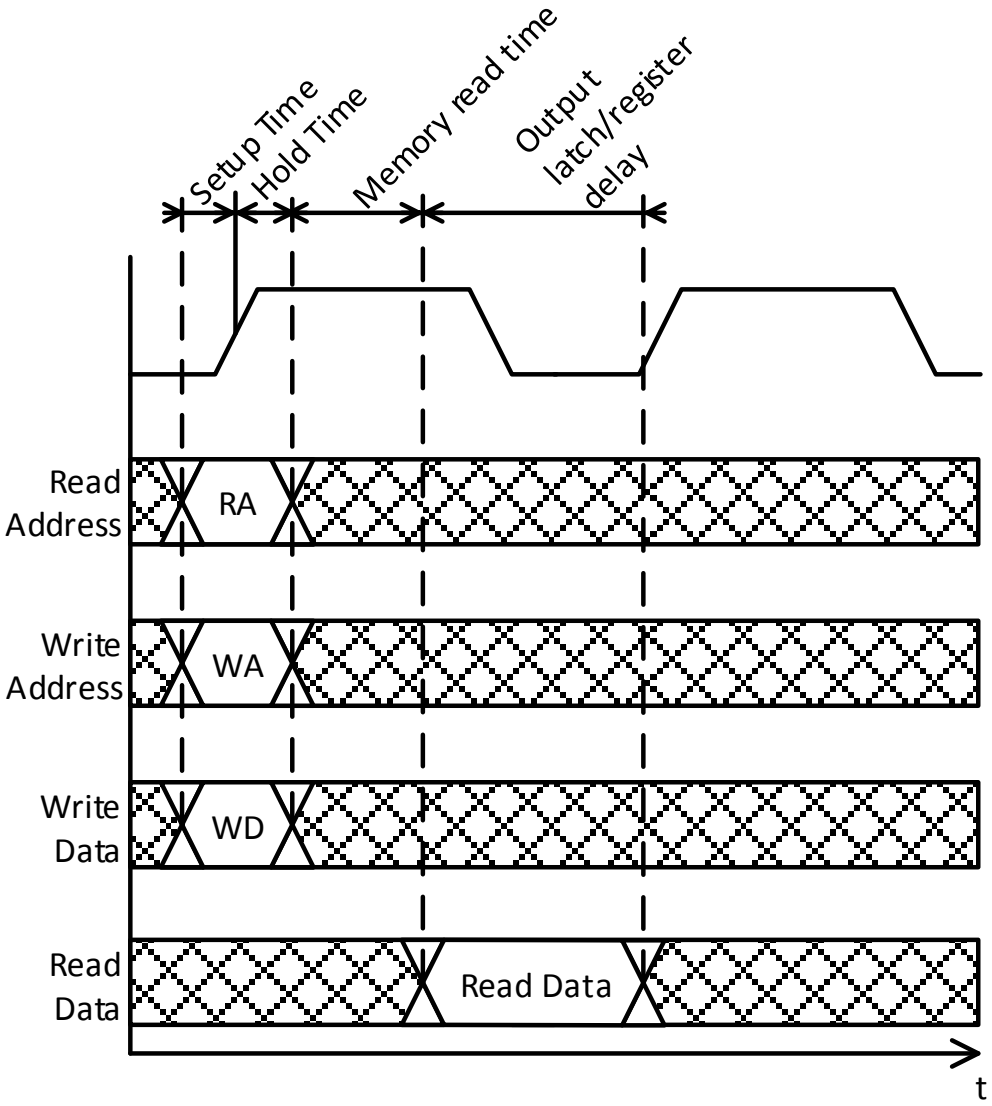
- Low-power, fast data rates, small pixels, radiation-hard …
- 65nm CMOS is the chosen technology for many sub-detector ASICs

High Luminosity LHC

SPECIFICATIONS

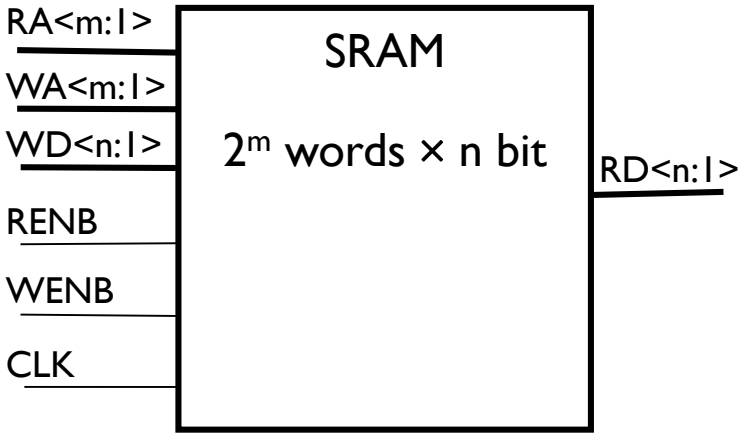
- Pseudo dual port behavior
- 65 nm technology with standard Vt devices
- 4 metal layers used
- Supply 1.2 V ± 10%
- Power consumption 24uW/MHz
- Temperature range: -40 ... 125°C
- Max frequency 80 MHz
- TID hardening > 200 Mrad
- LET threshold > 15 MeVcm^2/mg

TIMING BEHAVIOR



Pseudo dual port

- 1 master clock
- 2 address inputs (R/W)
- 1 data port (I/O)



LOW POWER

Multiple techniques

- Split word lines
  - Global word lines
  - Local word lines with optimized buffer
- Discharge level of bit-lines reduced to 100mV
- Timing optimized by self-timing
  - Dummy memory

RADIATION HARDENING

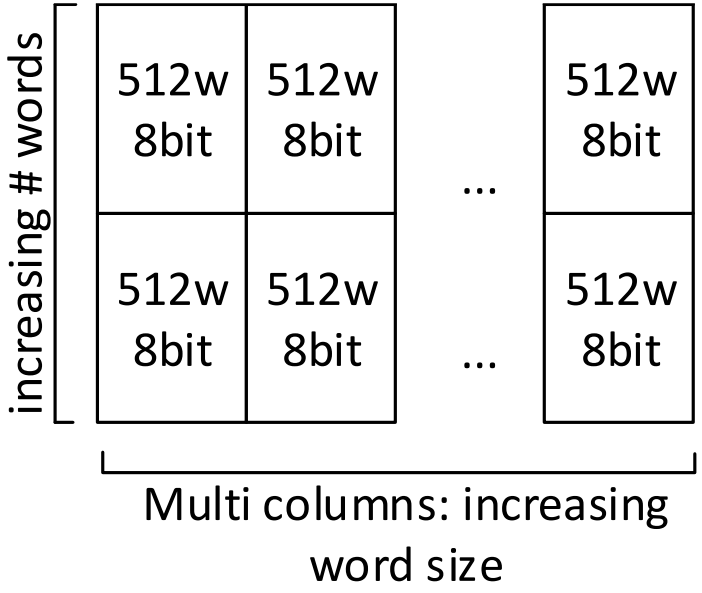
TID

- Minimum size MOS > DRC minimum
- p+ guard bands between n-type regions

SEE

- Drive strength hardening
- DICE FF

ARCHITECTURE



ADDRESS DECODING

3 LSB : bit interleaving decoding

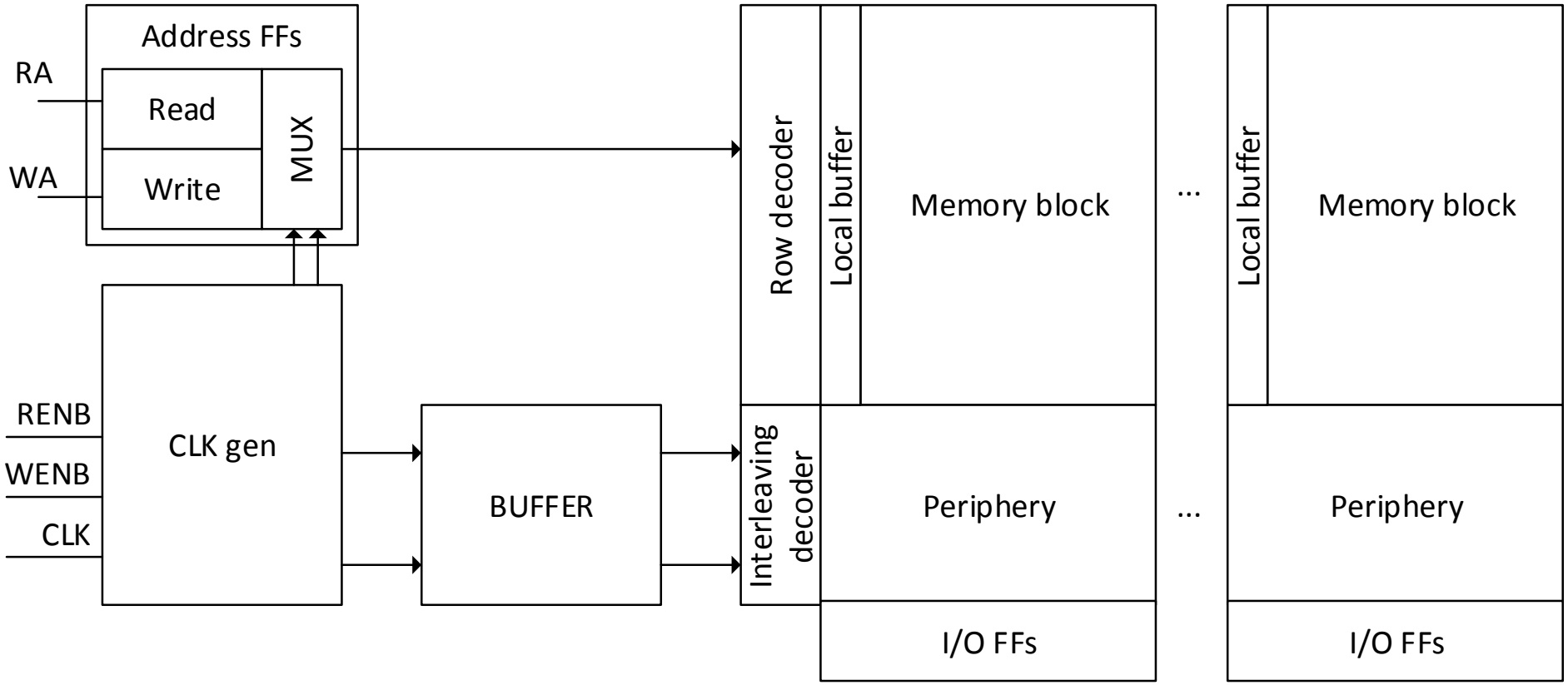
INT-B : word line decoding

1-2 MSB : row decoding

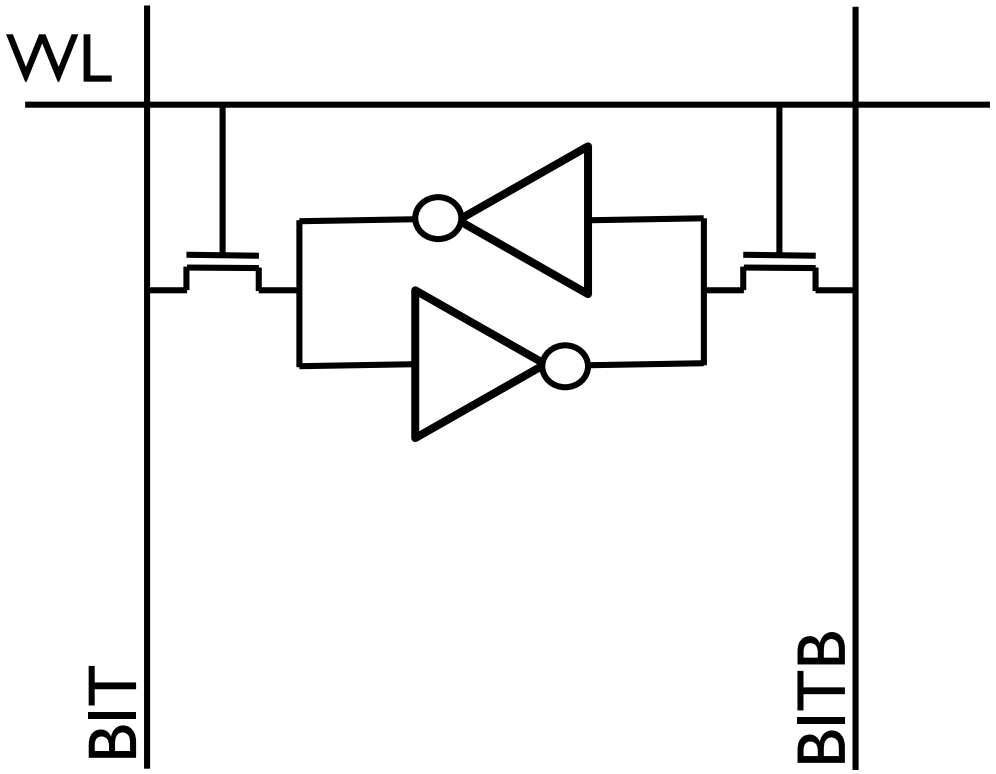
Aspect ratio improvement

$$\#mosaic\ rows = \sqrt{\frac{current\ aspect\ ratio}{target\ aspect\ ratio}}$$

ARCHITECTURE



MEMORY CELL



Standard 6T cell

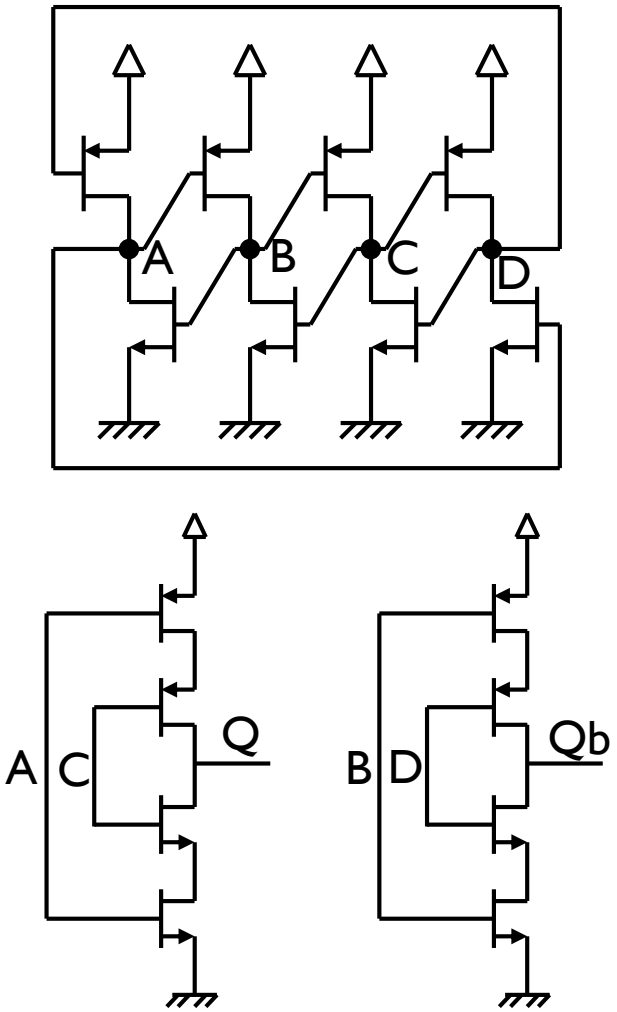
TID hardening:

- Not minimal width of MOS
- P+ guard band

Verified PVT

SNM > 18% of Supply voltage

DICE FLIP-FLOP



Corner stone of SEU hardening

Output redundancy

- A=C and B=D

cCell

- Absorbs SEU by going high impedance

Location in the design:

- Stores addresses
- Stores I/O data

PERIPHERY

8 bit interleaving 

- Preventing Multi Bit Upset
- Aspect ratio improvement for small word sizes
- Multiplexer between BIT lines

Sense amplifier

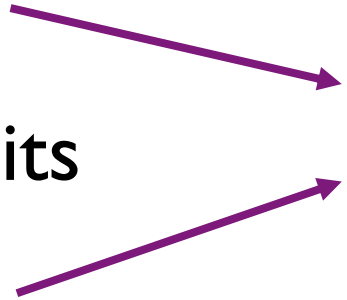
Precharge Transistors

Write transistors

MEMORY BLOCK

2 flavors

- 512 words x 8 bits
  - 64 word lines
- 128 words x 8 bits
  - 16 word lines



8 bit interleaving

Split word line

- Local optimized buffers

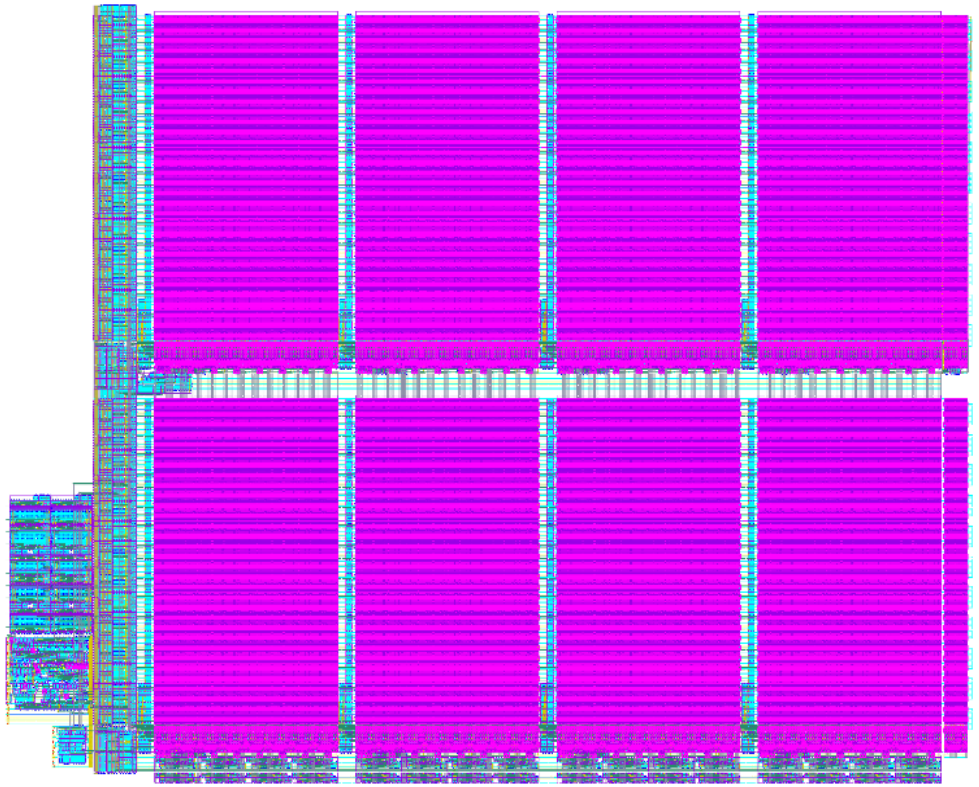
Output multiplexing gates to increase # words

CLOCK GENERATOR

State machine

- Controlling all signals
  - Precharge & discharge of BIT lines
  - Select read/write address
  - Output latch
  - Write transistor
- Self-timing delays between states
  - Dummy memory block
- Reset every clock cycle

LAYOUT



2 dedicated floorplans

- 128 words memory block
- 512 words memory block

2 SRAMs on test chip

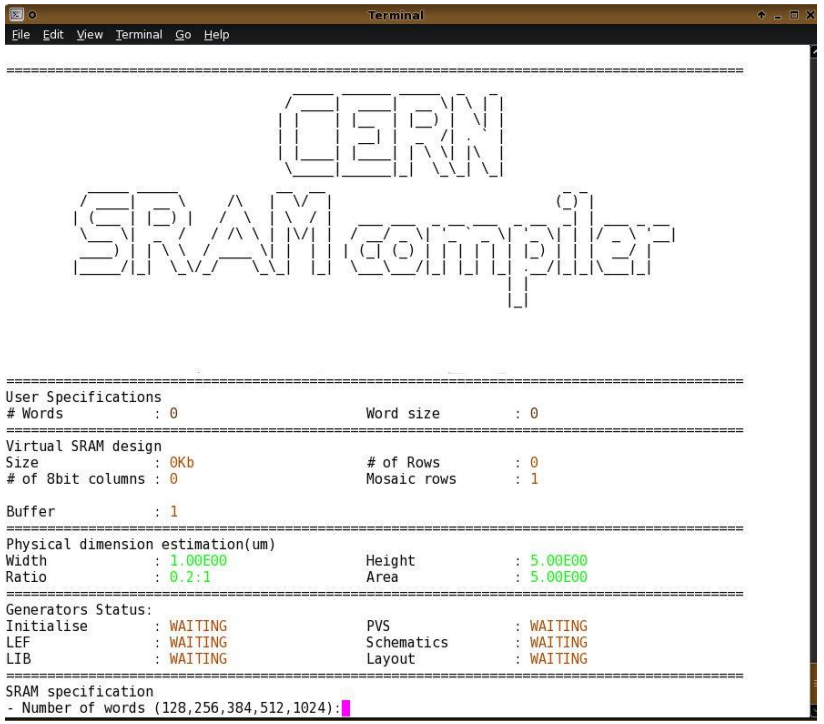
- 1024 words x 32 bits ≈ 450µm x 380µm
- 128 words x 8 bits ≈ 245µm x 70µm
- Post layout verified in all PVT corners

COMPILER

2 layered system

- VDL for easy planning
  - Dimensions
  - Buffer size
- IL generates views
  - Modular structure

Virtual design layer



JAVA

Implementation layer

SKILL

PEX

Open Access database

LEF

LIB

DOC

SUMMARY

Presented the design of a SRAM compiler

- 65nm CMOS technology
- Pseudo dual port
- Low power
- Radiation hardened against TID and SEE
- 2 flavors in memory blocks for optimal scalability
- 2 layered compiler
  - Virtual design
  - Modular implementation layer