Contribution ID: **12** Type: **Oral**

The development of a radiation tolerant low power SRAM compiler in 65nm technology.

Monday, 30 June 2014 16:40 (20 minutes)

With the upcoming upgrades of the LHC experiments, it will be necessary to improve the performance and reduce the power consumption of the detector readout electronics. CERN has chosen to use a 65nm technology for part the new generation ASICs targeted to these upgrades. For this technology the SRAM memories within the readout circuitries need special attention as the commercially available IP blocks don't give the necessary radiation tolerance.

This paper will describe the design of a technology independent SRAM compiler design platform with a custom SRAM design underneath. The generated SRAMs have clock synchronous write/read operations and pseudo dual-port addressing. They are implemented in the LP (Low Power) version of the technology and are designed to be radiation tolerant to reduce excessive power leakage due to TID (Total Ionizing Dose) and to minimize the impact of SEE (Single Event Effects) in the memory address decoding circuitry. An additional challenge for these SRAMs is to keep the power consumption to a minimum whilst maintaining the radiation tolerance.

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Session Classification: Radiation Hardened Technology for Mixed-Signal IC

Track Classification: AMICSA 2014