FAIR, a front-end ASIC for infrared detector readout

Netherlands Institute for Space Research

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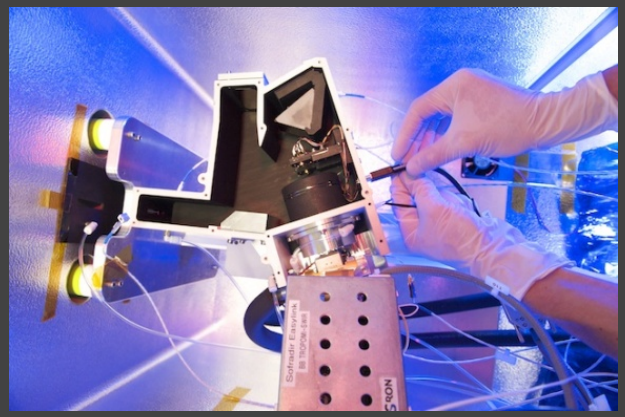
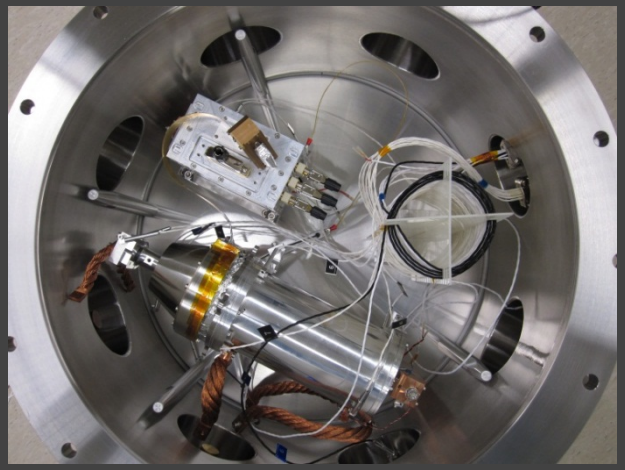
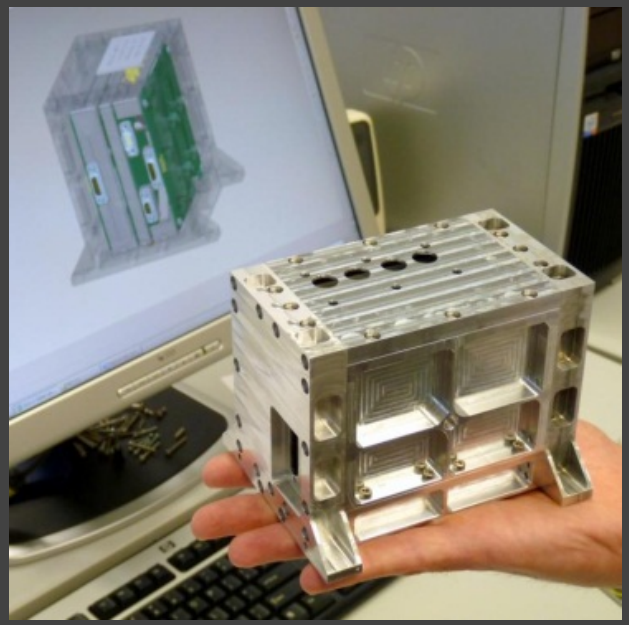
Our heritage: Tropospheric Monitoring (Tropomi) UVN-SWIR instrument







SRON heritage from Tropomi: Essential parts to be integrated in ASIC

NOT YET INTE GRA TED

YES INTE GRA TED

Vendor-specific

Digital Clocking &Pixel Addressing

Not at 55K due to dissipation

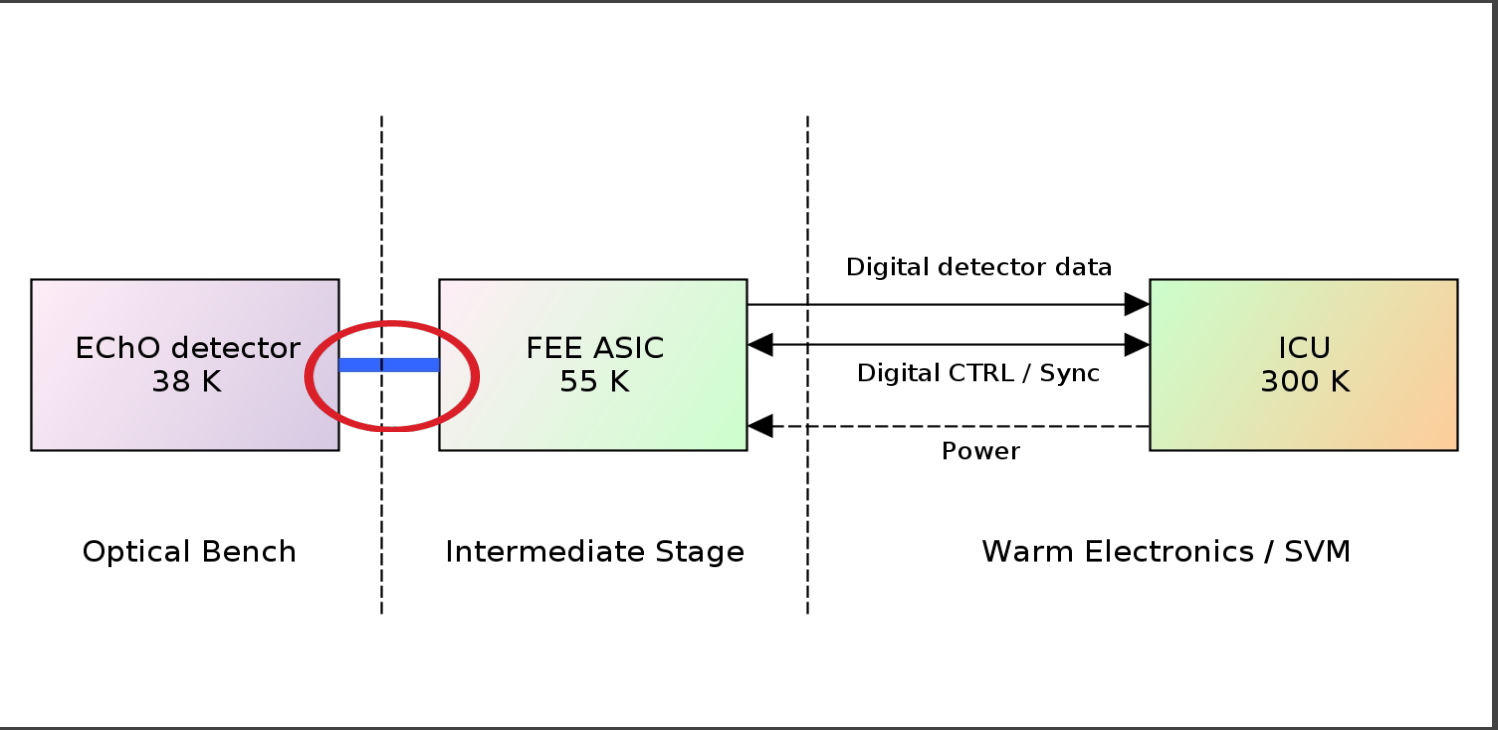
Power regulators

Gain Offset subtr. ADCs

Bias/ ref. Voltage regulators

To be integrated in phase 1

Cryogenic electronic front-end @ 55 Kelvin



- Close proximity, optimum signal integrity
- Low EMI pickup for sensitive analog signals - **EMI risk mitigation**
- Low-power operation @ 55 Kelvin

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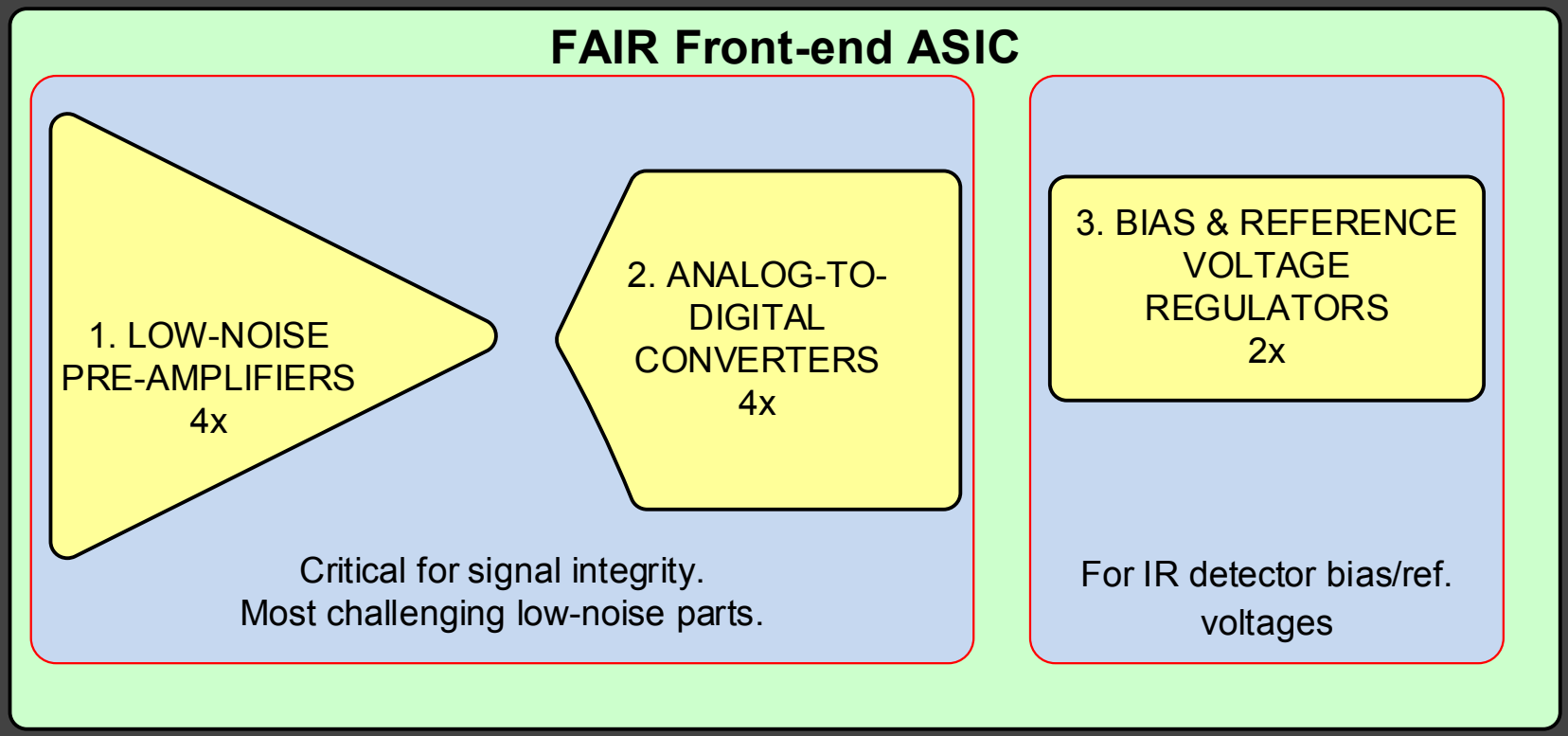
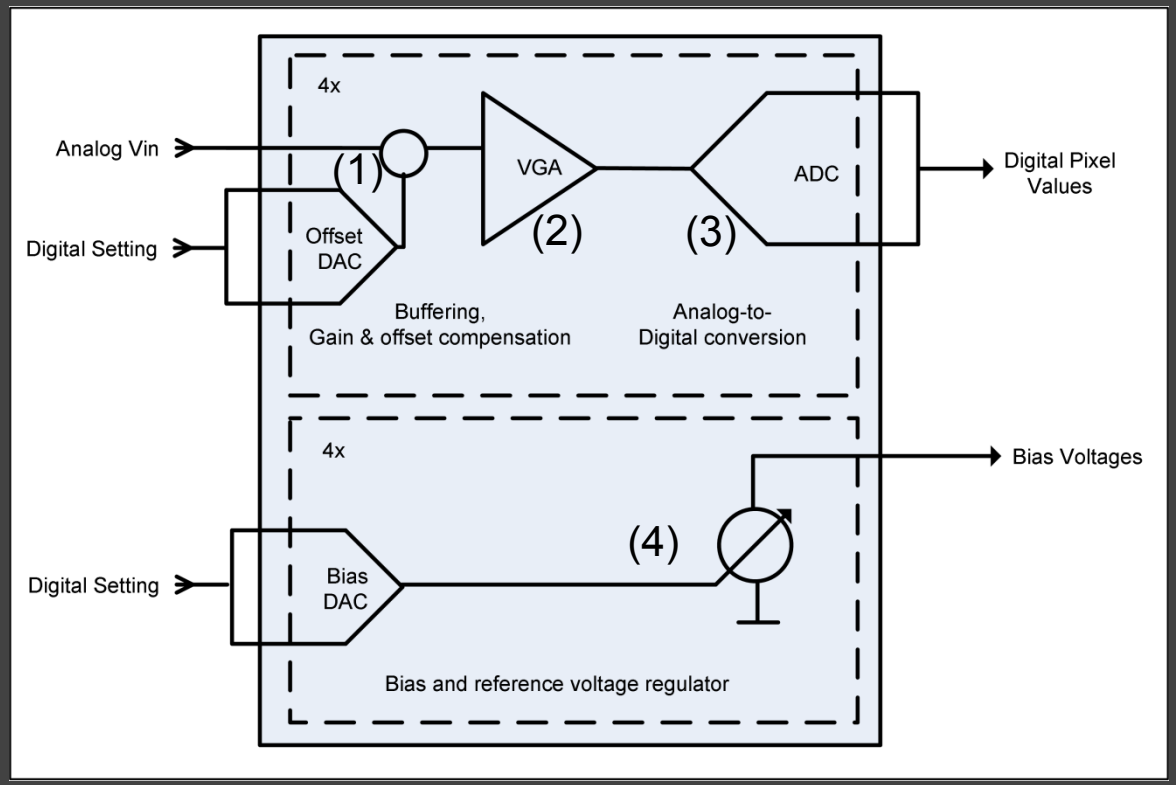
Front-end ASIC for InfraRed detector ('FAIR')

- Goal: 'broad compatibility' EU detectors:
  1st: **Sofradir (Saturn)** detector chip



All-in-one front-end ASIC



- (1) offset subtraction ~1V
- (2) variable gain amplifier (VGA) 0dB..18dB (1x..8x)
- (3) 16-bit A-to-D conversion @ 1MS/s
- (4) bias / reference voltage regulators

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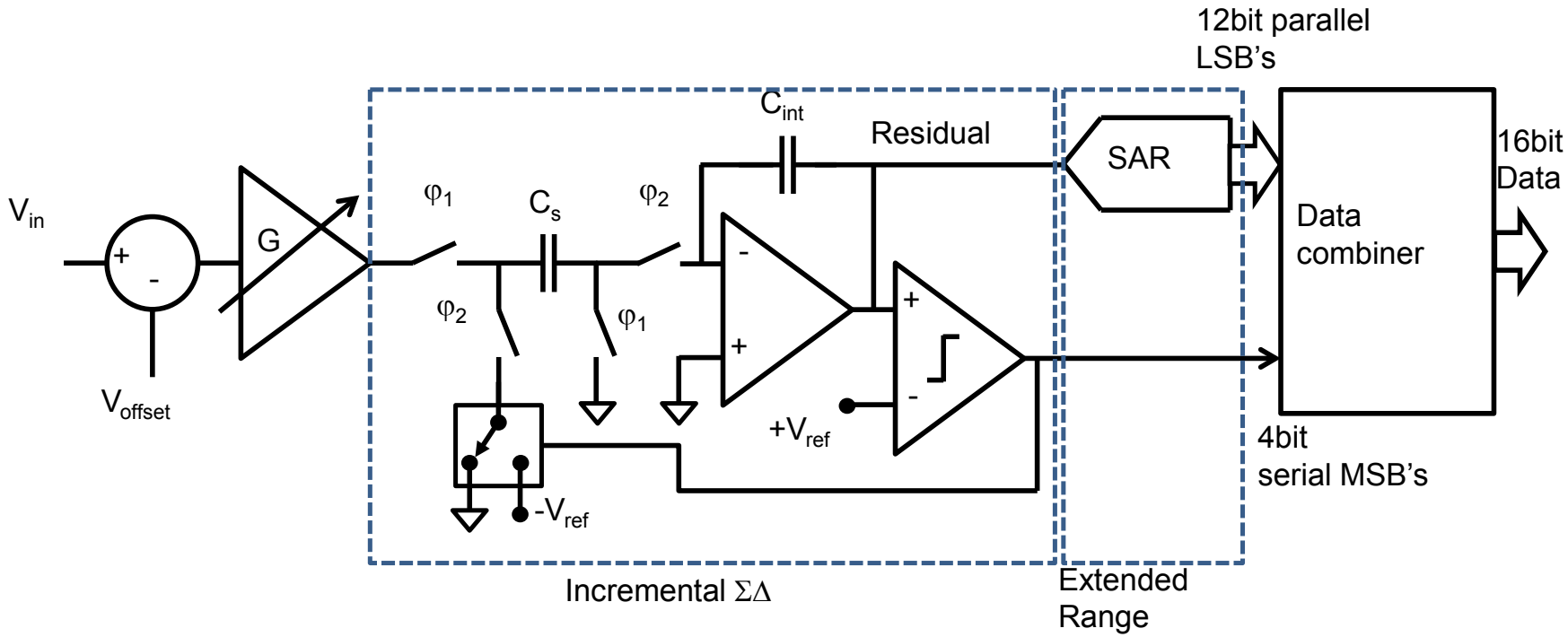
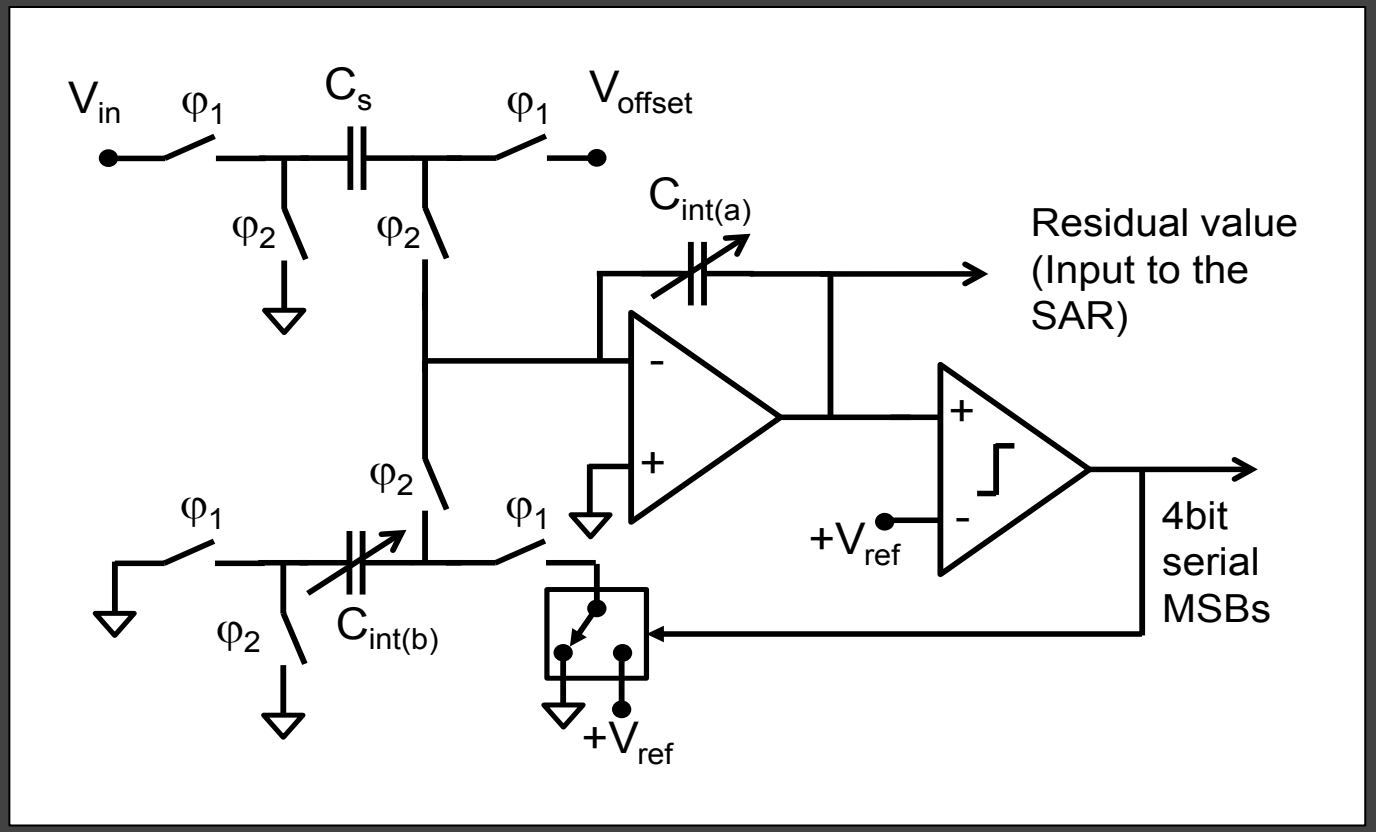
Front-end key technical specifications

Technology	UMC 0.18um CMOS
Supply voltage	3.3V (analog) 1.8V (digital)
Operating temperature range	40K - 328K
Analog front-end	
No. of independent front-end chains	4
Gain settings	1x, 2x, 4x 8x
Offset compensation range	0.5..3V
Offset DAC resolution	24 bits
Analog input voltage range	0V..3V
Analog input capacitance	12-16pF
Analog-to-digital converters (ADC)	
ADC sampling frequency	1.0 MHz
Analog bandwidth	500kHz
Resolution	16 bits
Effective number of bits (target)	15 ENOBs
Bias and reference voltage generators	
No. of independent regulators	2
Output bias/ref voltage range	0 .. 2.8V
DAC resolution	24 bits
Max current	2mA

Architecture of analog signal processing chain



Incremental sigma-delta front-end circuit with gain and offset cancellation



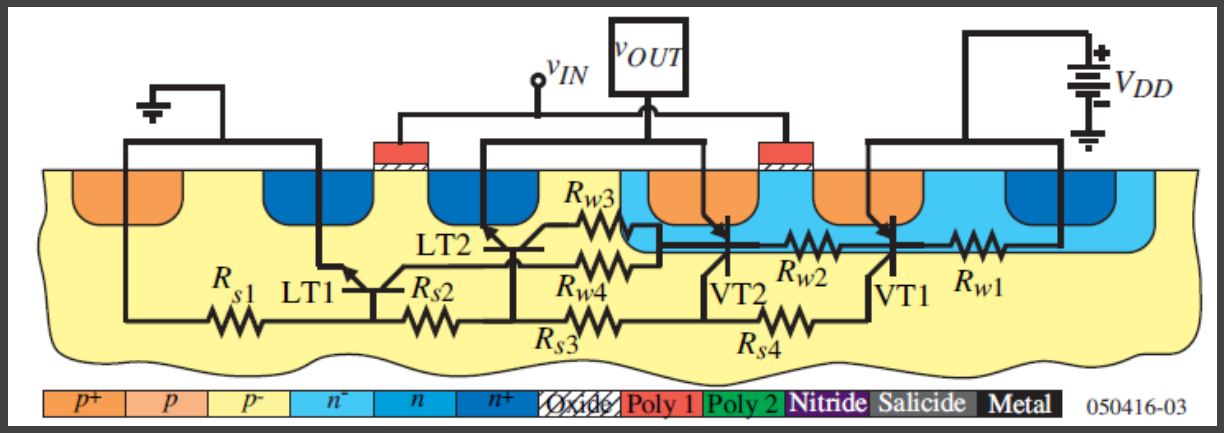
Radiation hardening

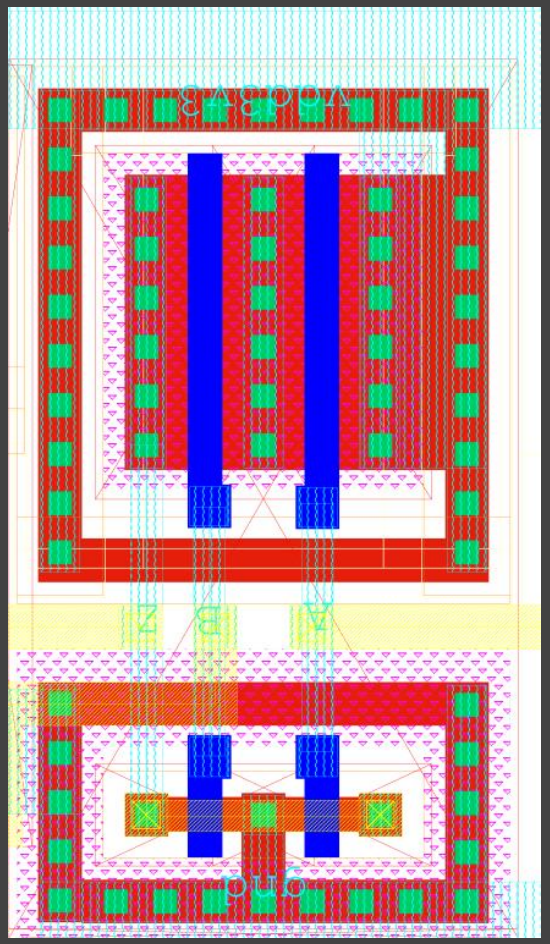
Analog

- Guard rings mitigate latchup of parasitic NPN-PNP structure

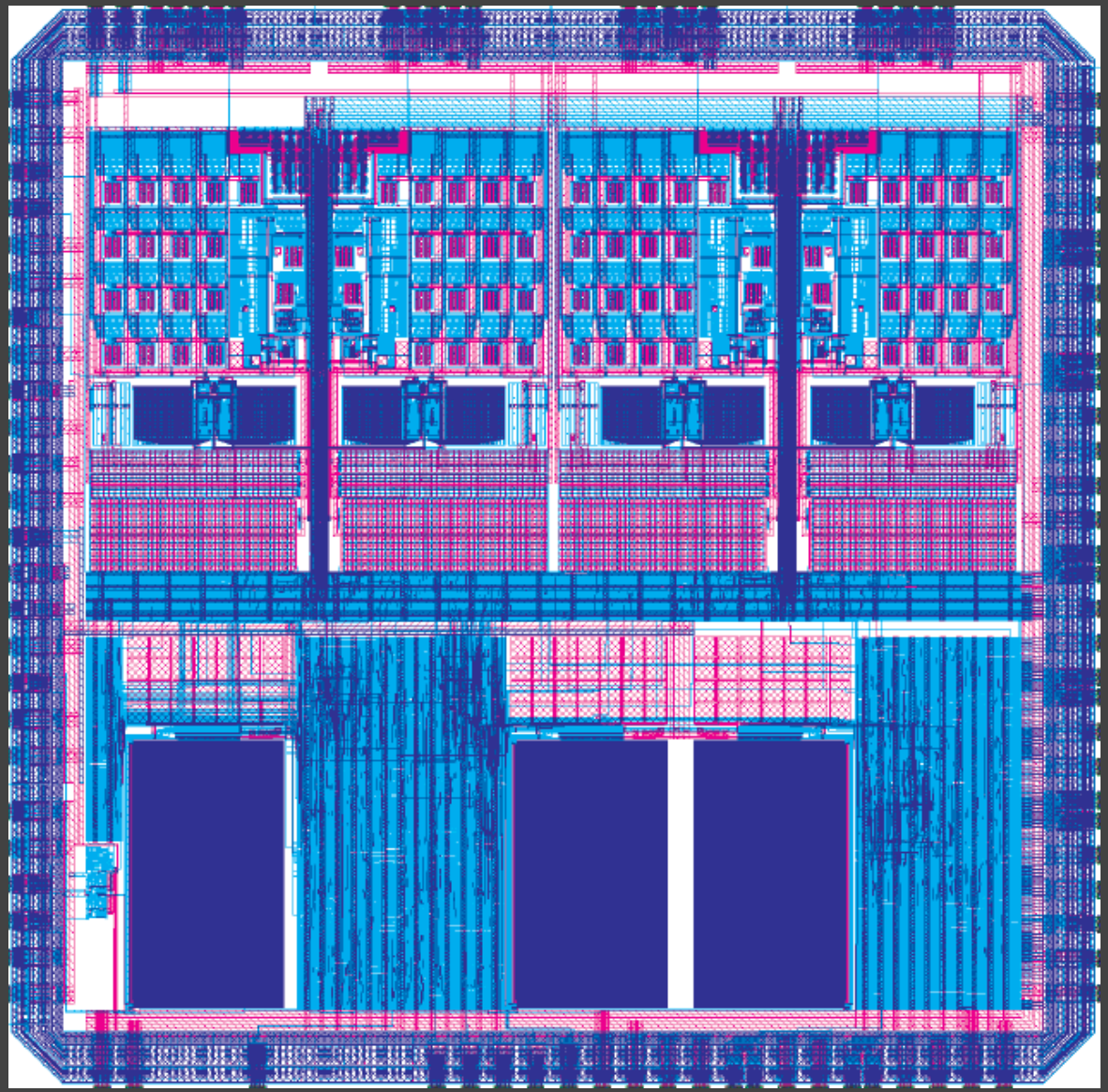
Digital

- Rad-hard IMEC DARE library





GDS of the complete design



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Project timeline

- Project started Q4 2012
- Design phase finished
- Tape-out was March 2014
- Packaged chips expected no 7th July
- Next up: test campaign!
- Mid 2015 >TRL 5

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Conclusions

FAIR:

Front-end ASIC for Infrared detector Readout

European read-out ASIC for IR detectors

- 0.18µm CMOS
- Close proximity, optimum signal integrity
- ADC:
  - 16-bit
  - 1 MSample / s
  - 16mW
  - 2mm^2
- Low-power operation @ 55 Kelvin
- Space qualified, rad-hard analog layout

Netherlands Space Office

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Thank you…

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