

ARQUIMEA

Passion for Technology



innovations
for high
performance

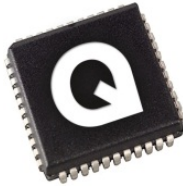
microelectronics

Use of IHP's 0.25 μm BiCMOS Process in the Development of European LVDS Devices*

 AMICSA 2014 – CERN – GENEVA – SWITZERLAND

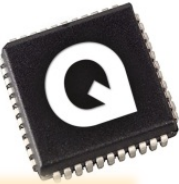
*EUROPEAN LVDS DRIVER DEVELOPMENT (ESA CONTRACT N°. 4000105866)

Outline



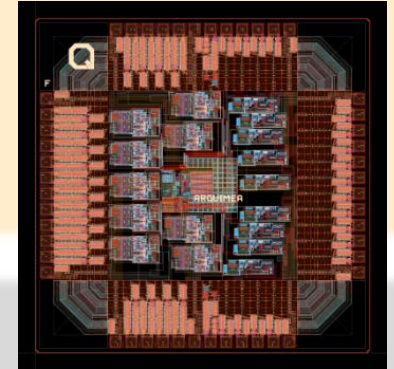
- ARQUIMEA / RAD HARD microelectronic products and services
- News!
- Introduction
- LVDS Octal Repeater
- Circuit Implementation
- Radiation Hardening
- Simulation Results
- Experimental Results
- Conclusions and Future Developments
- AOB

ARQUIMEA / RAD HARD MICROELECTRONIC PRODUCTS AND SERVICES



MIXED-SIGNAL ASICs & IPs

- Deep submicron **digital, analogue and mixed-signal** design and radiation hardening. **SMART POWER.**
- IP design, back-end and integration.
- ASICs Project Management (**full supply chain**).



TECHNOLOGY CHARACTERISATION

- Process or custom devices characterization (electrical and radiation test)

FPGAS

- Space FPGAs design and implementation as per ECSS-Q-ST-60-02

STANDARD COMPONENTS

- Development of rad hard standard components for space (LVDS, ANALOGUE MULTIPLEXORS, ADC's, DAC's, ...)

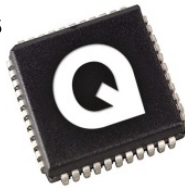
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NEWS!

ARQUIMEA & IHP become partners in Space microelectronics

Rad-hard processes, libraries and IPs for digital, RF, analogue & mixed-signal design



Rad Hard Technologies available for MPW & Small Volume Production (under ESA & DLR evaluation)

SGB25RH

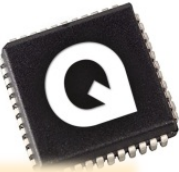
A cost-effective technology with a set of RF npn-HBTs up to a breakdown voltage of 7 V

SG13RH

A high-performance 0.13 μm BiCMOS with npn-HBTs up to $f_T/f_{\text{max}} = 250/300$ GHz, with 3.3 V I/O CMOS and 1.2 V logic CMOS

STEP	OUTPUT	CONTACT
1. Design Kit Access Service	PDK (basic/enhanced)	IHP/ ARQUIMEA
2. Support to Design	VHDL/NETLIST + SCHEMATIC	ARQUIMEA
3. Support to Analogue Layout	VHDL/NETLIST + SCHEMATIC + LAYOUT	ARQUIMEA
4. Support to A/D Integration	GDSII FILES	ARQUIMEA
5. Automatic Test Pattern Generation	TEST PATTERNS	ARQUIMEA
6. Netlist	NETLIST	ARQUIMEA
7. Place & Route	GDSII FILES	ARQUIMEA
8. Analogue Layout	ANALOGUE LAYOUT	ARQUIMEA
9. Analogue + Digital Integration	GDSII FILES	ARQUIMEA
10. DRC + LVS Checks	GDSII FILES VERIFIED	ARQUIMEA
11. Manufacturing	CHIPS	IHP
12. Assembly & Test	TESTED PARTS	ARQUIMEA
13. Delivery	PARTS & DOCUMENTATION (including CoC)	ARQUIMEA

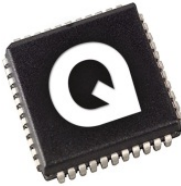
ARQUIMEA Projects



MIXED-SIGNAL ASICs & IPs

- **ELSA**: Mixed signal housekeeping and conditioning device for **Hispasat AG1 REDSAT** active antenna to be launched in 2015.
- **DETECTA**: High Speed Acquisition chain and ADC (>1 Gs, 10bit) based on IHP 0.13um (2010).
- **Cosmic Vision HF & MF**: Configurable mixed-signal ASIC for Cosmic Vision Instrumentation Payload, for the following applications: CCD signal, processor, Radiation detector, Radiation spectrometer, ADC, DAC, Filter, Low noise amplifier, Power amplifier. Two devices at high frequency and medium frequency are under development (2010).
- **European LVDS devices**: Development of European Rad Hard LVDS device family (2012).
- **RadHARQ**: Development of rad hard digital library and radiation detectors based on IT380 technology (2013).
- **SWIPE**: Development of a radiation detector (TID, SEU) for moon lander application (2013).
- **CARTU**: Development of a medium frequency 13-bit ADC (2013).

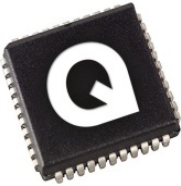
Introduction



- Video, photo, high speed links, telemetries, ... space systems use very high data rates.
- Data links have to be:
 - Fast
 - Reliable
 - Low Power
 - Low EMI
 - Low Cost



LVDS (Low Voltage Differential Signal) is used for **intra-spacecraft high speed** communications.



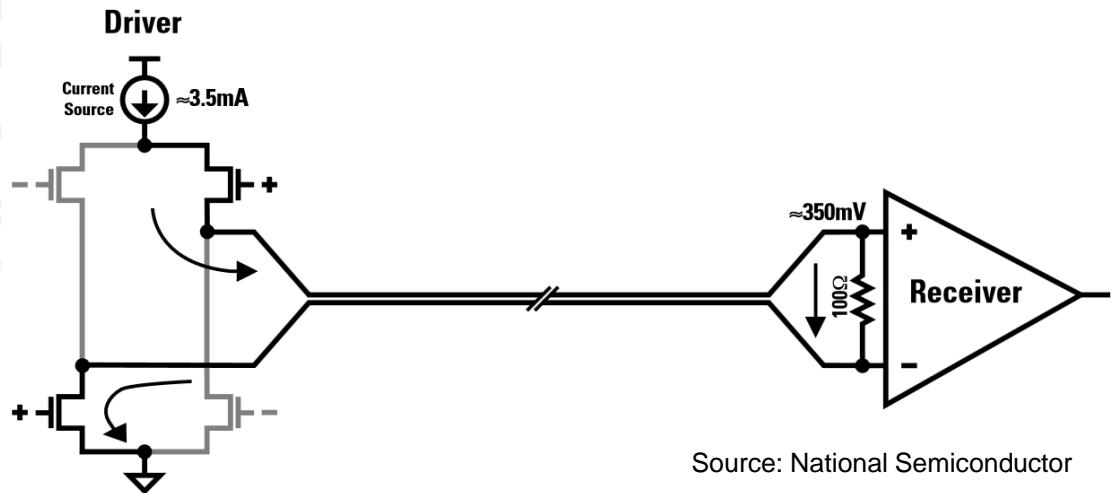
LVDS (Low Voltage Differential Signaling)

- Low Voltage Differential Signaling comprises the following advantages:

- High Data Rate
- Low Power
- Low EMI emissions
- High Noise Rejection
- Low Cost

- Its main characteristics are:

- Differential
- Low voltage: $\pm 350\text{mV}$
- Common Mode Voltage: 1.2V
- Rise/Fall times: 260ps minimum.
- High Data Rate (655 Mbps max. ANSI/TIA/EIA-644 standard).



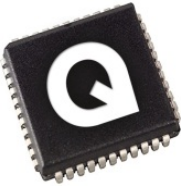
$$V_{OH} = 1.375\text{V}$$

$$V_{CM} = 1.2\text{V}$$

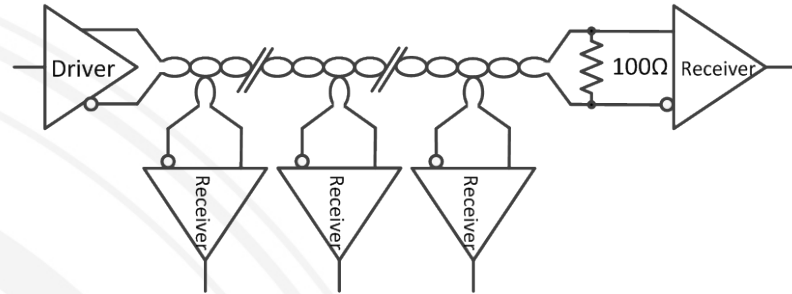
$$V_{OL} = 1.025\text{V}$$



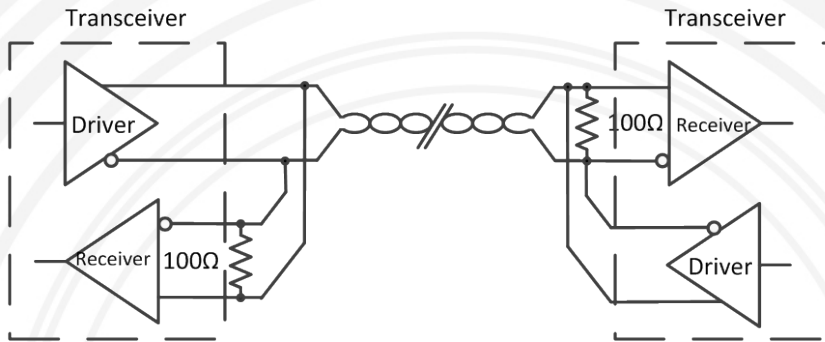
LVDS Topologies



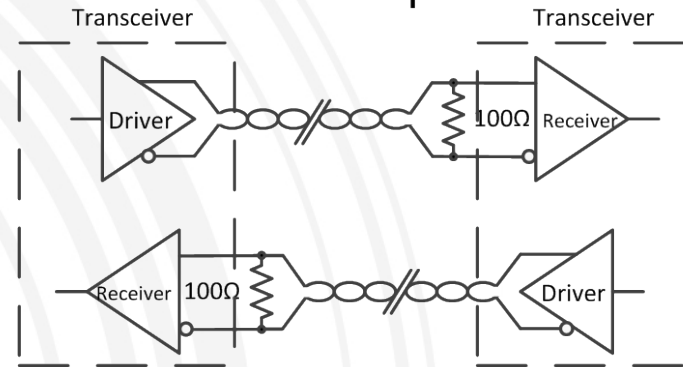
Point-to-Point



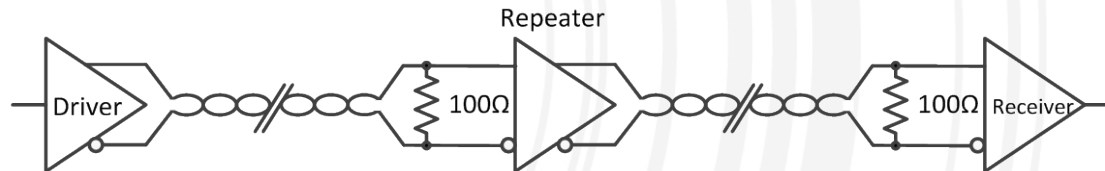
Multidrop



Bidirectional Half-Duplex

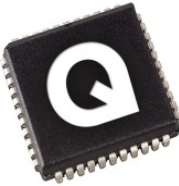


Bidirectional Full-Duplex



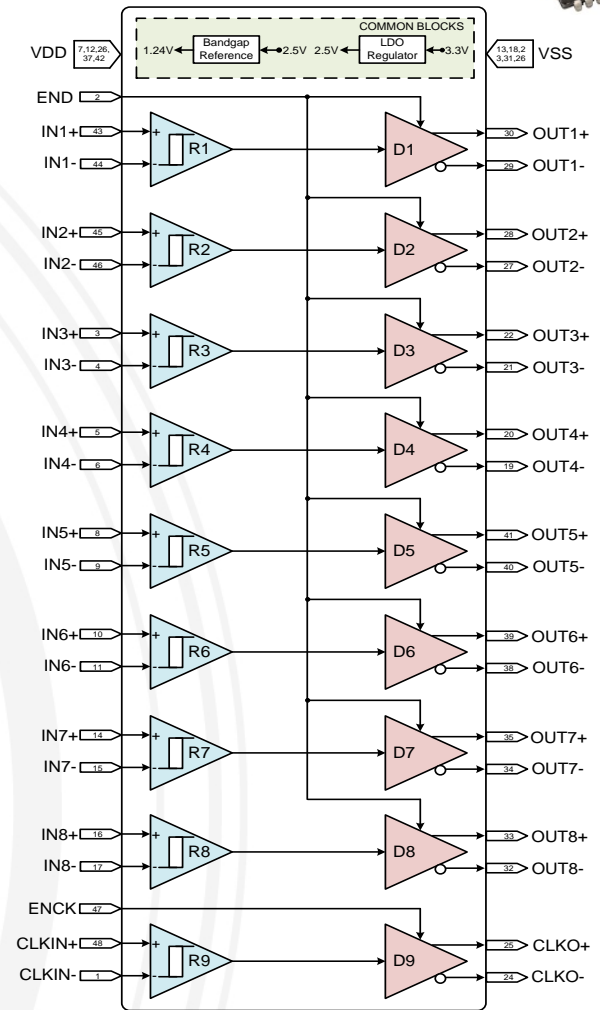
Long Harness Point-to-point including repeater

LVDS Octal Repeater



- Full ANSI EIA/TIA 644A compliance.
- Eight Data channels.
- One clock channel.
- Data channels enable pin.
- Clock channel enable pin.
- Tri-state driver capability.
- **>500 Mbps data rate (250 MHz).**
- Single 3.3 V Supply.
- Extended temperature range (-55°C, +125°C).
- Integrated voltage reference.
- **Extended input common mode for LVDS inputs (-4V, +5V).**
- Extended maximum absolute rating for LVDS inputs (-5V, +6V).
- TTL compatible digital inputs.
- Small channel delay, <2.7 ns typical, <3.5 ns over full temperature range.
- Low peak-to-peak jitter <236 ps ($\pm 3\sigma$).
- Low channel to channel skew <150 ps typical, <250 ps over full temperature range.
- **8 kV HBM ESD enhanced protection.**
- Fail-Safe functionality included.
- **Cold Spare functionality.**
- Radiation Hardness higher than **300 kRad (Si)** TID with ELDRS and SEL immune up to 60 MeV cm²/mg LET.
- CQFP48 package.

LVDS Octal Repeater Block Diagram



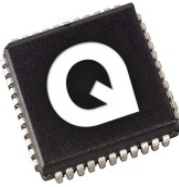
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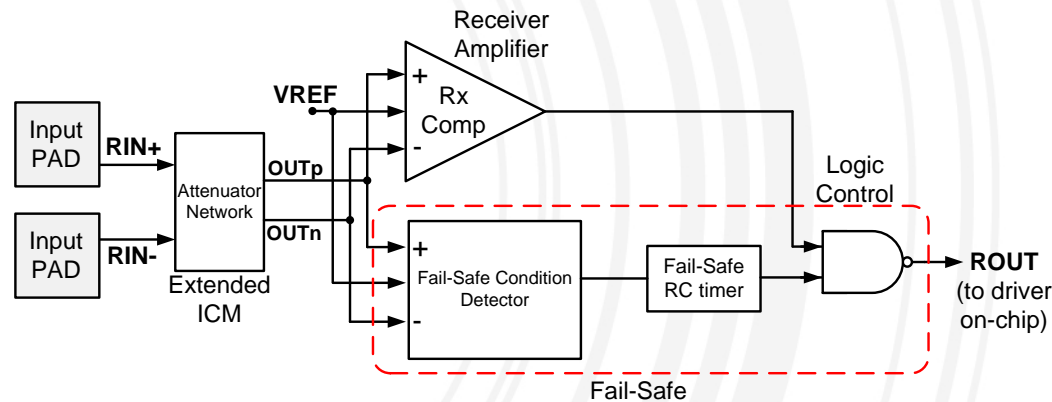
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Circuit Implementation



■ Receiver

- Frequency compensated Attenuation network
- Rail-to-rail high speed Comparator
- Fail-Safe Detector
- Fail-Safe 500ns RC timer
- Allows extended input common mode range from -4V to +5V
- Cold Spare inputs

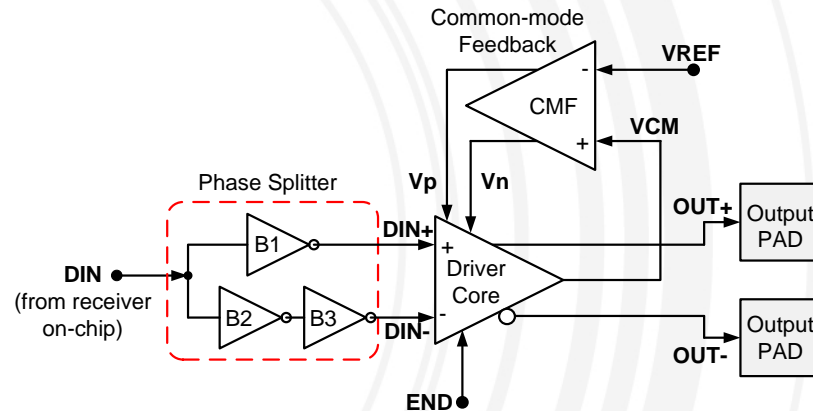


Circuit Implementation

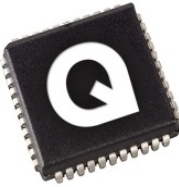


■ Driver

- Phase Splitter
- Driver Core
- Common Mode feedback amplifier
- Designed to achieve minimum **at least 500Mbps** data rate
- Cold Spare outputs



Circuit Implementation



■ Bandgap

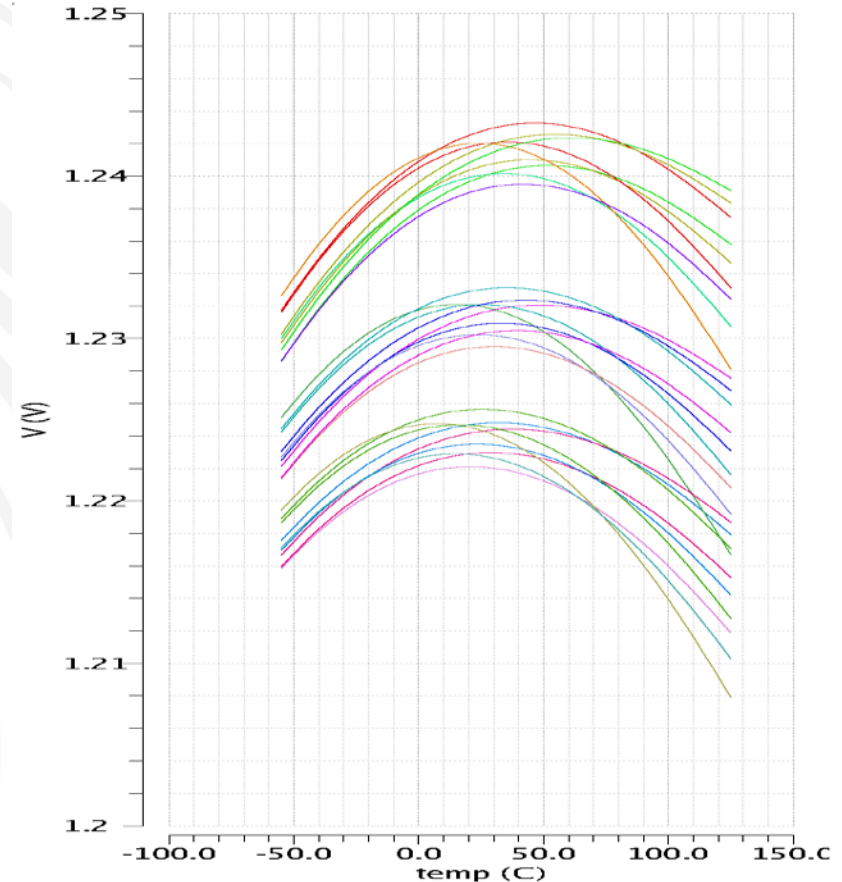
- 1.25V internal bandgap reference
- First order compensation

■ Voltage Reference

- LDO regulator
- 3.3V input voltage
- 2.5V output voltage (core voltage)

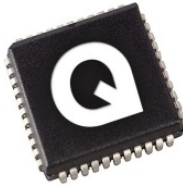
■ 8 kV HBM ESD pads

- Custom made ESD protections and pads for 8kV ESD and 250V MM.



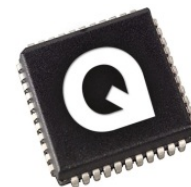
Bandgap output voltage across corner variations

Radiation Hardening

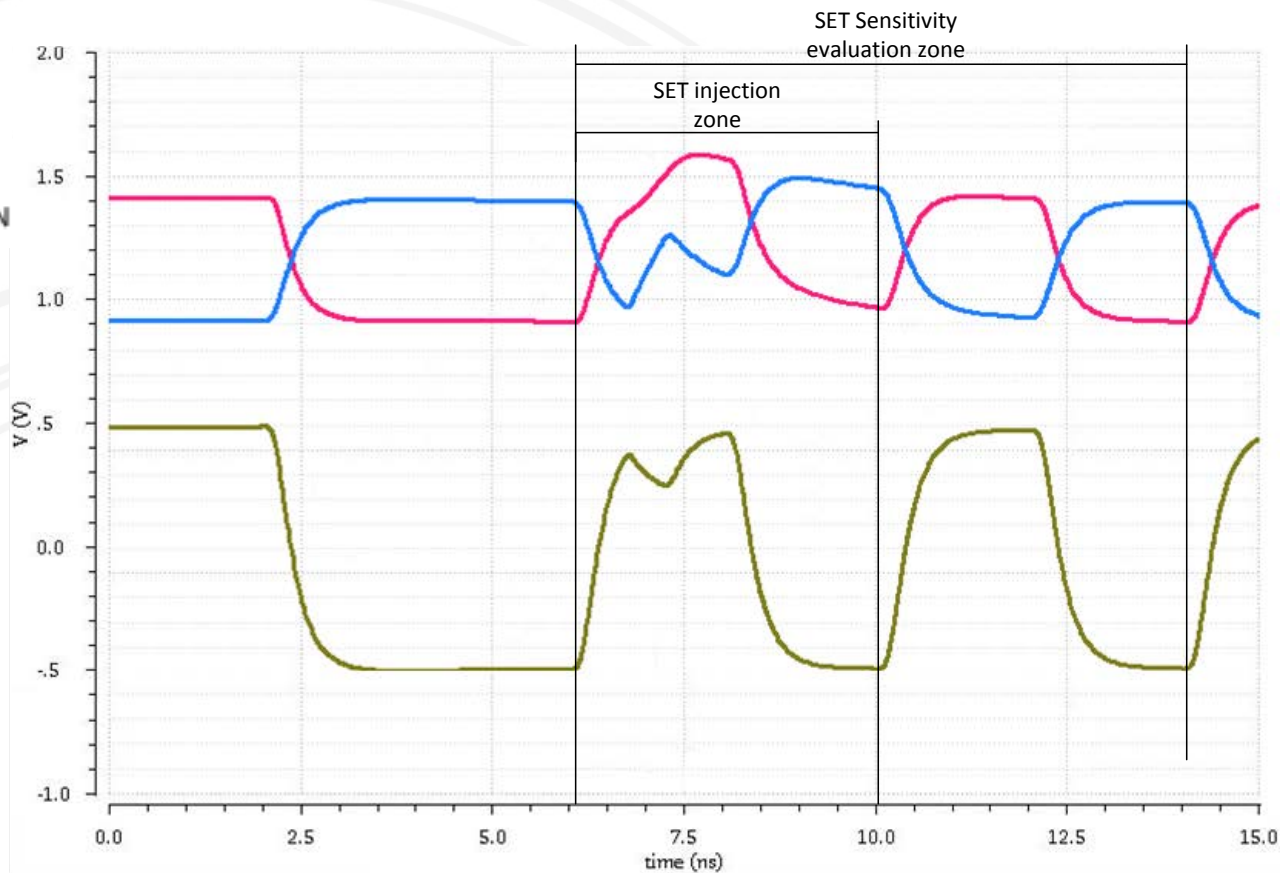


- Expected radiation performance of IHP SGB25RH (from previous radiation data):
 - Expected SEL immune > 60 MeV cm²/mg
 - Immunity up to 300 kRad for high and low dose rates
- Several techniques were used to improve radiation hardness (in addition to Rad Hard DRC design kit rules) including its application to custom digital cells.
 - High W/L or ELT layout for NMOS devices.
 - Systematic guard ring isolations or triple-well isolation.
 - Differential design.
- SET sensitivity has been evaluated using specific software tools (developed by *Grupo de Ingeniería Electrónica*, from *Universidad de Sevilla*).

Radiation Hardening – SET simulation

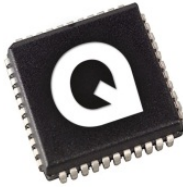


- Out_P
- Out_N
- Out_P- Out_N

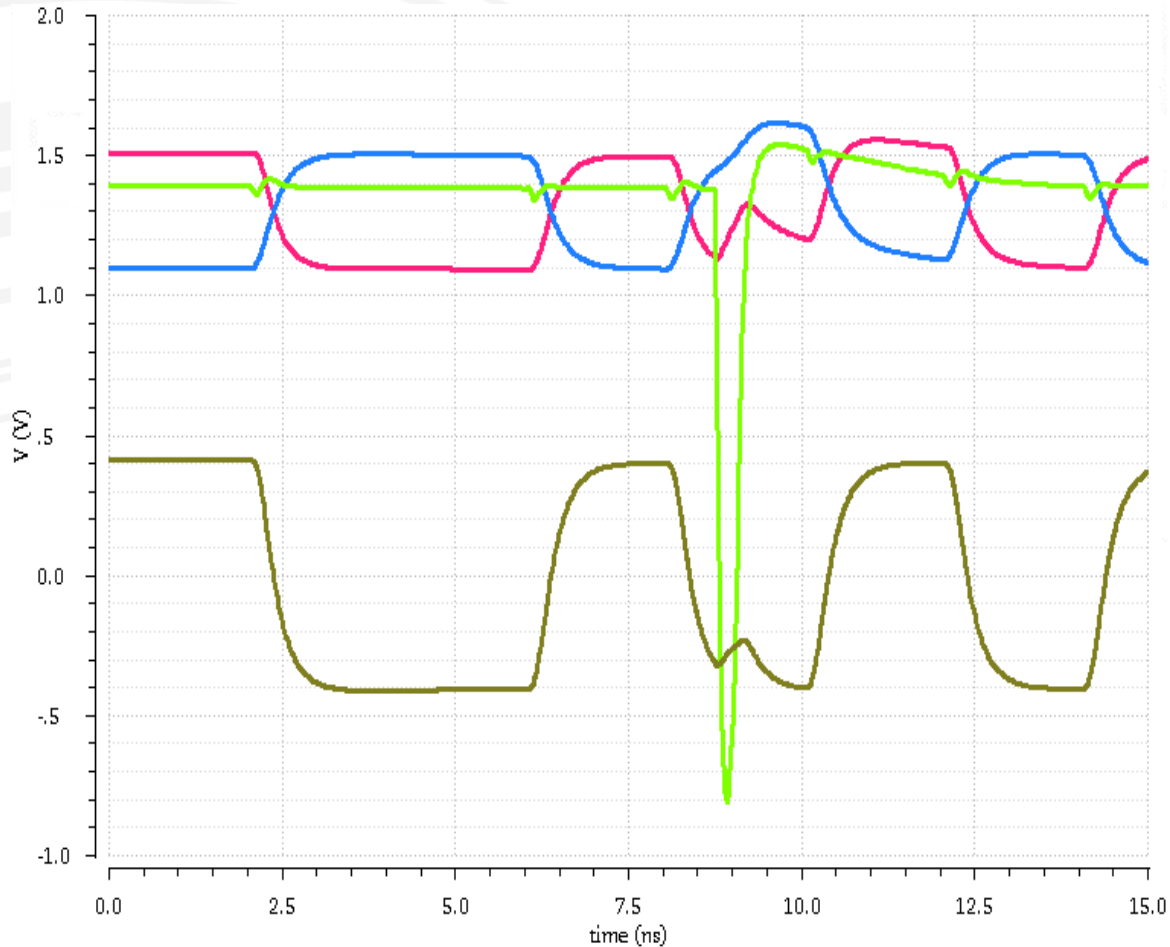


Example of SET injection in the driver core circuitry

Radiation Hardening – SET simulation

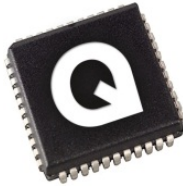


- Out_P
- Out_N
- Out_P- Out_N
- $(Out_P+Out_N)/2$



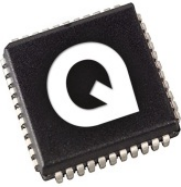
Example of SET injection in the driver common mode feedback.
Driver CMRR avoids bit flip at the LVDS output.

Simulation Results

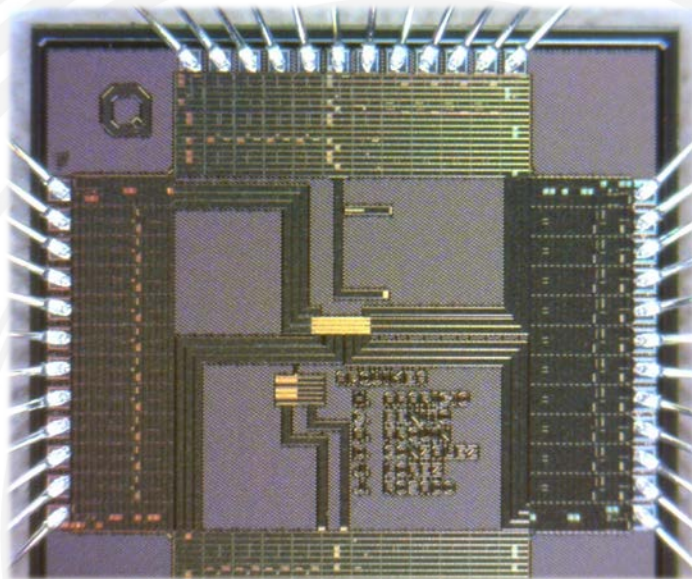


- Extensive extracted view simulations have been performed over:
 - Full temperature range,
 - Process corners,
 - Supply variations.
- Results:
 - Full ANSI EIA/TIA 644A compliance.
 - Minimum Data Rate: 500 Mbps (can go up to 728Mbps), with extended common mode (-4V to +5V).
 - Small Channel delay: 2.7ns
 - Low channel to channel skew: 150 ps
 - Cold Spare, tri-state and fail-safe functionality verified.

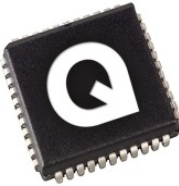
Chip implementation



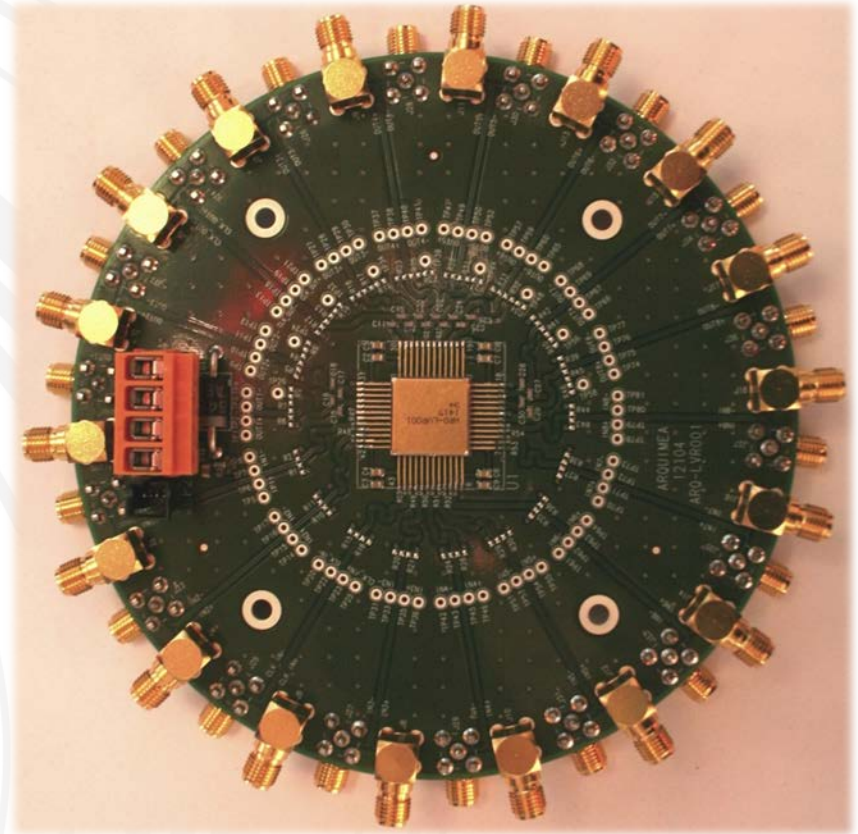
- IHP SGB25RH (MPW)
- Die size: 2x2 mm².
- Package: CQFP48
- (by MICROSS)



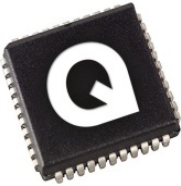
Test activities



- ESD testing has been performed by IHP achieving more than 7.3kV for all pads (limited by the test equipment capability).
- Full electrical characterization in July 2014
- Radiation tests expected in September 2014 (for TID and heavy ions) by ALTER Technology.

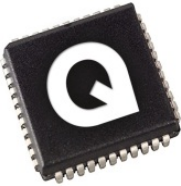


LVDS Octal Repeater Test Board



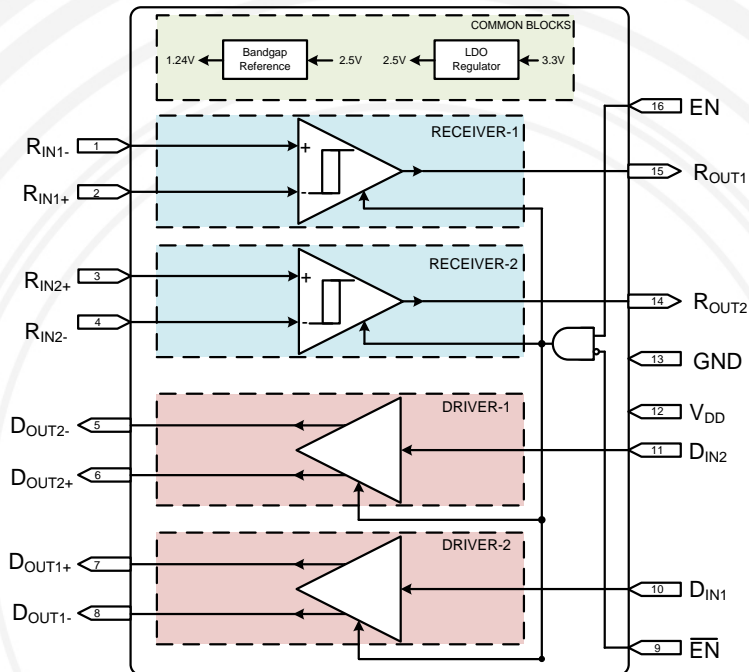
Conclusions

- A radiation hard, Octal LVDS repeater has been designed and manufactured.
 - Full ANSI EIA/TIA 644A compliance.
 - Minimum Data Rate of 500 Mbps (can go up to 728Mbps), with extended common mode (-4V to +5V).
 - Small Channel delay of 2.7ns
 - Low channel to channel skew of 150 ps
 - Cold Spare, tri-state and fail-safe functionality verified.
- Full electrical characterization and radiation testing ongoing.
- A full evaluation/qualification of the device it is expected to be performed in the next project phase.

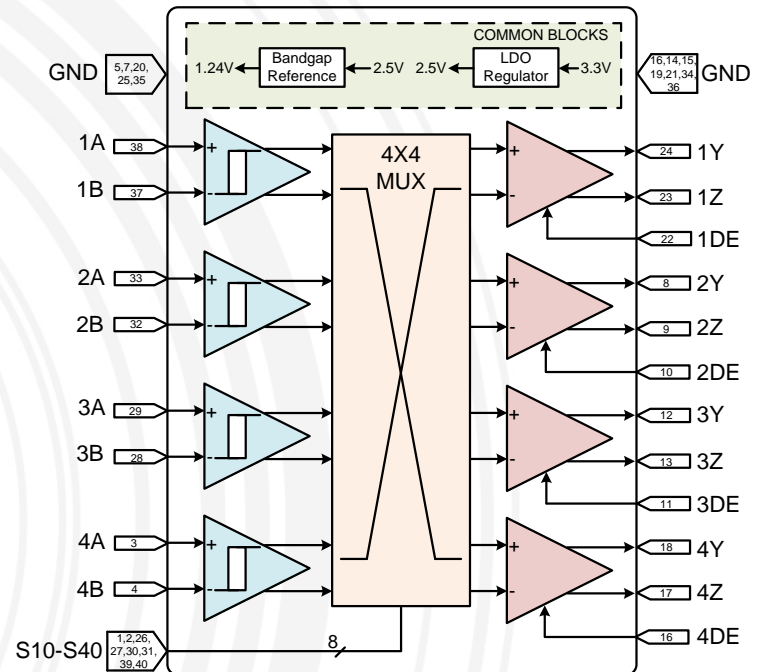


Future Developments

- A complete family of LVDS devices: driver, receiver, transceiver and crosspoint switch, with equivalent performances to the octal repeater, are under development by Arquimea as a continuation of this work.



Transceiver Block Diagram



Crosspoint Switch Block Diagram



for your attention...



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[arquimea_026](#)

ARQUIMEA



Microelectronics; Actuators; Space Electronics

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D E U T S C H L A N D



Microelectronics: Digital Design, Back-End & Test Services

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