Use of IHP's 0.25 µm BiCMOS Process in the Development of European LVDS Devices

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Abstract

Transmission of large amount of data is extensively used in communication among spacecraft and satellite onboard systems during a mission. LVDS (Low-Voltage Differential Signaling) Drivers and Receivers are key to provide means of sending/receiving data along twisted pair cables at very high data-rates with low power and excellent EMI performance. Rad-tolerant and Rad-hard ANSI EIA/TIA 644A complaint LVDS Drivers and Receivers products are essential in an extensive range of space applications. Typical applications with such needs are SpaceWire and clock distribution networks.

The purpose of this activity is the development of an LVDS Octal repeater in the frame of ESA's and ECI's European LVDS Driver Development intended to be used in space applications and built in IHP's 0.25-um BiCMOS process technology which has a good performance in terms of radiation, for both total dose and single event effects. Previous tests on this technology show no degradation up to 300kRad of total ionization dose (TID) and a single event latch-up (SEL) immunity up to 60MeV cm^2 mg^{-1} at least.

The key features of the octal LVDS repeater include cold sparing (essential for redundant systems architecture) up to 250MHz signaling rate per channel allowing 500Mbps transfer rates over SpaceWire, 3.3V single power supply, small propagation delay, low channel to channel skew, Tri-state output control, extended common mode on LVDS receivers and the minimum ESD tolerant rating of 8kV for human body model (HBM), 250V for machine model and +/- 500V for field induced charge device model. It also includes failsafe capabilities.

In order to validate and characterize the technology for the extended ESD tolerance an additional test vehicle chip has been built in the frame of the activity, with a set of ESD test vehicles that include NMOS clamps, PMOS clamps, and diodes.

I. INTRODUCTION

The capabilities of remote-sensing instrumentation are developing rapidly. As a consequence the data rates being handled on-board spacecraft are increasing. Photo and video data are a constant in many space missions. This pushes the need of connecting different systems with fast, reliable, low power links and to achieve this, Low-Voltage Differential Signaling (LVDS) addresses the need of high performance data transmission applications. The LVDS standard is becoming the most popular differential data transmission standard in the space industry.

LVDS delivers high data rates while consuming significantly less power than competing technologies. In addition, it brings many other benefits, which include:

- Low-voltage power supply compatibility
- Low noise generation
- High noise rejection
- Robust transmission signals
- Ability to be integrated into system level ICs. LVDS technology allows products to address high data rates in excess of hundreds of Mbps. For all of the above reasons, it has been deployed wherever the need for speed and low power exists.

LVDS is a differential, serial communication link, which uses low voltage differential signals (350 mV_p typ.), generated from a current source that delivers 3.5mA on a 100Ω termination resistor. It uses a typical common mode of 1.2V and limited slew rate to improve electromagnetic emissions. Point-to-point, single driver, single receiver and multipoint topologies, multiple drivers, multiple receivers, are compatible with LVDS devices where tri-state driver capability is present.

In this paper a LVDS octal repeater, with eight data channels plus and additional clock channel is presented. Each channel is made of an LVDS receiver and LVDS driver, with tri-state capability, to allow multipoint topologies. Failsafe feature is also included to ensure a known channel output in case of wiring or external driver failure. It works at a minimum of 500 Mbps data rate, at extended input common mode, with a typical 2.7 ns channel delay and extremely low channel-to-channel skew of 150ps. This repeater has Enable inputs for data and clock channels to set the LVDS outputs into tri-state mode. Cold spare functionality has also been included which means that the device input/outputs do not sink a significant amount of current if voltage is present at the pins while the device is at power off.

II. LVDS Octal Repeater Functionality

The LVDS Octal Repeater developed in the frame of ESA's and ECI's European LVDS Driver Development, has the following characteristics:

- Full ANSI EIA/TIA 644A compliance.
- Eight Data channels.
- One clock channel.
- Data channels enable pin.
- Clock channel enable pin.
- Tri-state driver capability.
- >500 Mbps data rate (250 MHz).
- Single 3.3 V Supply.
- Extended temperature range (-55ºC, +125ºC).
- Integrated voltage reference.
- Extended input common mode for LVDS inputs (-4V, +5V).
- Extended maximum absolute rating for LVDS inputs (-5V, +6V).
- TTL compatible digital inputs.
- Small channel delay, <2.7 ns typical, <3.5 ns over full temperature range.
- Low peak-to-peak jitter <236 ps (±3σ).
- Low channel to channel skew <150 ps typical, <250 ps over full temperature range.
- 8 kV HBM ESD enhanced protection.
- Fail-Safe functionality included.
- Cold Spare functionality.
- Radiation Hardness higher than 300 kRad (Si) TID with ELDRS and SEL immune up to 60 MeV cm2/mg LET.
- CQFP48 package.

III. Circuit Implementation

The block diagram of the circuit is presented in

Figure 1. It consists of nine channels, each of them using a LVDS driver and a LVDS receiver. In addition an integrated reference voltage and a linear regulator have been included.

A. *Receiver*

The receiver uses high frequency, high gain, rail-to-rail comparator to detect the LVDS differential signals present at the channel inputs. In order to accommodate the extended common mode range at the input, a frequency compensated attenuation network is placed at the input of the receiver. This reduces the signal to noise ratio of the signal, which makes the comparator design more complex. Fail-Safe circuitry is also included, which sets the output of the receiver in case an input is floating or the inputs are shorted together for more

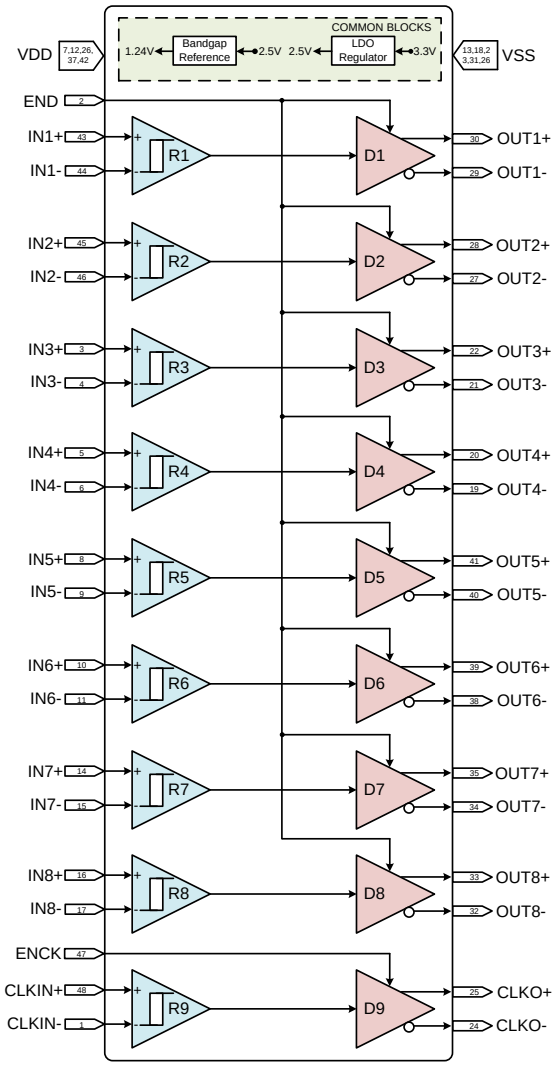

Figure 1. LVDS Octal repeater block diagram.

than 500ns. A fail-safe condition detector block checks when this condition is present and turns on an RC timer, than triggers after 500ns, setting the output of the receiver at high level, through a NAND gate.

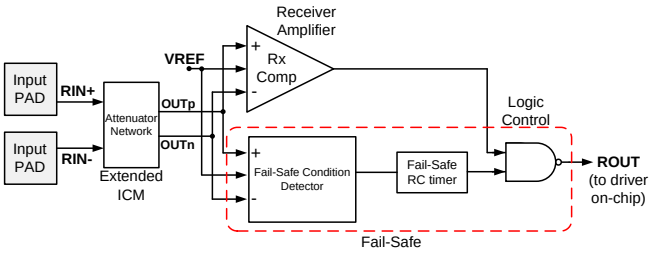

Figure 2. LVDS Receiver block diagram.

B. *Driver*

The driver consists of a driver core which generates the output currents (±3.5mA typ.) for the LVDS signals. The driver core has two current sources, which can be switched to sink or source current depending on the input level. The current levels are modified by the common mode feedback

loop in order to ensure the output voltage levels remain within certain limits that ensure that the common mode voltage is appropriate. The stability of the common mode loop is ensured by a minimum phase margin of 60º. The driver core is design to achieve a minimum data rate of 500Mbps.

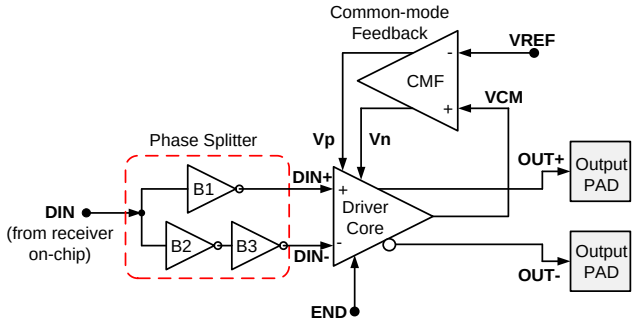

Figure 3. LVDS Driver block diagram.

The driver outputs have been designed to stand cold sparing. The enable input allows setting the output at high impedance.

Figure 4. Driver output at nominal conditions.

C. Voltage Reference

A 1.25V voltage reference has been included to generate the common mode voltages and biasing currents of the device. A first-order compensated bandgap reference was designed.

D. Voltage Regulator

A Low Drop Output voltage regulator is included to allow using a 3.3V supply for a core technology voltage of 2.5V.

E. 8kV HBM Pads

Pads have been designed, including full custom devices, to achieve a minimum ESD protection of 8kV using a Human Body Model and 250V for Machine Model. These pads include analog input/outputs, power/ground pads and digital input pads. The digital pads were designed to be TTL compatible.

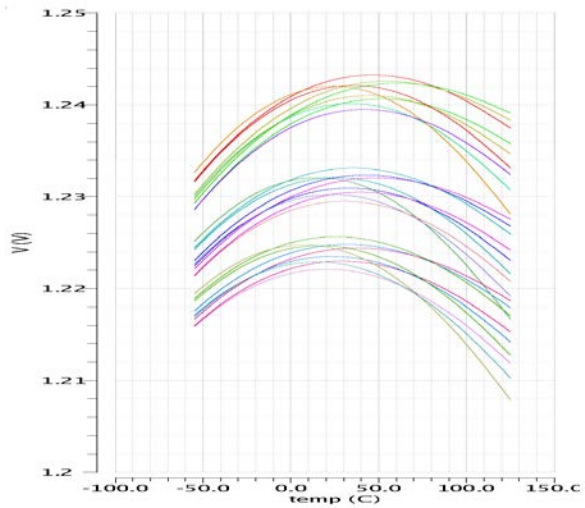

Figure 5. Bandgap output vs temperature in all corners.

F. Hardening by Design

Hardening By Design (HBM) techniques have been extensively used in the device design. Based on IHP SGB25RH technology, with radiation hardness heritage [1][5], techniques like systematic guard rings, custom digital cells, adequate W/L ratios or ELT for MOS transistors layouts among others have been used to achieve to a TID tolerance up to 300 krad(Si) at standard (1 rad/sec to10 rad/sec) and low dose-rate (0.01 rad/sec to 0.1 rad/sec). No bipolar transistors, excepting those used in the voltage reference, are used to improve LDRS. The design has been done to be SEL immune to LET levels higher than 60 MeV cm2/mg. Specific design rules provided by the manufacturer to improve radiation hardness have been used.

The SET sensitivity has been evaluated by the *Grupo de Ingeniería Electrónica*, from *Universidad de Sevilla*, using a proprietary software tool [2]. The tool injects certain charge in different circuit nodes to simulate a particle impact and analyses the transient on the relevant output. The results have mainly shown some sensitivity on certain nodes of the driver block, which in some cases can be outside of the LVDS voltage range, but results have to be correlated with the radiation tests to ensure SET hardness. Particle impacts in the common mode amplifier generate small output transients, due to the high CMRR of the driver. Transients at the output of the bandgap and the regulator have very little effect on the LVDS outputs, and no spurious glitches have been detected at the receiver output due to heavy ion impacts.

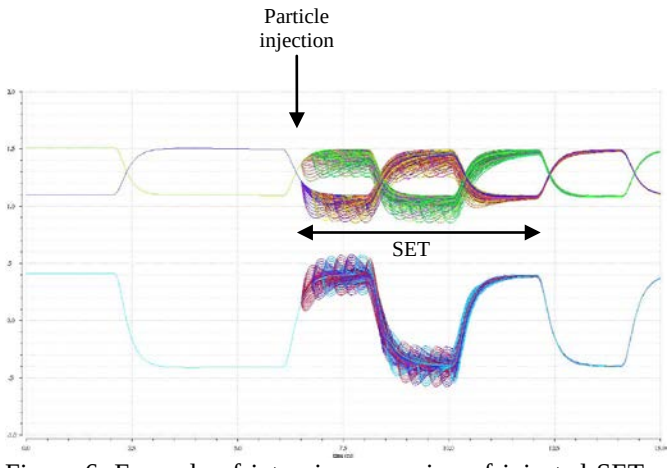

Figure 6. Example of intensive campaign of injected SETs at LVDS outputs and differential signal shown.

IV. Simulation results

The device has been extensively simulated in post layout, achieving full compliance with ANSI EIA/TIA 644A [3]. All simulations have been performed in the -55ºC up to +125ºC temperature range, including process and power supply variations when needed. The minimum data rate of 500 Mbps has been obtained, with an extended common mode of -4V to +5V. Small channel delay, lower than 3.5 ns and low channel to channel skew of 226ps have been achieved for worst case conditions. Cold sparing, tri-state and failsafe functionality have been also verified. The rise/fall times of the driver output are 412ps for a 1pF differential load [3], allows achieving a theoretical simulated maximum data rate of 728Mbps. The phase margin obtained in the common mode feedback loop is 72º in all conditions ensuring stability. In the regulator the minimum phase margin obtained is 90º. The bandgap has a minimum phase margin of 51º in worst case condition and 60º for typical ones.

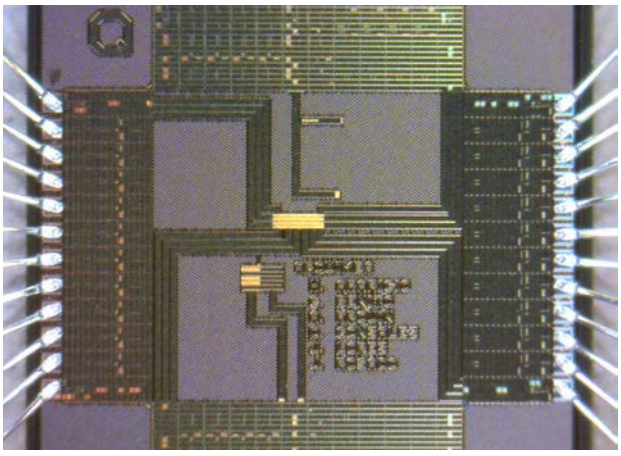

Figure 7. LVDS Octal Repeater die.

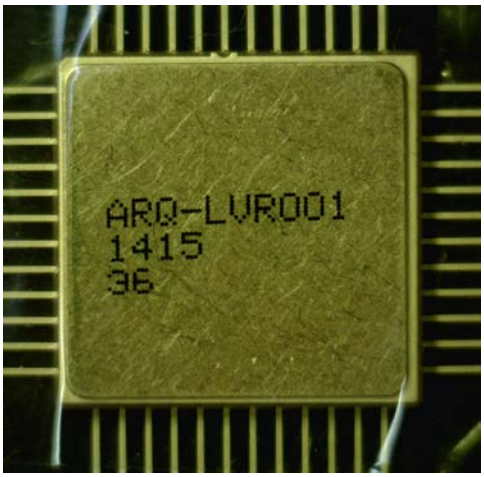

Figure 8 CQFP 48 Octal repeater package

V. Experimental results

The device has been implemented in a die of 2.06x2.06 mm^2, on IHP SGB25RH. A compact, low inductance, ceramic CQFP48 package has been used, to minimize channel to channel skew. ESD testing has been performed by IHP achieving more than 7.3kV for all pads, being the maximum voltage limited by the test equipment capability. Transmission Line Pulse technique has been used to perform the ESD testing.

Full temperature electrical characterization and radiation testing against TID and heavy ions is being performed by ALTER, not being finished at the time this paper is being published.

VI. Conclusions and Future Developments

A radiation hard, Octal LVDS repeater has been designed and manufactured, showing a minimum data rate of 500 Mbps, small channel delay of 2.7 ns and low channel to channel skew of 150 ps. All this has been verified by extensive post layout simulations, over temperature, process and power supply variations. Full electrical characterization and radiation testing is being performed at the time this paper is being published. A theoretical simulated maximum data rate of 728 Mbps could be achievable.

A complete family of LVDS devices: driver, receiver, transceiver and crosspoint switch, with similar performances to the octal repeater, is under development by Arquimea as a result of this work.

A full evaluation/qualification of the device it is expected to be performed under an ESA contract.

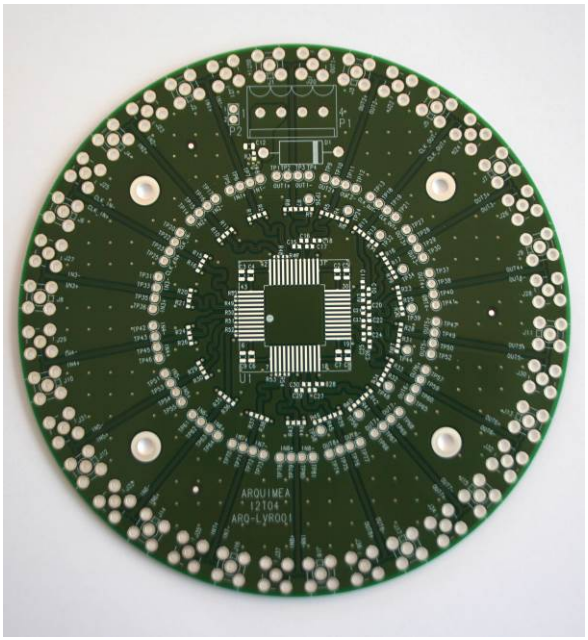

Figure 9 LVDS Octal repeater test board

ACKNOWLEDGMENTS

We would like to acknowledge the support of ESA for the Development of European LVDS Devices, on which this paper is based. We appreciate the assistance of the IHP team, René Scholz, Milos Krstic, Vladimir Petrovic and Florian Teply. For the design of the ESD protections, the support from Sofics, in particular from Bart Keppens and Olivier Marichal has also been appreciated.

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