High performance analog Front End ASIC for interfacing with a Si Drift Detector and the control electronics

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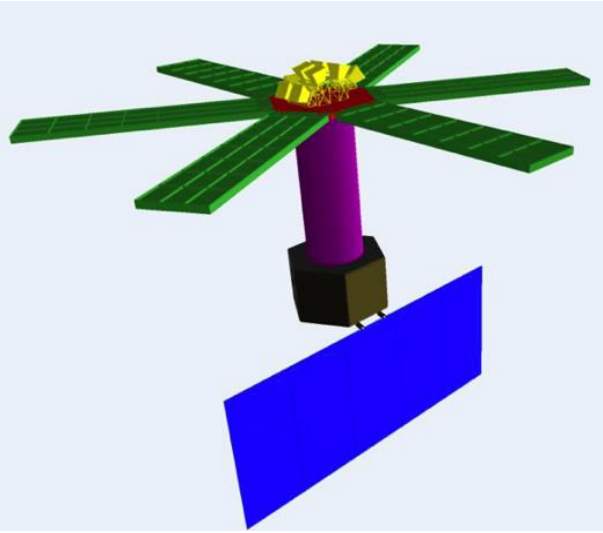
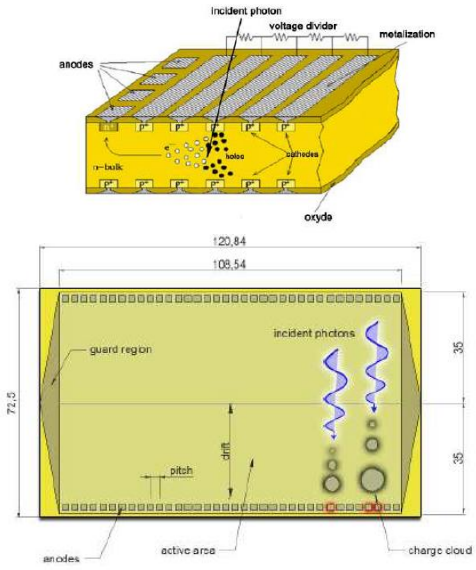
Context of the project: LOFT requirements

LOFT (Large Observatory For x-ray Timing) was dedicated to the study of strong field gravity and the equation of state of dense matter for mission M3

Loft payload
At the top of the structural tower (purple) the 6 panels of Large Area Detector - LAD (green) and in the center the 6 cameras of Wide Field Monitor - WFM (yellow) over the optical bench (red)



Context of the project: LOFT requirements - Si Drift Detector



LAD and WFM are based of X-ray sensitive large area Silicon Drift Detectors (SDD)

The project targets a 10 m² detector array for 2 to 80 keV Xrays detection at high sensitivity (50 – 200 eV) and good energy resolution (limited by electronic noise, itself limited by EOL detector leakage current) with a dead time << 1% at 1 Crab.

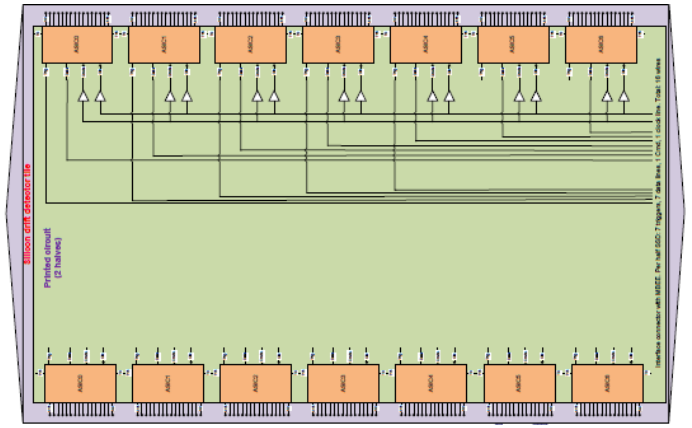
Such a system will require 500 k to 600 k SDD detectors managed by 35 k to 40 k ASICs.

A LAD detector has 112 anodes on each side.

16 detection chains are implemented in each ASIC

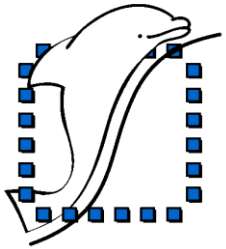
14 ASICs are glued on the rear side (seven per detector side).

Each ASIC has a SPI like interface with the Module Back End Electronics (MBEE)



Project organization

The collaboration among IRAP, CNES and Dolphin Integration targeted these ASICs interfacing the SDDs and the digital back end on the satellite. Stringent requirements on the noise performance were dictated by the low-energy threshold of the WFM (50 eV) and the spectral resolution of the LAD (200 eV at 6 keV at -30° C).



Analog and mixed-signal
Mixed-signal ASIC design
Custom Fabless products

cnes
CENTRE NATIONAL D'ÉTUDES SPATIALES

Instrument requirements
Space environment expertise

irap
astrophysique & planétologie

Application knowledge
Test expertise
System design

Dolphin Integration

- Founded in 1985
- Enabler of Mixed-signal Systems-on-Chip through silicon IP offering and ASIC/SoC design services
- Listeded as ALDOL on Alternext of NYSE in 2007
- 200 employees, including 135 Design Engineers
- now active from 180 nm down to 28 nm
- ISO-9001:2008 certified
- 2 subsidiaries for product development: Laval (Canada) – Power Management, Netanya (Israël) – Register Files
- 4 domains of activity:
  - Silicon IP provider offering flexible configurations:
    - **High Resolution Audio** Subsystems
    - **High Resolution Measurement**
    - **Low-power storage** Subsystems
    - Low-power Microcontrol
    - **Innovative libraries** of Standard Cells and Memory Register
    - Power Regulation, Reference, Clock & Detector Networking
  - EDA Solutions:
    - **Mixed-signal simulator SMASH**, "All-in-One"Schematic editor SLED for graphic entry and design configurations in a shorter time
    - Mixed-signal power consumption estimator SCROOGE TLA
  - SoC Integration and Custom Fabless Services: Dolphin offers **25 years of experience in circuit design, SoC layout and application competency.** Mastery of major EDA stages, especially testability, with a special emphasis on simulation to ensure circuit launches right-on-first- pass.
  - Design services: on-site at customers

2011 TSMC IP Partner Award for Analog/Mixed-Signal IP

Sirius odyssey: challenges

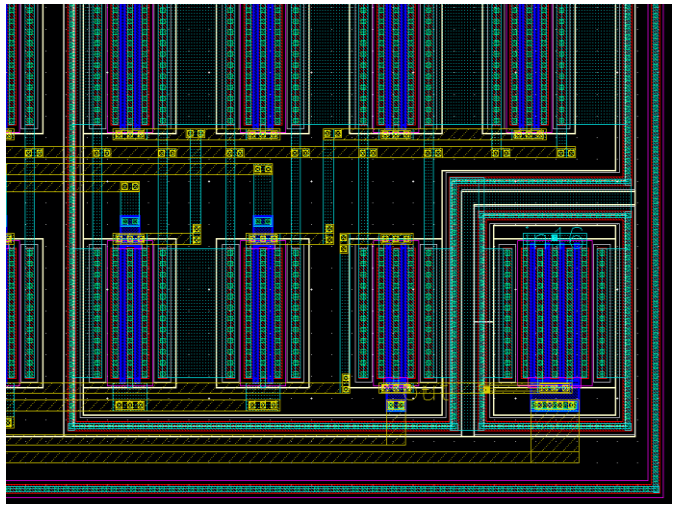
	State-of-the-art 2012	SIRIUS 1 - TESTCHIP Q1-2013	SIRIUS 2 - ASIC Q2-2014
Input charge range	500 eV – 50 keV	200 eV – 80 keV	200 eV – 80 keV
ENC (at -30° C)	< 30 electrons rms	< 20 electrons rms	< 20 electrons rms
EOF leakage current of the SDD	< 2 pA	< 10 pA	< 10 pA
Shaping peak time	1-10 µs programmable	2-8 µs programmable	2-8 µs programmable
ADC resolution	9-10 bits		13 bits
Dead-time	Not available	0.7 %	0.7 %
Baseline restoration	Not available	50 µs	50 µs

Sirius odyssey: radiation challenges

The total radiation dose expected on the LOFT orbit is low, so there is no need for a hardened technology. The ASIC was designed using some layout mitigation techniques to reduce the SEU effects and to increase the LET:

- guard ring around the various functions
- ring of the opposite polarity around transistors when NMOS and PMOS transistors are closed
- increased distance of active zone from the pads when they are connected to a pad
- …

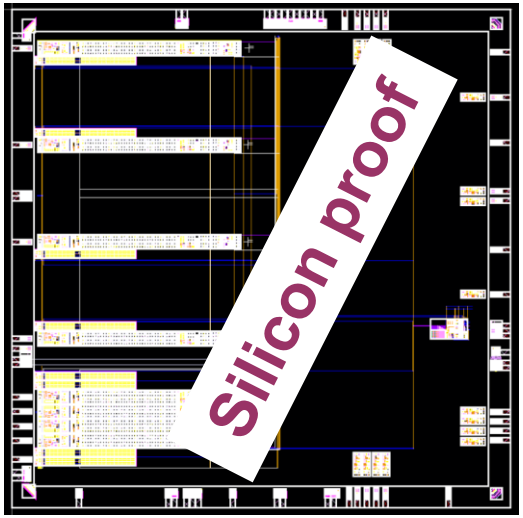
Detail of the layout showing the rules (rings) used to reduce the susceptibility to latch-up



Sirius odyssey

SIRIUS 1 (25 mm²)

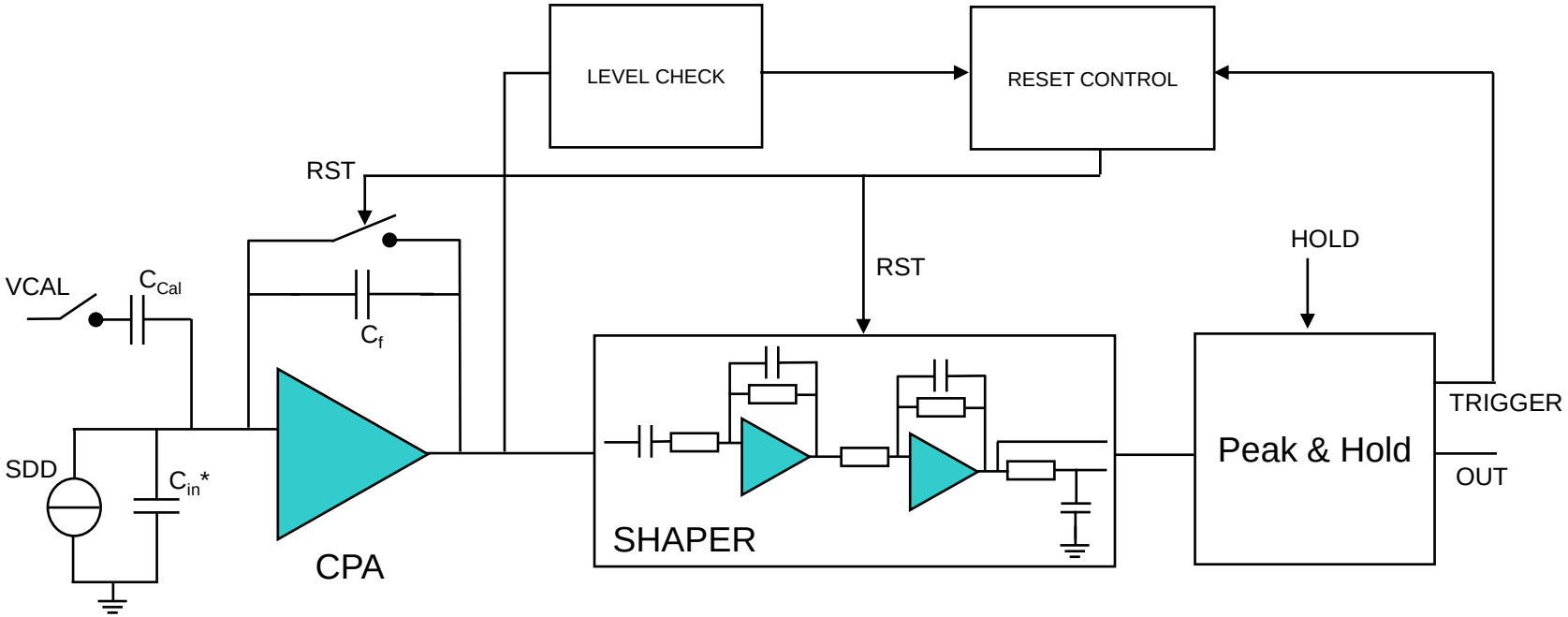
- 4 LADs + 4 WFMs
- Analog design for test
- Consider Spatial constraints on 600 km-orbit:
  - 1 krad radiation and latchup immunity
  - - 55° C functionality
  - - 30 ° C full performances



SIRIUS 2 (60.2 mm²)

- 16 LADs
- interface with the Front End Electronics
- PGA and 10/12/14 bit ADC
- threshold control (16 x 8 bit DACs)
- calibration DAC (5 bit)
- reference band gap
- Analog design for test for a set of channels

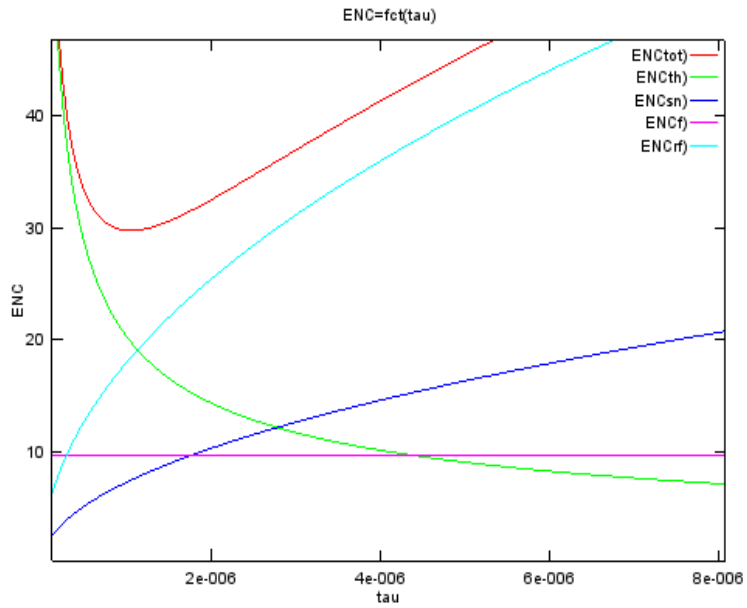
SIRIUS1/2: AFE architecture

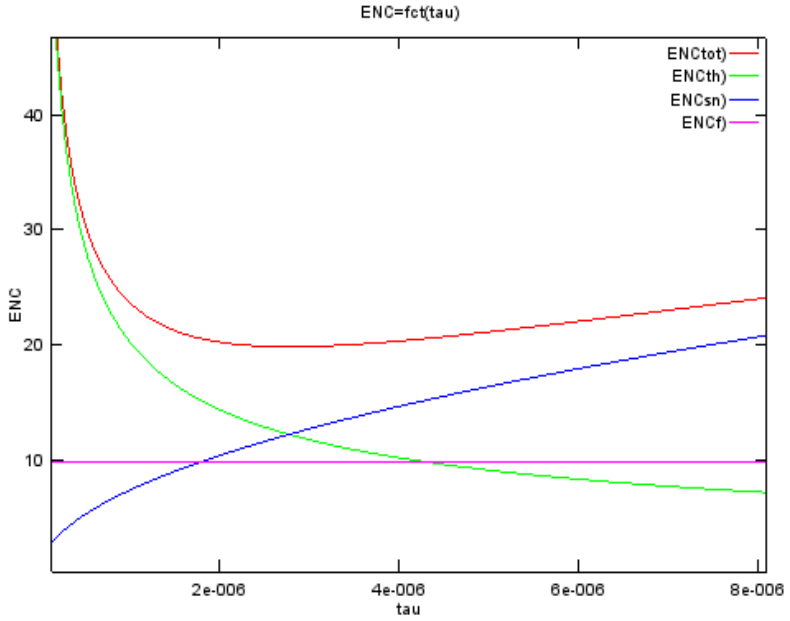


- CPA, Shaper, Peak and Hold, reset control and calibration circuit.
- Calibration circuit is implemented to allow gain calibration, functional and performance testing before coupling with the detector.
- Outputs of each CPA and each shaper can be buffered for testing purpose.

SIRIUS1/2: Noise consideration

$$ENC_{total} = \sqrt{(ENC_{th} + ENC_f + ENC_{Rf} + ENC_{sn})}$$





Simulation showing the noise performance as a function of τ (switched reset, 10pA SDD leakage, τ in s). ENC_{tot} (red) is the square root of the sum of the square of the various ENC (ENC_{th}: CPA thermal noise, green; ENC_{sn}: shot noise due to detector, blue; ENC_f: 1/f noise, violet).

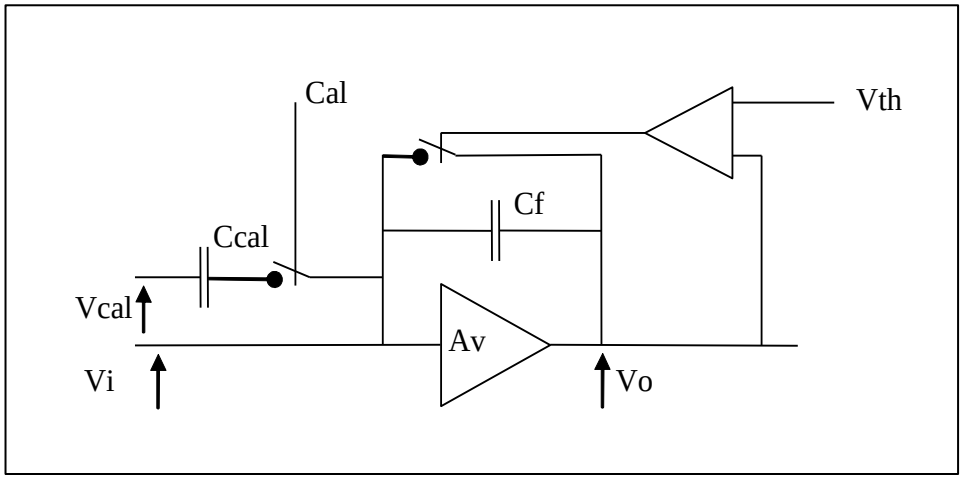
On the left with a Rf of 1.5 Gohms and on the right without Rf

SIRIUS1/2: AFE – CPA conclusions

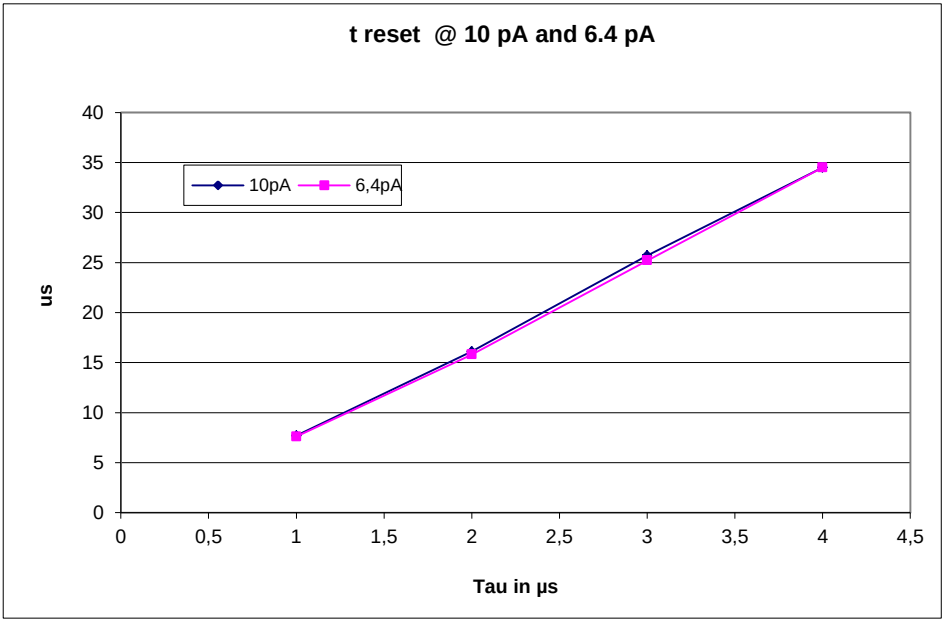
It has been shown that resistance based leaky integrator cannot meet the critical specifications for LOFT project.

A reset circuit has been used to restore the base line after each event and when the baseline drift is such that a threshold is reach. A capacitor is used to inject charges for calibration purpose.

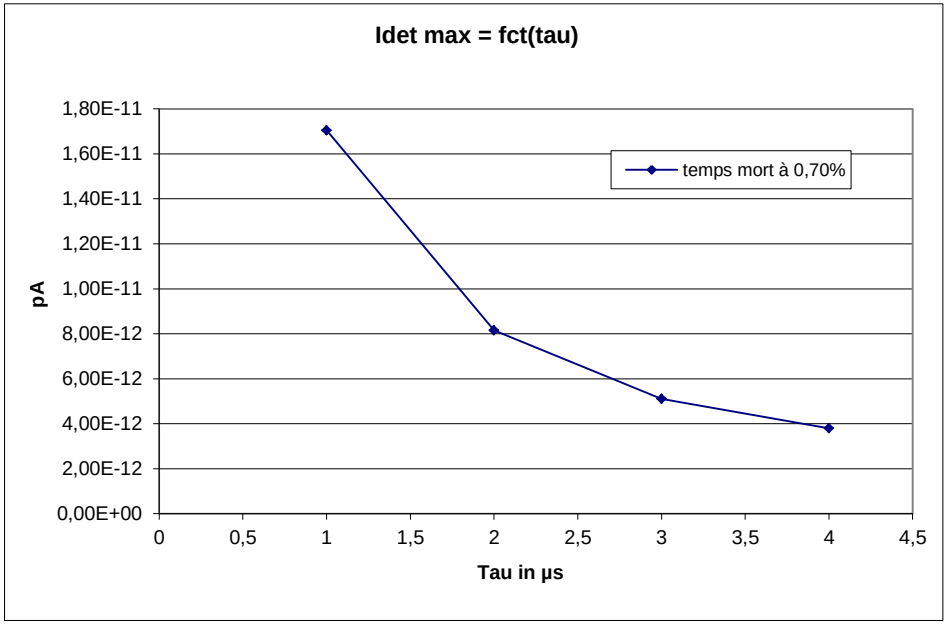
Minimal gain Av is 60 dB worst case.
Power consumption target is 250 µW worst case.
Gain feedback capacitor is 75 fF: this is the best tradeoff between signal gain and fast recovery (which requires low capacitance) and reset rate (which claims for larger capacitance).



SIRIUS1/2 : dead time consideration



Baseline restor (SHAPER output < 1 lsb)

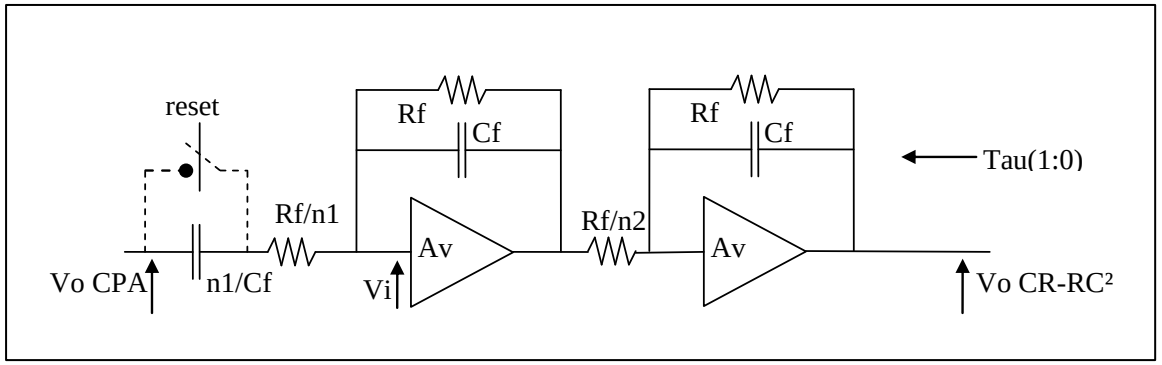


Maximum leakage current of the detector for a dead-time of 0.7 %

SIRIUS1/2: AFE – SHAPER conclusions

Pulse shaper is a single ended simple RC-CR^2 semi Gaussian filter. Inverting configuration allows for a simple common mode voltage buffer with low drive requirements. The time constant is set by a switched network capacitors and selection logic. This allows maintaining the input impedance (at high frequency) identical regardless τ.

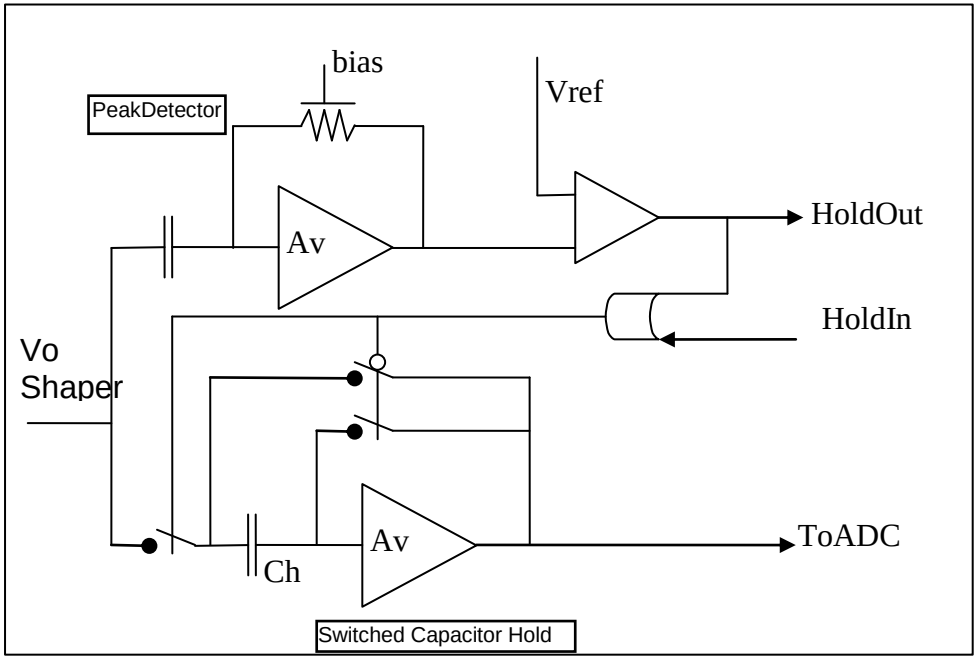
Gain settings: n1 = 8 and n2 = 5. This is achieved with R = 125 k W and C = 8pF at t = 1 µs (C1 = 64 pF).
Offset is less than 5 mV per amplifier.
Time constant is programmable between 1µs and 4 µs.
Power consumption target is 200 µW worst case.



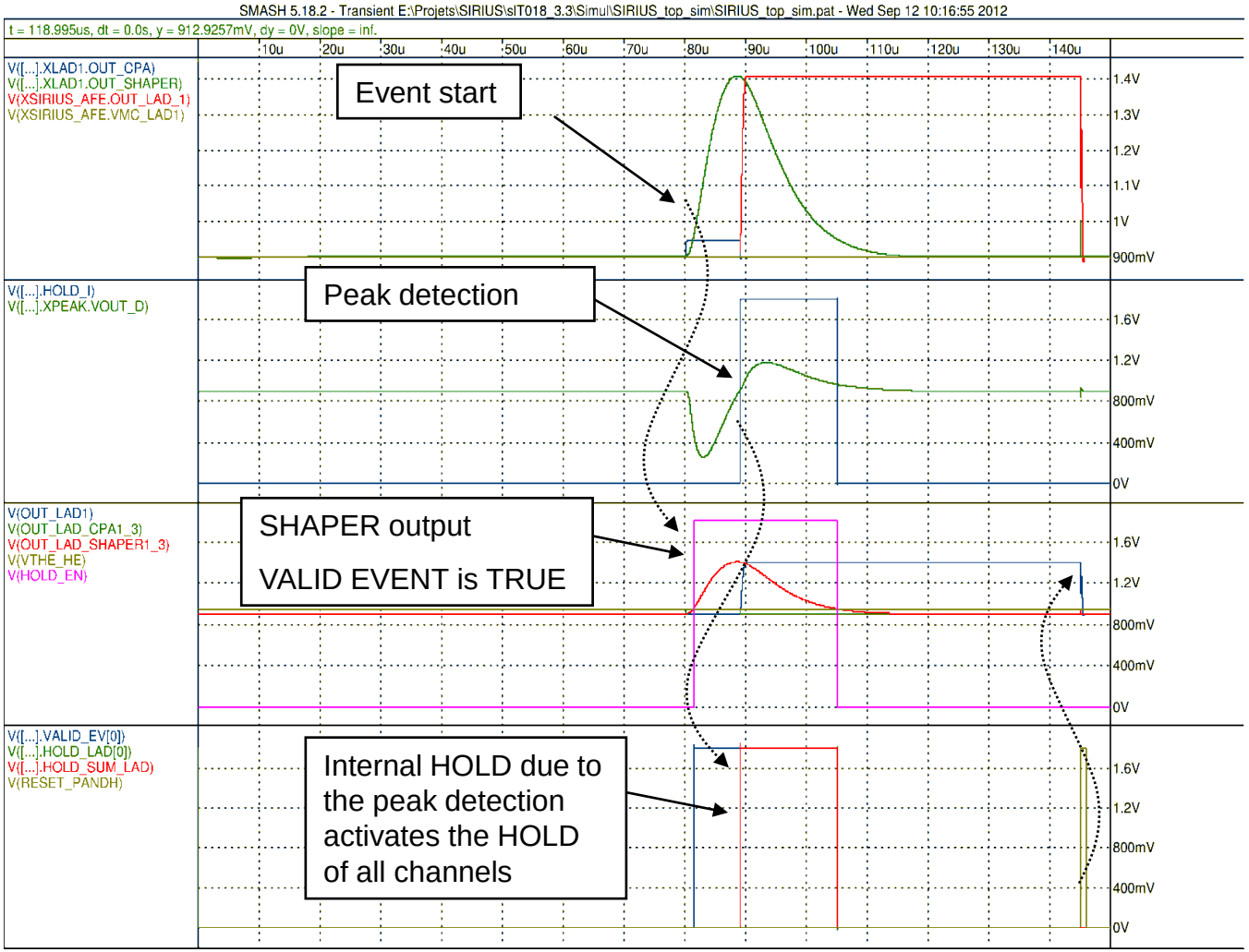
SIRIUS1/2: AFE – Peak&Hold conclusions

The P&H is based on a peak detector and switched capacitor based hold amplifier. Peak detection is performed by voltage derivation and zero detection, and for best performance, separate Peak and Hold functions are used. The feedback capacitor is selected according to Tau value to optimize the detection.

A 5 pF hold capacitance Ch provides good noise and retention performances at reasonable power consumption (target: 150 µW worst case).



SIRIUS1/2: AFE – simulation results 80 keV event



SIRIUS2: ADC

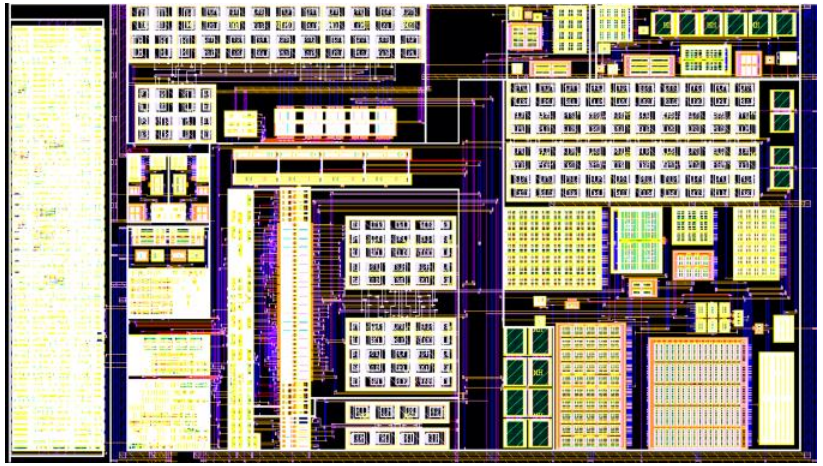
- Single 1.8 V analog power supply
- Main clock: 20 MHz – Conversion frequency: 1Msps

Main features

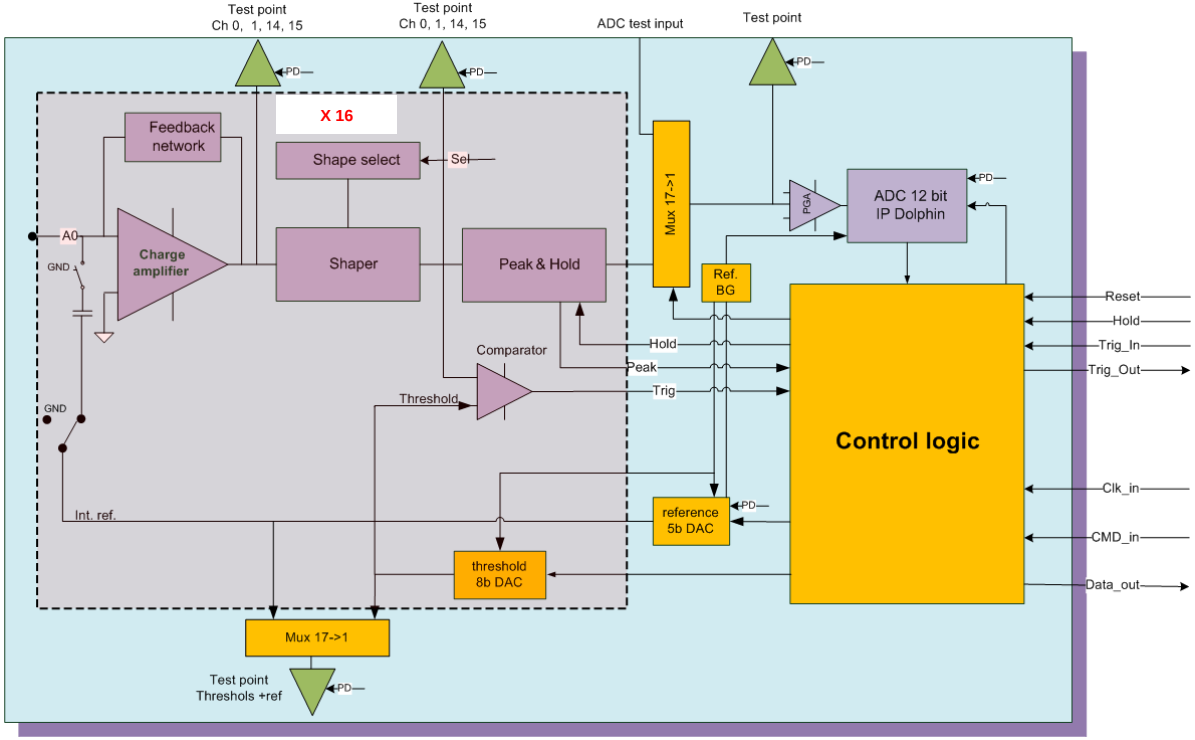
- Differential input, ground or common-mode voltage referred (selectable)
- Programmable full-scale input range x1, x2, x4, x8
- programmable conversion mode: single shot, continuous run
- Programmable resolution 8, 10, 12, 14 bits

Main performances

- Linearity
  - DNL: ±0.5 LSB (12 bits), no missing code
  - INL: 0.05% FS
- ENOB 11 bits
- PSRR: 40 dB@1kHz
- Power consumption: 3.6 nJ per conversation

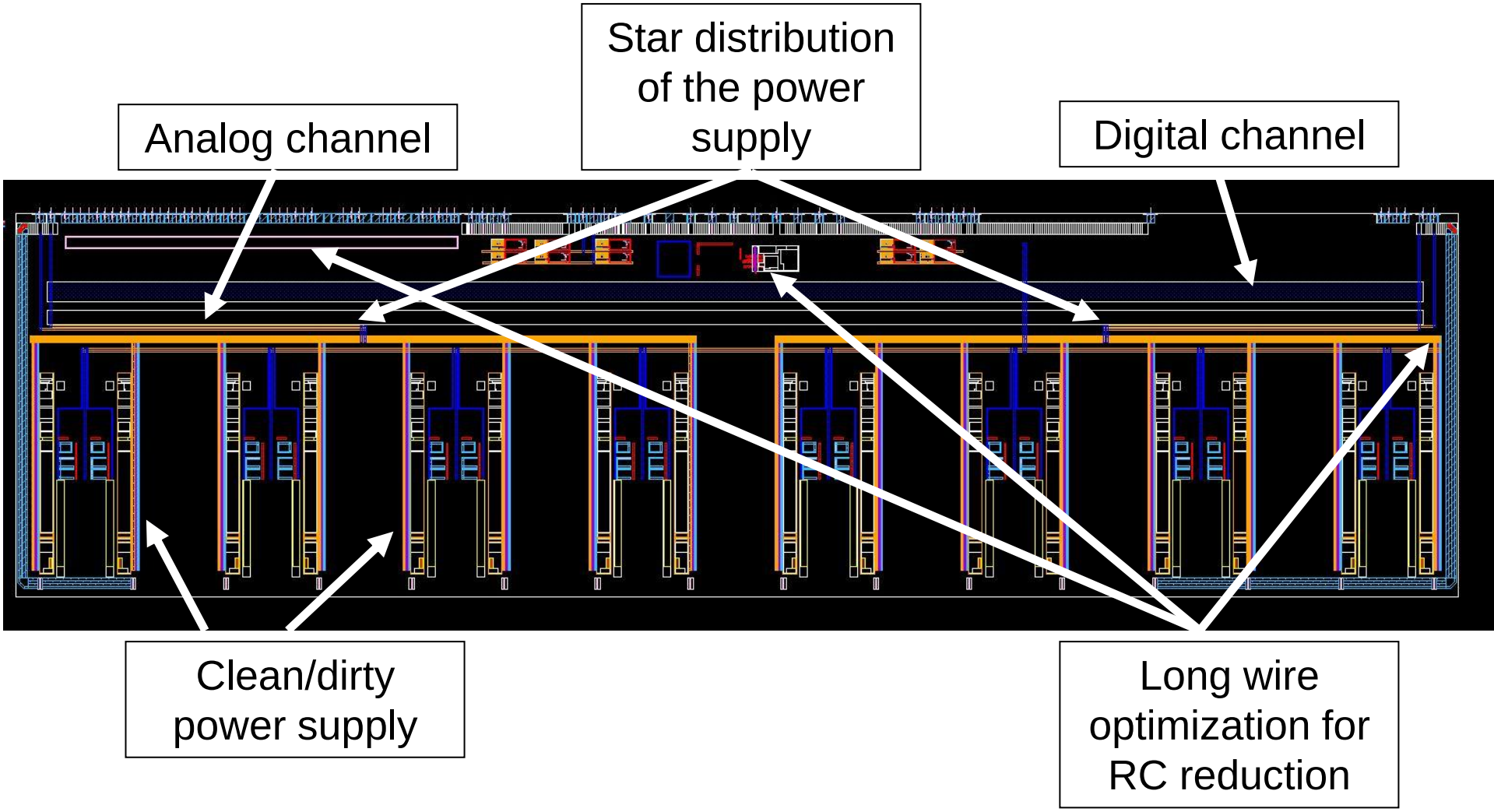


SIRIUS2: embedding 16 AFEs and the digital control

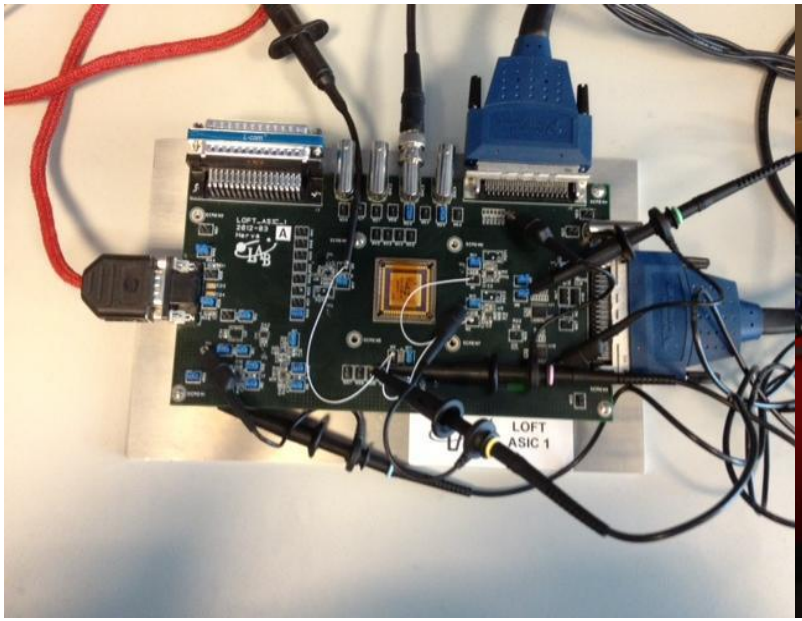


Functional block diagram of the SIRIUS 2 ASIC designed by IRAP and Dolphin. Orange color indicates the functions designed by IRAP.

SIRIUS2: physical implementation

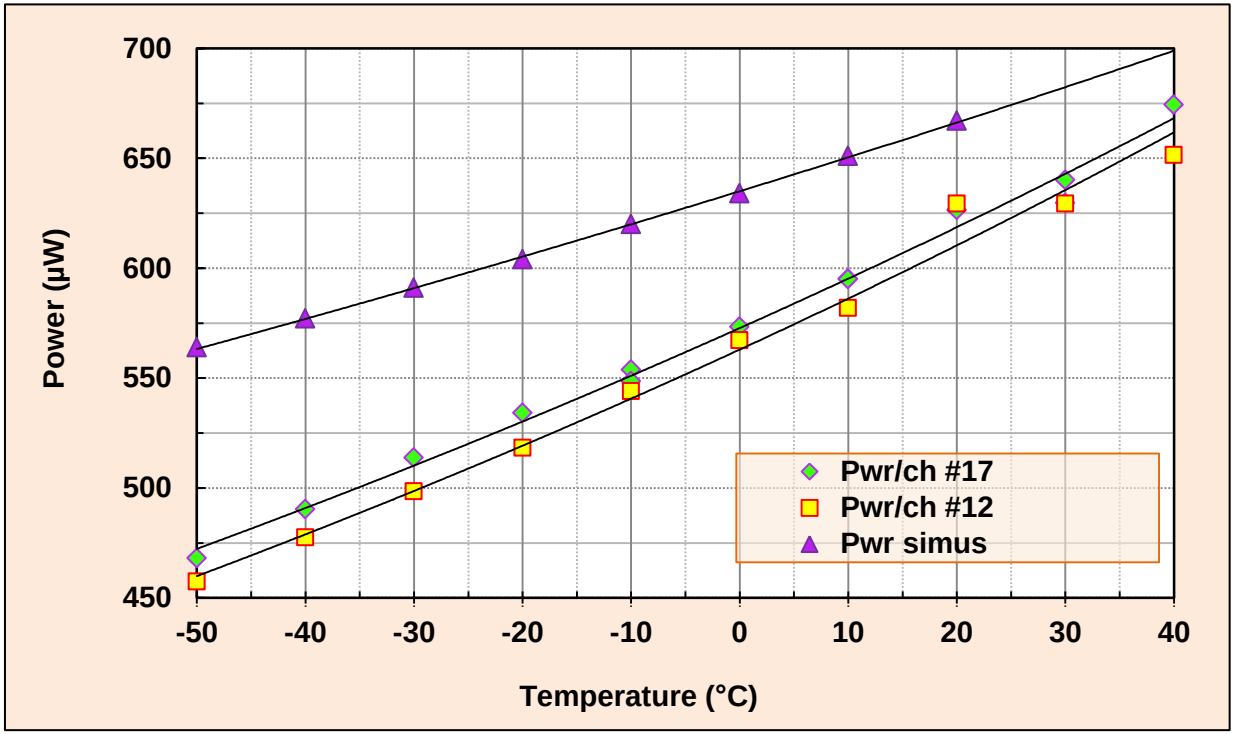


SIRIUS1: tests on prototypes



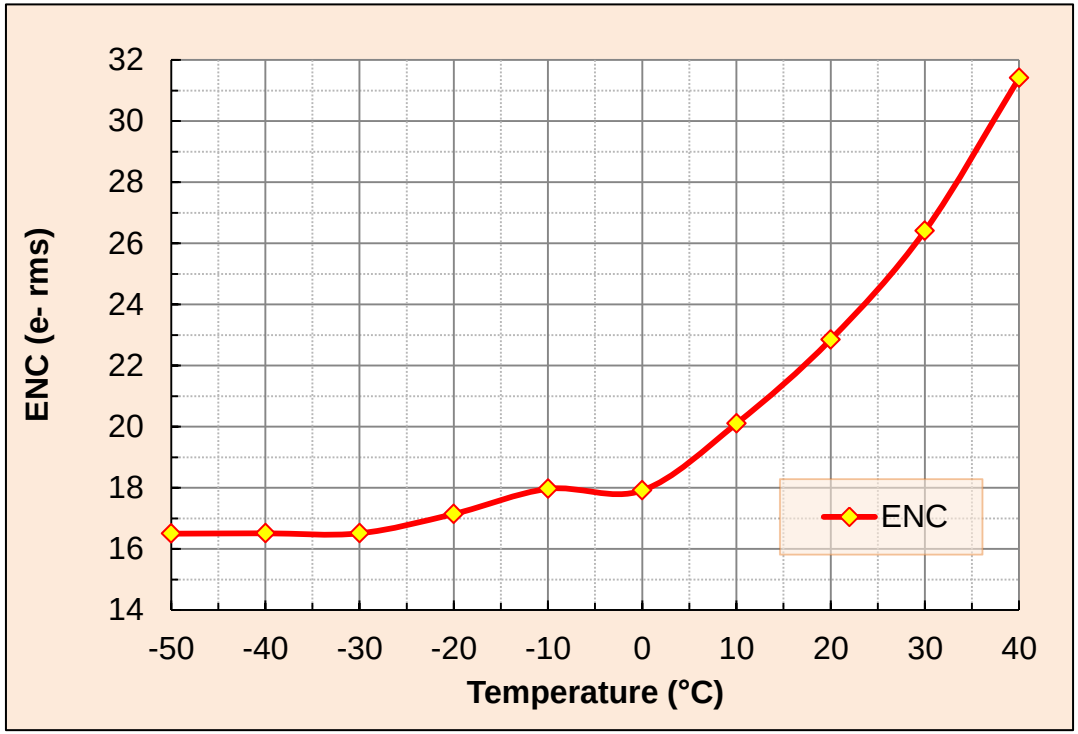
The test tools use modules installed in a PXI Express Chassis: controller with 16 bit Digitizers, Virtex 5 FPGA and Multi bank multiplexer.

Power consumption



Measured power consumption of 2 ASIC versus temperature (green lozenge and yellow square) compared to post layout simulations (purple triangle)

Measurement vs temperature



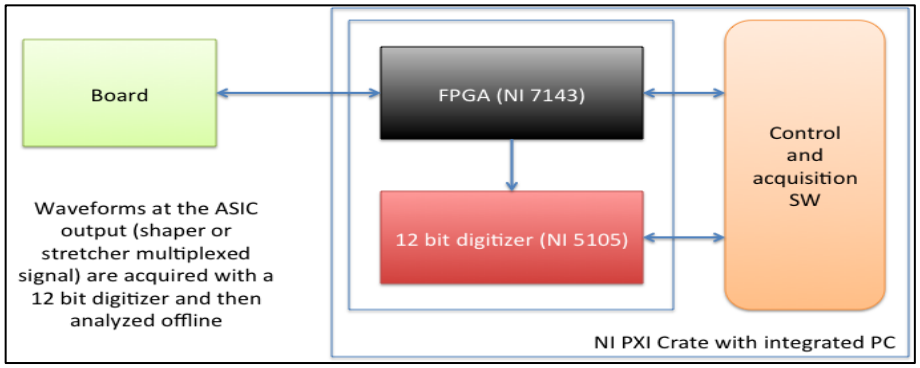
Variation of the noise of the ASIC alone, versus temperature
the post-layout simulations provides the following performances:
27.3 e- @ +25° C and 13 e- @ -30° C

Measurement at room temperature
Conclusions

Item	Specification	Simulations	Measurements
Power consumption (in µA)	360	325	317
AFE noise (in e-)	< 30 e-	23 e-	22 e-
Linearity (in %)	< 1 %	< 1 %	< 0.5 %

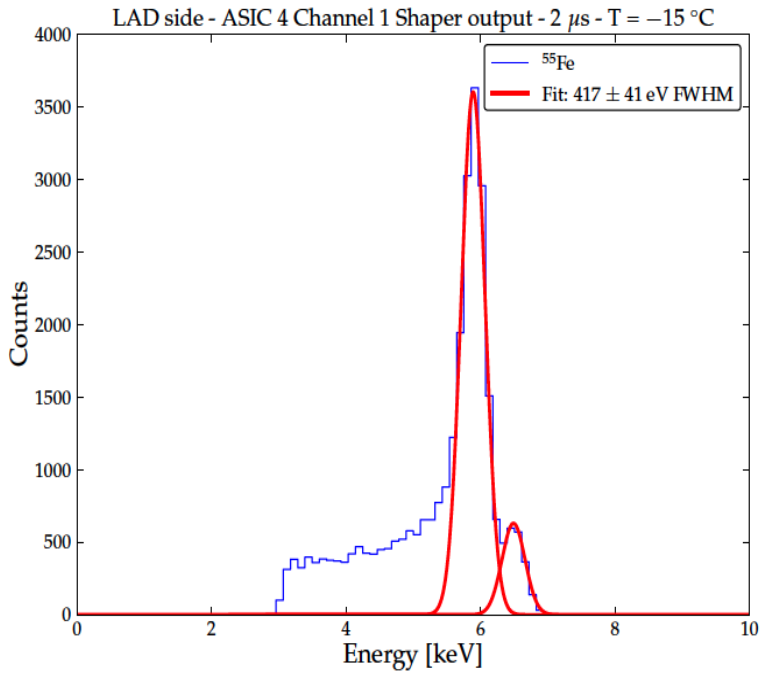
The performances in term of noise, power consumption and linearity meet the specification and the excellent correlation with the simulations permit to have a good predictability of the performances of the 40 k ASICs

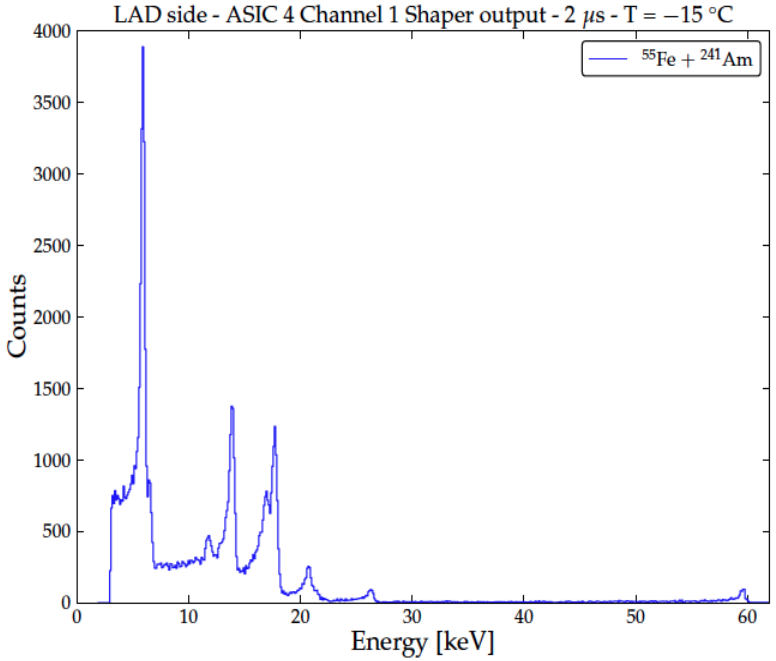
SIRIUS1: tests with the SDD



Test setup (left) and Test board (right). The SDD Detector is in the middle. On the bottom of the detector (LAD side of the SDD), 4 SIRIUS1 ASICs are bonded directly to the pads of the SDD, and on the top of the detector (WFM side), 2 other SIRIUS1

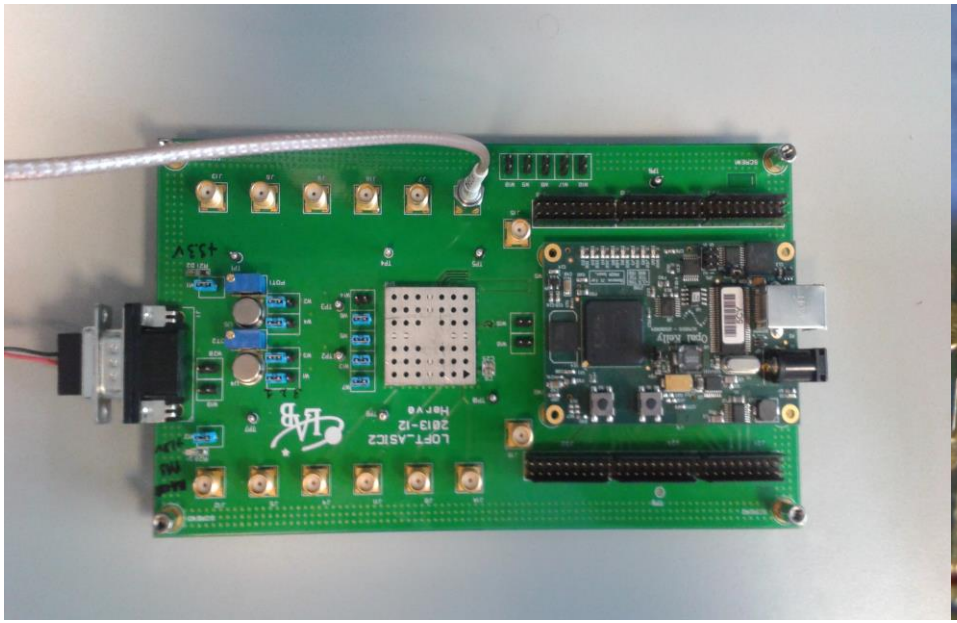
SIRIUS1 :Spectra from (buffered) shaper output

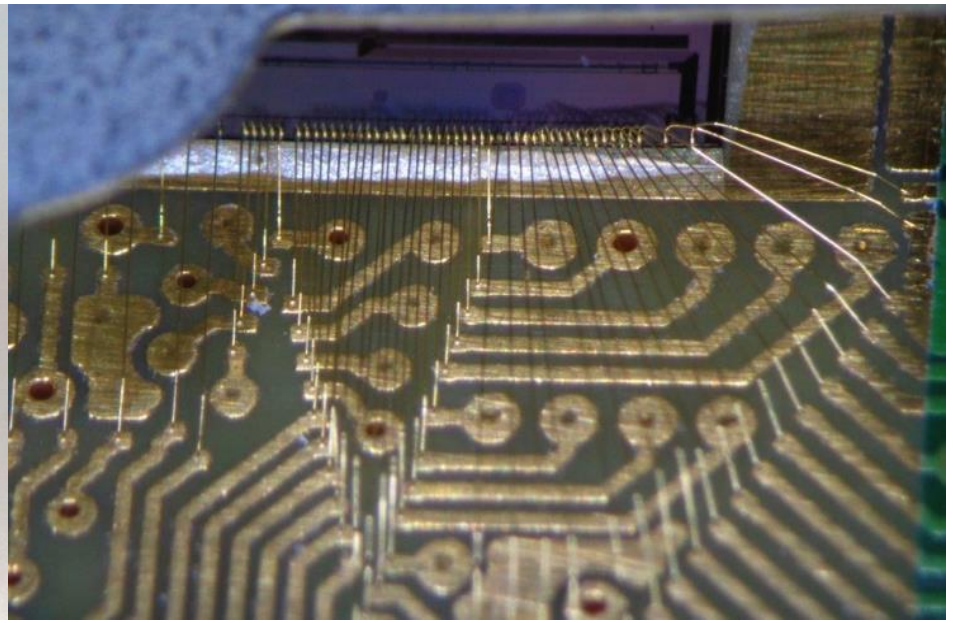




The resolution of the peaks, (see Fe-55 spectra) suffers for the charge sharing effect between two or three adjacent anodes that cannot be taken into account with this simple setup. The raw spectrum of a single channel acquired with the shaper signal includes not only the complete charge collection for one event, by the connected anode (single-anode events), but also the partial charge due to events impinging near the adjacent anodes. This is reflected in the tail on the left side of the peaks.

SIRIUS2: tests on prototypes





ASIC board (left) and ASIC bonding (right)

The functionality has been tested successfully
The characterization is in progress…

SIRIUS Odyssey: Conclusions

Two ASICs have been developed in 2 years demonstrating:

- State-of-the-art electrical performances in term of noise of the Analog Front End
- High reactivity and good team work between Dolphin Integration and IRAP to cope with the design, the characterization of the logic and mixed-signal blocks
- Mastery in controlling high performance analog blocks in terms of functionality and noise sensitivity to get the specifications
- Performances reached on silicon

Thank you

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