High performance analog Front End ASIC for interfacing with a Si Drift Detector and the control electronics – AMICSA 2014

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Abstract

In the frame of the LOFT (Large Observatory For x-ray Timing) program, a high performance analog Front End ASIC has been developed for interfacing with a Si Drift Detector and the control electronics.

The collaboration among IRAP, CNES and Dolphin Integration targeted an ASIC embedding 16 Analog Front Ends (AFEs,) a 12-bit ADC for digitization, DACs for the generation of the threshold for the minimum detectable event, low noise comparators, multipliers and the full digital interface used to control the AFEs and to read the measures. The ASIC was developed using the 180nm mixed technology of TSMC.

Keywords: ASIC, SDD, Xray, low power, low noise, CPA, shaper, LOFT, Analog Front End, mix signal, high performance.

I. INTRODUCTION

A. Context of the development of the ASIC

In the frame of the LOFT (Large Observatory For x-ray Timing) program, IRAP, CNES and Dolphin Integration have collaborated to develop a high performance ASIC (SIRIUS2) for interfacing Silicon Drift Detectors (SDDs, [13]) with the digital back-end

LOFT was candidate X-ray mission for the M3 slot of the Cosmic Vision program of the European Space Agency [10], [14]. It will be proposed again for the M4 mission. The LOFT objectives are to study the neutron star structure and equation of state of ultra-dense matter and to explore the conditions of strong-field gravity.

The primary enabling technology for the Large Area Detector (LAD) is the SDDs developed for the Inner Tracking System in the ALICE experiment of the Large Hadron Collider at CERN, by scientific institute INFN Trieste, Italy.

The project targets a 10 m² detector array for 2 to 80 keV Xrays detection at high sensitivity (50 – 200 eV) and good energy resolution (limited by electronic noise, itself limited by EOL detector leakage current) with a dead time << 1% at 1 Crab.

Such system will require 500 k to 600 k SDD detectors managed by 35 k to 40 k ASICs.

In Figure 1, the LAD and WFM (Wide Field Monitor) instruments are shown (The instrument design is described in detail in reference [10] and [11]).

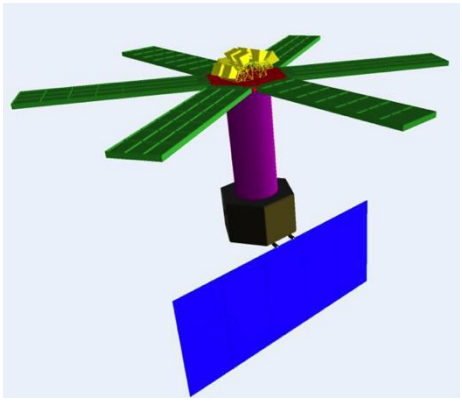

Figure 1: Loft payload in its original M3 proposal configuration. At the top the 6 panels of LAD (10 m2 effective area) and in the center the 6 cameras of WFM: green = LAD, yellow = WFM, red = Optical bench, purple = Structural Tower.

B. Interfaces with SDD and Module Back End Electronics

A LAD detector has 112 anodes on each side. 16 detection chains are implemented in each ASIC to fit with the size and the number of anodes of the detector

14 ASICs are glued on the rear side of a panel (seven per detector side). The Figure 2 shows the rear of a panel detector.

The ASIC control/test pads are bonded to the PCB, and the sixteen inputs directly to the SDD anodes, to reduce as much as possible the capacitance of the bonding's and so minimize the induced noise.

Each ASIC communicates through SPI like interface with a Module Back End Electronics (MBEE). A trigger line is provided to indicate that an event has occurred. An internal register (trigger map) indicates which anode is hit. This trigger is provided to the adjacent ASICs in order to hold and then read the 16 ASICs for noise measurements and common mode correction.

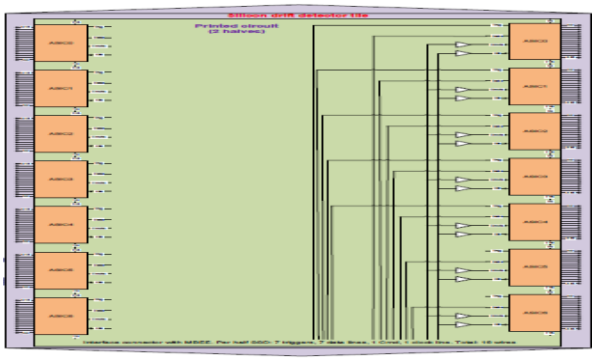

Figure 2: One panel of SDD and the 14 ASICs.

C. *Performance requirements*

The project started in 2012 targets the development of a first testchip (SIRIUS1) for the validation of the analog performances in a first phase and the development of the ASIC embedding all required functionalities (SIRIUS2) in a second phase.

SIRIUS1 embedding 8 Analog Front Ends (AFEs) was developed using the 180nm mixed technology of TSMC.
SIRIUS2 content has been extended for ASIC version with 16 Analog Front Ends (AFEs,) a 12-bit ADC for digitization, DACs for the generation of the threshold for the minimum detectable event, low noise comparators, multipliers and the full digital interface used to control the AFEs and to read the measures. The ASIC was developed using the 180nm mixed-signal technology of TSMC.
The challenging performances of SIRIUS1/SIRIUS2 are the energy resolution of 200eV @ 6keV (requiring a very high performance in term of noise corresponding to an ENC of 17 electrons end of life of the SDD), the very low power consumption (lower than 650 µW/channel) and a full scale higher than 22200 electrons.

The electrical requirements of SIRIUS1/SIRISU2 are summarized in the Table 1.

Main requirements impacting the design of the analog Front End of SIRIUS1/SIRIUS2

Item	State-of-the-art 2012	SIRIUS requirements
Input charge range	500 eV – 50 keV	200 eV – 80 keV
ENC (at -30°C)	< 30 electrons rms	< 20 electrons rms
EOF leakage current of the SDD	< 2 pA	< 10 pA
Shaping peak time	1-10 µs programmable	2-8 µs programmable
ADC resolution	9-10 bits	13 bits
Dead-time	Not available	0.7 %
Baseline restoration	Not available	50 µs

In term of radiation challenges, the total radiation dose expected on the LOFT orbit is low (1 krad), so a standard technology was used with design precautions. Indeed, the ASIC was designed using layout mitigation techniques to reduce the SEU effects and to increase the LET (the LOFT requirement is LET > 60 MeV):

- guard ring around the various functions
- ring of the opposite polarity around transistors when NMOS and PMOS transistors are close
- increased distance of active zone from the pads when they are connected to a pad
- maximized the number of contacts and vias
- differential design and differential routing
- optimized the matching (by reducing the size of the basic elements if necessary)
- avoided using the polysilicon for routing

The Figure 3 shows the detail of the layout mitigation techniques.

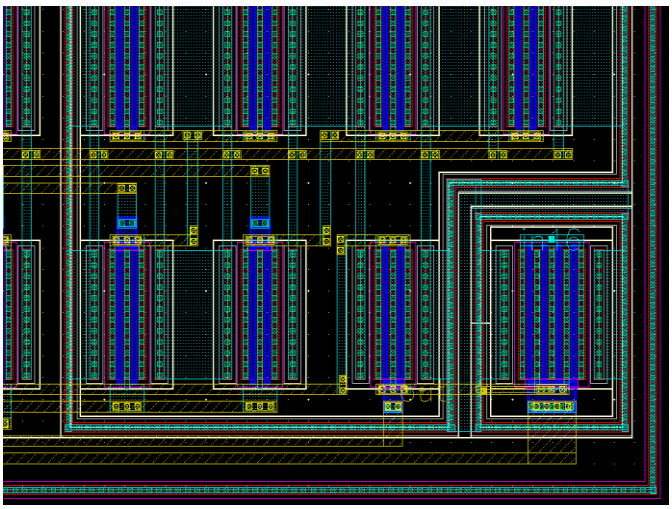

Figure 3: Detail of the layout showing the rules (rings) used to reduce the susceptibility to latch-up.

II. SIRIUS1/2: AFE ARCHITECTURE

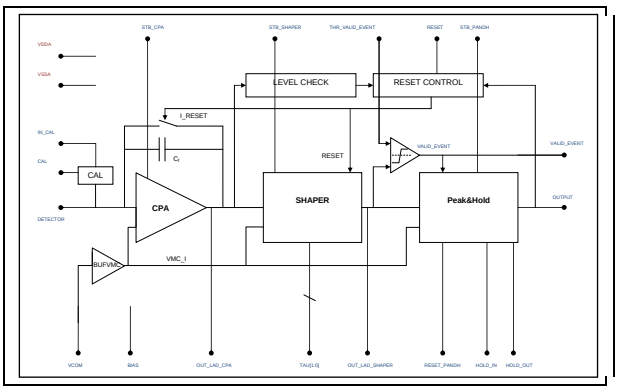

Figure 4: Detection Analog Front End (AFE) diagram

In terms of analog design, since the SDD delivers current pulses of low intensity and short duration, the AFE uses an integrator to accumulate the corresponding charge in a capacitor to deliver the resulting voltage output. This structure

is called a charge preamplifier, and will be noted CPA here below.

In order to add gain and improve signal to noise ratio, the CPA is usually followed by a pulse shaper, working as a matched filter.

The output of the CPA plus the shaper is a voltage pulse. Depending on the application, this pulse is either compared to a threshold and sent to an event counter, or sampled and digitized. In order to capture the energy of the Xray events, it is required to detect the pulse maximum and hold the voltage by a Peak and Hold, or P&H here below.

The Figure 4 provides an overview of the AFE architecture.

D. CPA design

The choice of the architecture of the CPA was driven by the noise performance which had to be lower than 20 e^-.

The Figure 5 describes a resistor based CPA. The effects of the resistance on noise and recovery time have been analyzed. As expected from theoretical analysis, noise is inversely proportional to feedback resistance (curves at 1 to 100 GΩ).

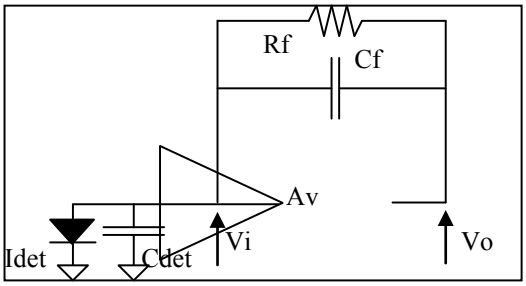

Figure 5: Resistor based CPA

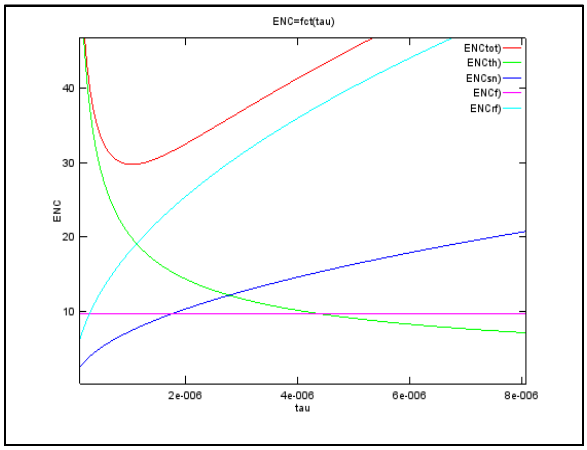

Figure 6: Simulation showing the noise performance as a function of τ with a resistor of 1.5 GΩ (10pA SDD leakage, τ in s). ENC_{tot} (red) is the square root of the sum of the square of the various ENC (ENC_{th}: CPA thermal noise, green; ENC_{sn}: shot noise due to detector, blue; ENC_f: 1/f noise, violet).

The Figure 6 represents total noise (red), thermal noise of CPA (green), 1/f flicker noise from preamplifier (blue-green), Rf thermal noise (light blue) and detector noise -at end of life worst case leakage current of 10 pA- (dark blue).

$$ENC_{tot} = \sqrt{\left(ENC_{th}^{\,2} + ENC_{C_f}^{\,2}\, ENC_{sn}^{\,2}\, ENC_{R_f}^{\,2}\right)}$$

As shown in Figure 6, simulations and computations prove that a 1.5 GΩ resistor is not sufficient to keep noise within the specifications: it is mandatory to select a CPA structure without a feedback resistor. The Figure 7 provides the noise performances for a reset-based CPA: the noise performances are achievable!

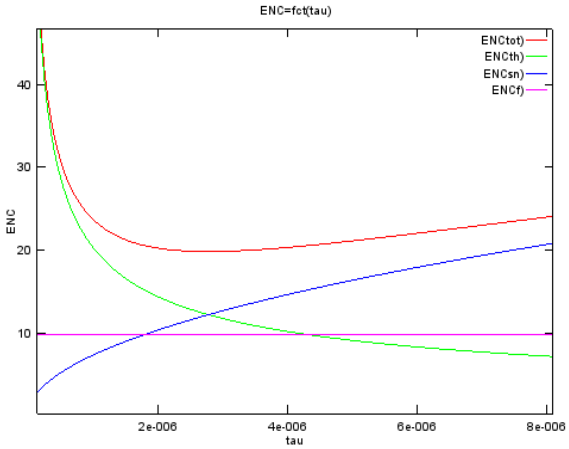

Figure 7: Simulation showing the noise performance as a function of τ without resistor (switched reset, 10pA SDD leakage, τ in s).

A reset circuit has been used to restore the base line after each event and when the baseline drift is such that a threshold is reached. A capacitor is used to inject charges for calibration purpose (see Figure 8).

Minimal gain Av is 60 dB worst case.

Power consumption target is 250 µW worst case.

Gain feedback capacitor is 75 fF: this is the best trade-off between signal gain and fast recovery (which requires low capacitance) and reset rate (which claims for larger capacitance).

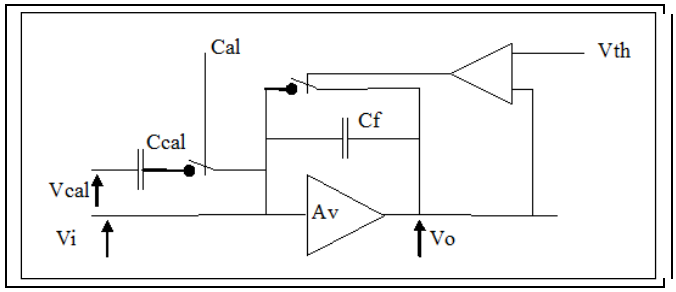

Figure 8: CPA architecture.

A. Shaper design

Pulse shaper is a single ended simple RC-CR^2 semi Gaussian filter (see Figure 9). Inverting configuration allows for a simple common mode voltage buffer with low drive requirements. The time constant is set by a switched network capacitors and selection logic. This allows maintaining the input impedance (at high frequency) identical regardless of time constant τ.

Gain settings: n1 = 8 and n2 = 5.

This is achieved with R = 125 k W and C = 8pF at t = 1 µs (C1 = 64 pF).

Offset is less than 5 mV per amplifier.

Time constant is programmable between 1µs and 4 µs.

Power consumption target is 200 µW worst case.

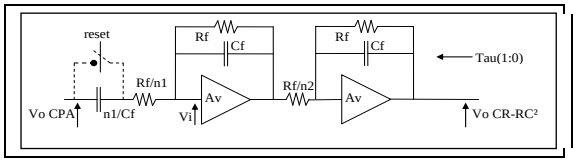

Figure 9: SHAPER architecture.

E. Peak&Hold design

The P&H is based on a peak detector and switched capacitor based hold amplifier (see Figure 10). Peak detection is performed by voltage derivation and zero detection, and for best performance, separate Peak and Hold functions are used. The feedback capacitor is selected according to Tau value to optimize the detection.

A 5 pF hold capacitance Ch provides good noise and retention performances at reasonable power consumption (target: 150 µW worst case).

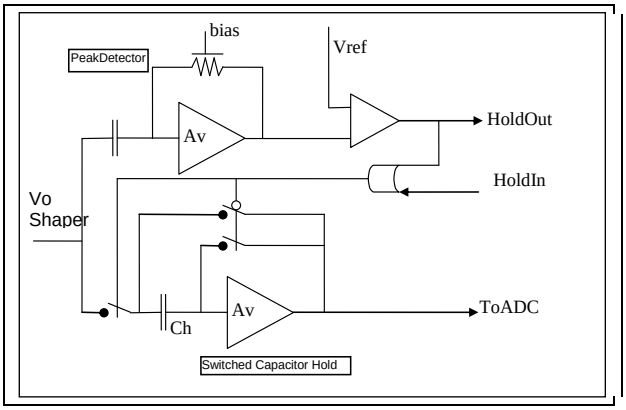

Figure 10: Peak&Hold architecture.

A. SIRIUS2: ASIC ARCHITECTURE

The ASIC version (SIRIUS2, Figure 11), jointly developed by IRAP and Dolphin Integration, is a fully functional version implementing all the functionalities required for LAD-LOFT: various controls capabilities and serial interface with the Front End Electronics, size and pitch for LAD, 16 channels, PGA and 10/12/14 bit ADC, threshold control (16 x 8 bit DACs), calibration DAC (5 bit), reference band gap and internal test feature. The topology of the ASIC was also changed with all detector inputs placed at one side of the chip and the control on the opposite side to comply with size of the SDD and to reduce the coupling between digital section and low level signal sections.

No improvement of the analog section (analog chains) has been added due to the short time before the ESA M3 selection.

The ASIC prototype will be used to perform radiation tests, aimed at qualifying the ASIC design and technology for TID and Latch-up.

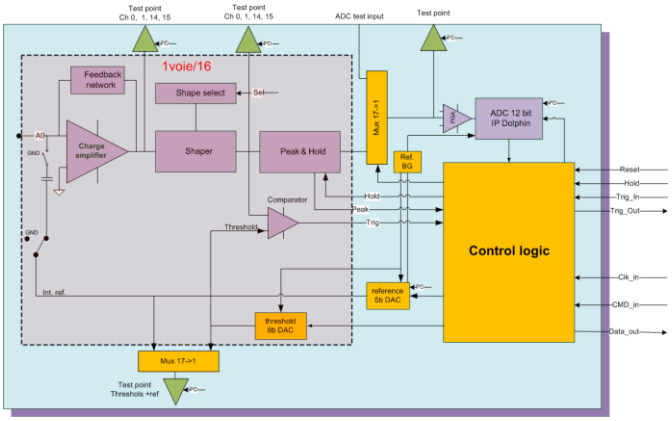

Figure 11: Functional block diagram of the SIRIUS 2 ASIC designed by IRAP and Dolphin. Orange colour indicates the functions designed by IRAP

B. SIRIUS1: MEASUREMENTS

The SIRIUS1 testchip was tested alone at IRAP, Toulouse and with the SDD detector at INAF/IASF, Bologna, Italy. The test tools use modules installed in a PXI Express Chassis: controller with 16 bit Digitizers, Virtex 5 FPGA and Multi bank multiplexer (Figure 12 and Figure 13)

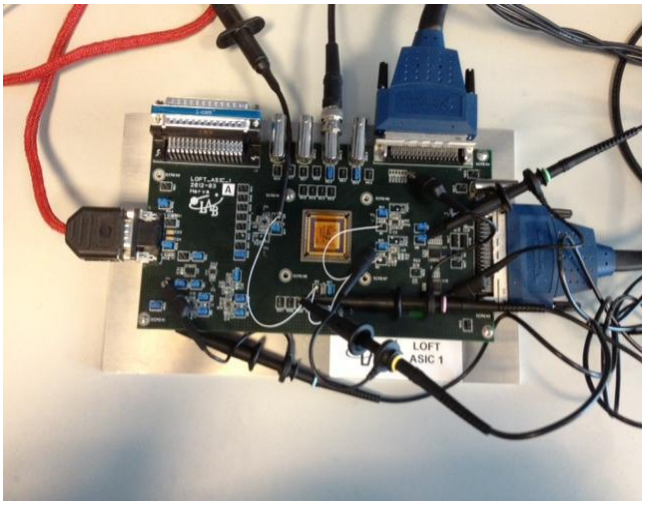

Figure 12: Test board for SIRIUS1

Figure 13: Test bench for SIRIUS1

The testchip was powered by an external power supply that provides +5V for the test board electronics. Linear regulators provide the 3.3V to the digital I/0's of the testchip. A low noise power supply provides the 1.8V to the internal analog and core digital electronics of the ASIC. It is possible to power or switch off independently the bias circuits, the 8 CPA's, the 8 Sampler's, the 8 Sample & Hold's and the 12 buffers. We measured (Figure 14) at each temperature, the power consumed by the 8 analog chains (buffers off). The power is lower than the expected from simulations and within specifications.

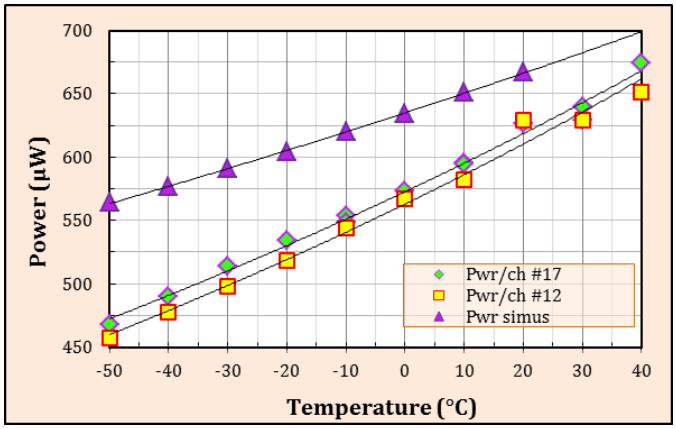

Figure 14: Measured power consumption of 2 ASIC versus temperature (green lozenge and yellow square) compared to post layout simulations (purple triangle)

We used the testchip built-in capacitor to inject a charge at the input of the CPA. For each injection 1000 measurements are made of the hold voltage using a 24-bit ADC. The mean value is calculated to minimize the noise due to the test equipment. One thousand identical charges are injected for each injection level. The mean value of the output voltage is computed and the sigma of the distribution of the 1000 measurements. The value of noise is computed from this sigma value. It is not varying much according to the injected level. We repeated the same measures at various temperatures (see Figure 15). The ENC is decreasing with the temperature to reach 16.5 e- below -30°C.

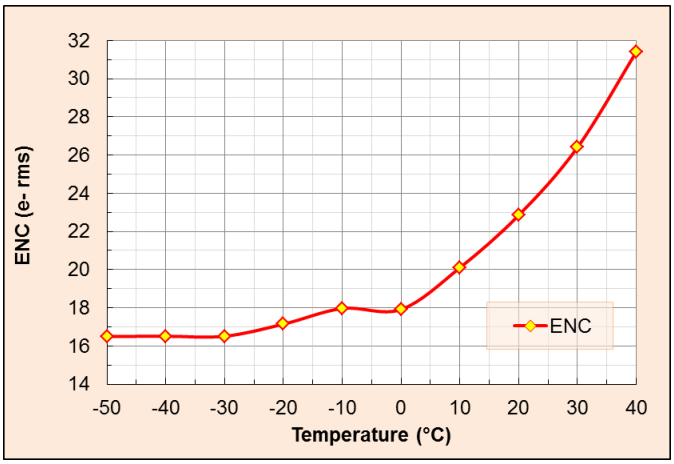

Figure 15: Variation of the noise of the ASIC alone, versus temperature the post-layout simulations provides the following performances: 27.3 e- @ +25°C and 13 e- @ -30°C

The performances in term of noise, power consumption and linearity meet the specification (see Table 2) and the excellent correlation with the simulations permit to have a good predictability of the performances of the 40 k ASICs

Measurement at room temperature

Item	Specification	Simulations	Measurements
Power consumption (in µA)	360	325	317
AFE noise (in e-)	< 30 e-	23 e-	22 e-
Linearity (in %)	< 1 %	< 1 %	< 0.5 %

C. *Test with the SDD*

Figure 16: Test board

Figure 16: the SDD Detector is in the middle. On the bottom of the detector (LAD side of the SDD), 4 SIRIUS1 testchip are bonded directly to the pads of the SDD, and on the top of the detector (WFM side), 2 other SIRIUS1.

Figure 17 and Figure 18: the resolution of the peaks, (see Fe-55 spectra) suffers for the charge sharing effect between two or three adjacent anodes that cannot be taken into account with this simple setup. The raw spectrum of a single channel acquired with the shaper signal includes not only the complete charge collection for one event, by the connected anode (single-anode events), but also the partial charge due to events impinging near the adjacent anodes. This is reflected in the tail on the left side of the peaks.

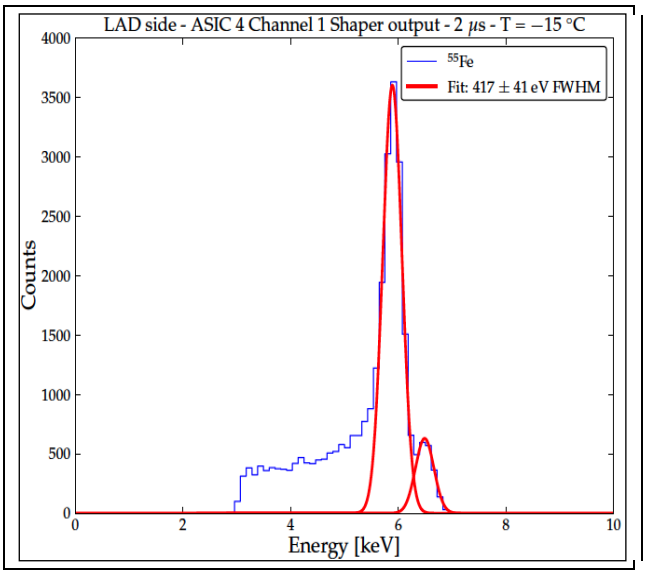

Figure 17: Spectrum measurement (^{55}Fe)

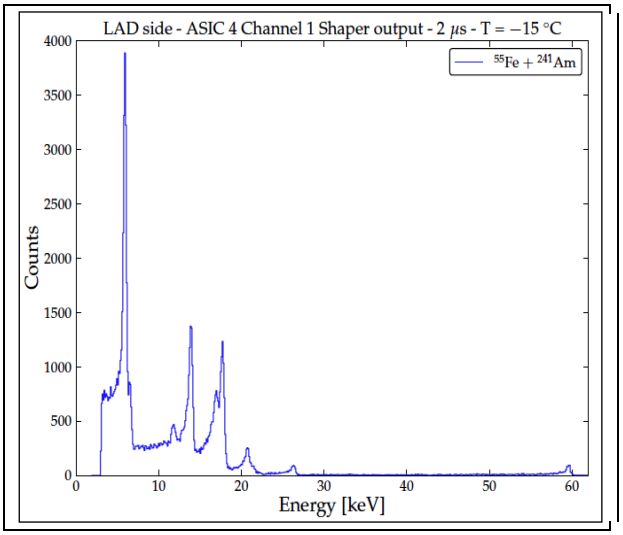

Figure 18: Spectrum measurement (^{55}Fe+^{241}Am)

D. SIRIUS2: MEASUREMENTS

A High Density PCB (Figure 19 and Figure 20) has been developed to support the test of SIRIUS2: more than 50 bondings are necessary to feed the inputs/outputs; the 16 CPA input pads are not bonded and left unconnected. Low noise power supply regulators for the ASIC and the associated decoupling capacitors are installed on this board. A temperature sensor placed close to the ASIC is used to measure the temperature of the ASIC. It is readable through a SPI like protocol. The interface with the control PC is made through an Opal Kelly board plugged directly on the test board.

The characterization is in progress.

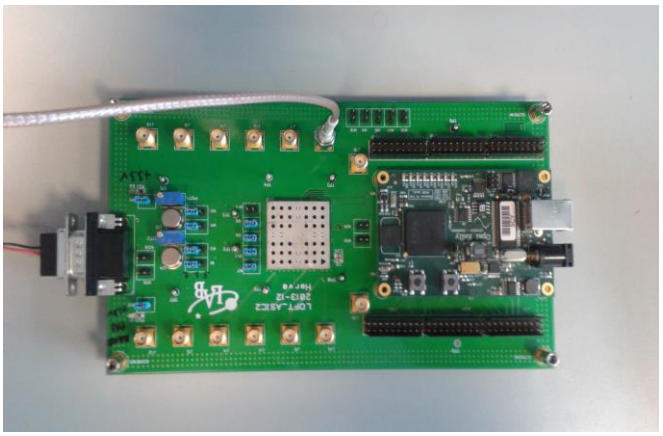

Figure 19: ASIC board

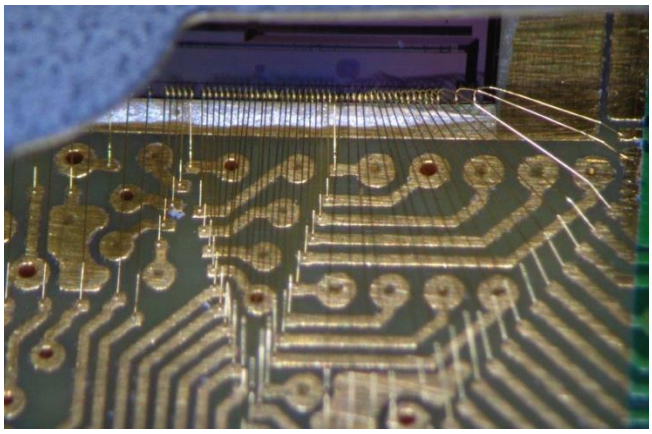

Figure 20: ASIC bonding

E. CONCLUSIONS

Two circuits (testchip + ASIC prototype) have been developed in 2 years demonstrating:

- State-of-the-art electrical performances in terms of noise of the Analog Front End
- Good team work between Dolphin Integration and IRAP to cope with the design, the characterization of the logic and mixed-signal blocks
- Mastery in controlling high performance analog blocks in terms of functionality and noise sensitivity to get compliance to the specifications
- Performances verified on silicon

REFERENCES

[1] Willy M.C. Sansen, Zhong Yuan Chang, "Limits of Low Noise Performance of Detector Readout Front Ends in CMOS Technology," IEEE transactions on circuits and systems, vol. 37, N°11, November 1990.

[2] Caccia, S., Bertuccio, G., Maiocchi, D., Malcovati, P., Ratti, N., Martin, D., "A Mixed-Signal Spectroscopic-Grade and High-Functionality CMOS Readout Cell for Semiconductor X-gammaRay Pixel Detectors," IEEE Transactions on Nuclear Science, Vol. 55, N°. 5, October 2008, p. 2721.

[3] Bastia, P., Bertuccio, G., Caccia, S., Cappelluti, I., Grassi, M., Malcovati, P., Martin, D., Ratti, N., "STARX32: A Complete On-Chip X-Ray Spectroscopy Readout System with Imaging Capability," AMICSA 2010, 5-7 September (2010).

[4] Singh, H., Dr. Sarin, R.K., Dr. Singh, S., "Analysis and Modeling of 1/f noise in MOSFETs for circuit Applications: The Joint Effect of Channel Length and Conducting Slab Resistance," Canadian Journal on Electrical and Electronics Engineering, Vol. 1, N°6, October (2010).

[5] Izadpanah, S., Gollmakani, A., "Three Stage Low Noise Operational Amplifier in 0.18m CMOS Process," ICSES proceedings (International Conference on Signals and Electronic Systems), 2012.

[6] Habid Muhammad Nazir Ahmad, Mohammad Shafquatul Islam, Arman Riaz Ochi, "Analysis of Ultra Wide Band Four stage Distributed Low Noise Amplifier in TSMC 0.18um Process," International Journal of Research in Computer Engineering and Electronics, vol. 2, issue 6, (Dec. 2013).

[7] Tsividis, Y., "Operation and modeling of the MOS transistor," McGraw-Hill, pp. 440-512, (1999).

[8] Bouyjou, F., "Nouvelles chaînes d'instrumentations intégrées multivoies pour l'astrophysique," These of Toulouse University, December 2011.

[9] Goulding, F. S., Landis, D. A., "Signal processing for semiconductor detectors," IEEE Transactions on Nuclear Science, Vol. NS-29, No. 3, June 1982.

[10] Feroci, M, et al., "The Large Observatory for X-ray Timing (LOFT)," Experimental Astronomy 34, issue 2 (2012) 415.

[11] Zane, S., et al., "The Large Area Detector of LOFT: the Large Observatory for X-ray Timing," SPIE proceedings, Montreal, 2014.

[12] Miller, J., "Dependence of the input impedance of a three-electrode vacuum tube upon the load in the plate circuit," Scientific Papers of the Bureau of Standards, Volume 15, 1919-1920, 330-368.

[13] Rachevski et al. 2014, SPIE proceedings, Montreal 2014.

[14] Feroci, M., et al. 2014, SPIE proceedings, Montreal 2014.