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High performance analog Front End ASIC for interfacing with a Si Drift Detector and the control electronics

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In the frame of the LOFT (Large Observatory For x-ray Timing) program, IRAP, CNES and Dolphin Integration have collaborated to develop a high performance ASIC (SIRIUS2) for interfacing Silicon Drift Detectors (SDDs) with the digital back-end

LOFT was candidate X-ray mission for the M3 slot of the Cosmic Vision program of the European Space Agency. It will be proposed again for the M4 mission. LOFT is designed to study the neutron star structure and equation of state of ultra-dense matter and to explore the conditions of strong-field gravity.

The primary enabling technology for the Large Area Detector (LAD) is the SDDs developed for the Inner Tracking System in the ALICE experiment of the Large Hadron Collider at CERN, by scientific institute INFN Trieste, Italy.

The project targets a 10 m² detector array for 2 to 80 keV Xrays detection at high sensitivity (50 –200 eV) and good energy resolution (limited by electronic noise, itself limited by EOL detector leakage current) with a dead time « 1% at 1 Crab.

Such a system will require 500 k to 600 k SDD detectors managed by 35 k to 40 k ASICs.

The collaboration among IRAP, CNES and Dolphin Integration targeted these ASICs interfacing the SDDs and the digital back end on the satellite.

SIRIUS2 embeds 16 Analog Front Ends (AFEs,) a 12-bit ADC for digitization, DACs for the generation of the threshold for the minimum detectable event, low noise comparators, multipliers and the full digital interface used to control the AFEs and to read the measures. The ASIC was developed using the 180nm mixed technology of TSMC.

The harder performances of SIRIUS2 are the energy resolution of 200eV @ 6keV (requiring a very high performance in term of noise corresponding to an ENC of 17 electrons end of life of the SDD), the very low power consumption (lower than 650 μW/channel) and a full scale higher than 22200 electrons.

In term of analog design, since the SDD deliver current pulses of low intensity and short duration, the AFE uses an integrator to accumulate the corresponding charge in a capacitor to deliver a voltage output. This structure is called a charge preamplifier, and will be noted CPA here below.

In order to add gain and improve signal to noise ratio, the CPA is usually followed by a pulse shaper, working as a matched filter.

The output of the CPA plus the shaper is a voltage pulse. Depending on the application, this pulse is either compared to a threshold and sent to an event counter, or sampled and digitized. In order to capture the energy of the Xray events, it is required to detect the pulse maximum and hold the voltage by a Peak and Hold, or P&H here below.

Critical performances have been analyzed and quantified.

Noise contributions have been estimated and rated.

It has been highlighted that important characteristics such as noise, gain, speed, power, area have conflicting requirements and that some trade-offs must be carefully balanced.

The resulting formulas will be presented, in parallel to simulations, in order to highlight the technical solutions that have been chosen for LOFT project requirements.

The CPA has been designed using switched reset structure based on a gain capacitor of 75 fF. This offers a good balance between preamplifier gain and dead time requirements, while keeping transient behavior of pulse shaper within acceptable limits. Instead of generating a tiny continuous leakage, the capacitor is regularly shorted for a small time (after detection, when leakage current has generated an excessive offset at CPA output). This solution is the best in term of noise with a drawback link to the dead time due to the reset.

The noise performance of around 20 ENC at tau of 2 µs, for a dead time lower than 0.7 % meets the initial specifications.

For the SHAPER the best trade off comes with CR-RC² topology. Higher the orders lower the ENC. But global optimization requires significant gain in the shaper. Higher order filters (CR²-RC2 or CR-RC3) have lower peak gain. Hence it is necessary to boost resistors ratios, severely loading the CPA or generating higher shaper noise. Simulations have confirmed that total signal to noise ratio was not improved by higher order shapers.

For the P&H, a derivation-based peak detector followed by a switched capacitor hold cell will feed the analog to digital converter.

The measurement with the SDD have been done at room temperature (≈25°) showing a best value obtained in term of noise of 24.5 e- rms with shaping time 4 us. The gain linearity is very good and the gain is stable over temperature range. The power consumption achieved is lower than 580 µW per channel at room temperature.

Primary author: BONZO, Andrea (Dolphin Integration)

Co-authors: Mr CROS, Alain (IRAP); Mr GAILLARD, Christophe (Dolphin Integration); Mr RAMBAUD, Damien (IRAP); Mr BARRET, Didier (IRAP); Mr GRAND, Emmanuel (Dolphin Integration); Mr MOUTAYE, Emmanuel (IRAP); Mr SEYLER, Jean-Yves (CNES); Mr LETUVEE, Nicolas (Dolphin Integration); Mr BODIN, Pierre (CNES); Mr CLEDASSOU, Rodolphe (CNES); Mr MORANDINI, Yvan (Dolphin Integration)

Presenter: BONZO, Andrea (Dolphin Integration)

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