Mixed-Signal Design Methodology for Various Radiation Environments with Applications to a 0.35μm, 65V Quadruple-Well BCD Technology

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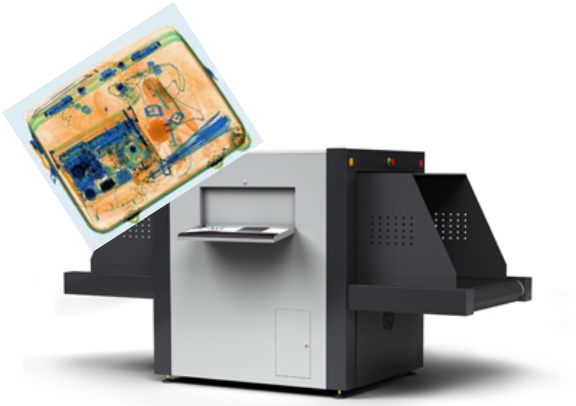
Outline

- Radiation Environments for Different Applications
- Key Process Parameters for 0.35 μm BCD (Bipolar-CMOS-DMOS)
- Library, PDK, Analog IP
- Total Ionizing Dose Testing
- Single Event Effects Testing
- Life Testing Results
- Application Classifications
- A Note about Recent Changes to US Export Law
- Summary

Example Radiation Environments



Key Process Parameters: Baseline 0.35μm

- P-Substrate, 10 Ohm-cm
- Triple-Well
- LOCOS Isolation
- 3.3V and 5V Transistors
- 1 Polysilicon, 4 Metal
- Planar Metallization with Tungsten Plugs
  - Stacked Contacts/Vias
- Ti Salicide for Source/Drains
- PETEOS/SiN Passivation Stack

Key Process Parameters: High Voltage 0.35μm

- Quadruple-Well
- High Voltage Devices (5 Device Types):
  - 40V N- and P- LDMOS
  - 65V N- and P- LDMOS
  - 65V N- eDMOS
- HV Diodes (NLDMOS, PLDMOS)
- Zener Diode

0.35 μm RH Library and Analog Cells

- RH Digital Library
- RH I/O
  - Single ended 2.5V to 5.0V
  - LVDS/differential
- RH Analog Cells
- RH Analog I/O

Example RH Analog Cells

- Analog IP (Aeroflex):
  - Low-Noise Analog Front-Ends (AFE's)
  - Band-gap references, Voltage References
  - Comparators
  - High slew-rate op amps
  - Instrumentation amplifiers
  - Gate Drivers, Floating Gate Drivers
  - Low resistance analog switches with over-current protection
  - Precision current sources
  - RC Oscillators (30ppm stability)
  - Watch-Dog Timers
  - Power On Reset (POR)
  - LDO Voltage Regulators
  - Charge Pumps
  - Level Shifters
  - Analog I/O with 4000V (HBM)

Example RH Analog Cells

- IP (Aeroflex):
  - Data converters:
    - Over-sampled ADC's:
      - 12 to 22 bit (ENOB 10 to 19 bits)
      - Delta-Sigma and Current to Frequency
      - 2^{nd} to 4^{th} order modulators
      - Sample rates to 100kHz+
      - Correlated Double Sampling, Auto-Zero, Chopped
      - Programmable digital filters
    - Pipeline ADC's:
      - 10 to 16 bit (ENOB 10 to 14 bit)
      - Low latency
      - Sample rates to 20MHz
      - Low power (e.g. 2.5mW/MHz @ 16 bit, SNR = 90dB)
    - Successive Approximation (SAR)
      - 8 to 10 bit (ENOB 7 to 9 bit)
      - Sample rates to 500kHz

Example RH Analog Cells

- IP (Aeroflex):
  - Data converters:
    - Current-Steering DACs:
      - 10 bit to 14 bit input
      - Settling times allow operating to 4MHz
      - High SFDR
      - Current or Voltage Outputs
      - Buffered Outputs up to +/- 15V
    - R2R DACs:
      - 10 bit to 14 bit input
      - Settling times allow operating to ~1MHz
      - Voltage Outputs
      - Buffered Outputs up to +/- 15V

Example RH Analog Cells

- IP (Aeroflex):
  - Digital Filters
    - SincN, COI
    - Programmable FIR, IIR
  - Analog Filters
    - Biquads
    - Elliptical, Butterworth, Bessel, Chebyshev
    - Continuous Time or Discrete Time/Switched Capacitor
  - NV Memory Controllers
    - Aeroflex proprietary adaptive memory controller senses and adapts to “age” of NV memory, extending endurance lifetime
  - SRAM Memory Compiler
    - Aeroflex leaf cells and SRAM cells

Total Ionizing Dose (TID) Testing of BCD

▼ Transistors:

Voltage	Aeroflex Transistor Type	W/L (microns)
3.3V	i-NMOS	6.85/0.35
3.3V	PMOS	5.0/0.35
5.0V	i-NMOS	6.85/0.5
5.0V	PMOS	5.0/0.5
40V	nLDMOS	10/0.2
40V	pLDMOS	10/0.2
65V	nLDMOS	10/0.2
65V	pLDMOS	10/0.2

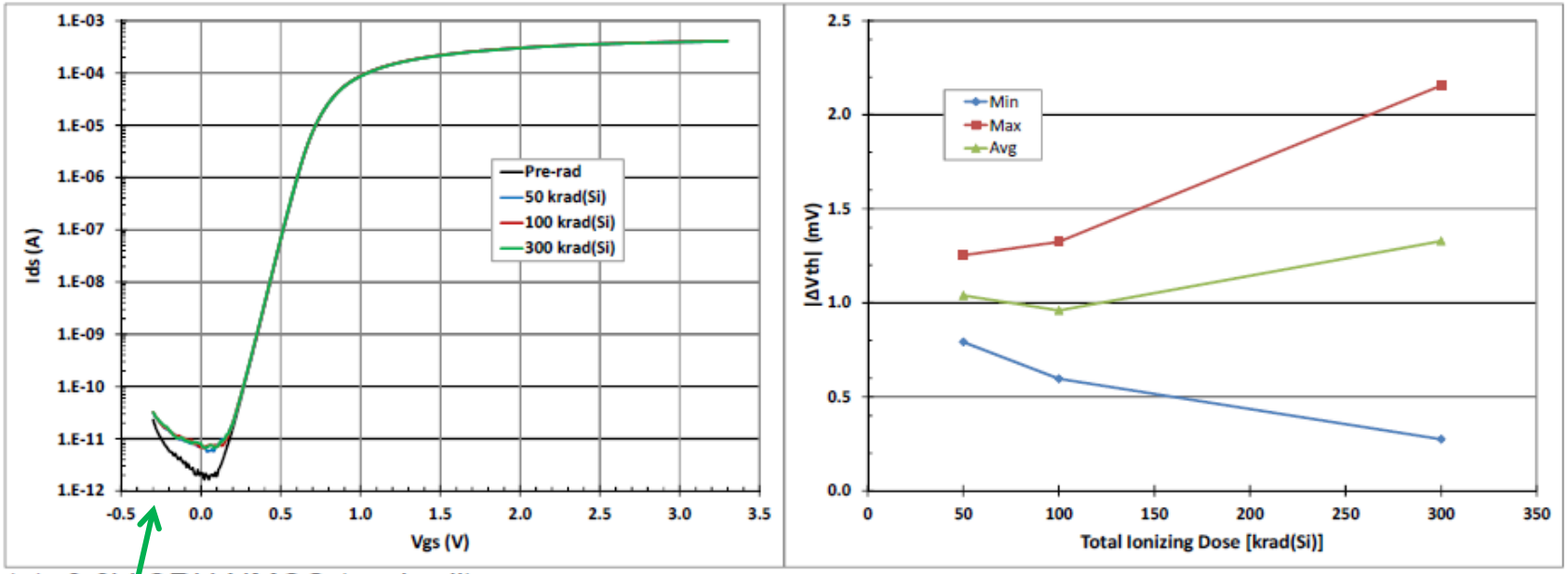
▼ Bias:

- **Worse case gate electric field (MOS capacitor)**

▼ Temperature:

- **22°C**

TID Results: Aeroflex 3.3V NMOS

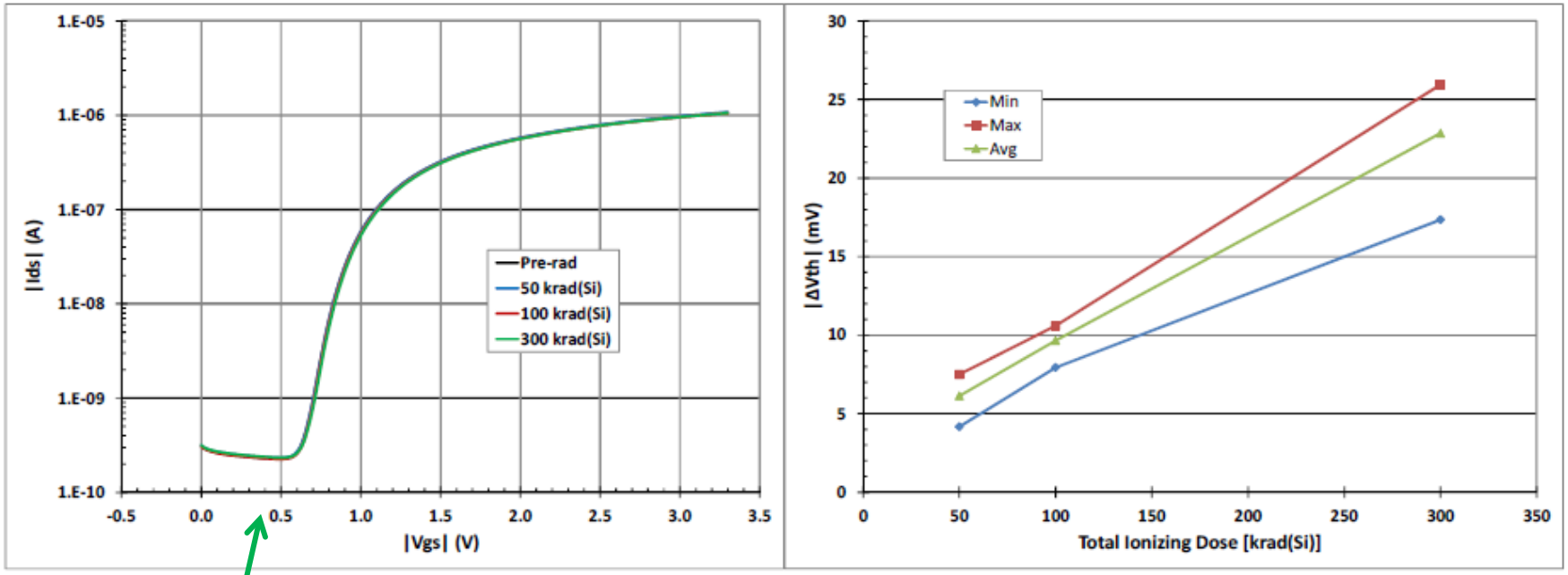


(a) 3.3V CRH NMOS (xnchadi)

Acceptable leakage increase up to 300krad(Si)

Threshold voltage shift < 1.5mV at 100krad(Si).

TID Results: Aeroflex 3.3V PMOS

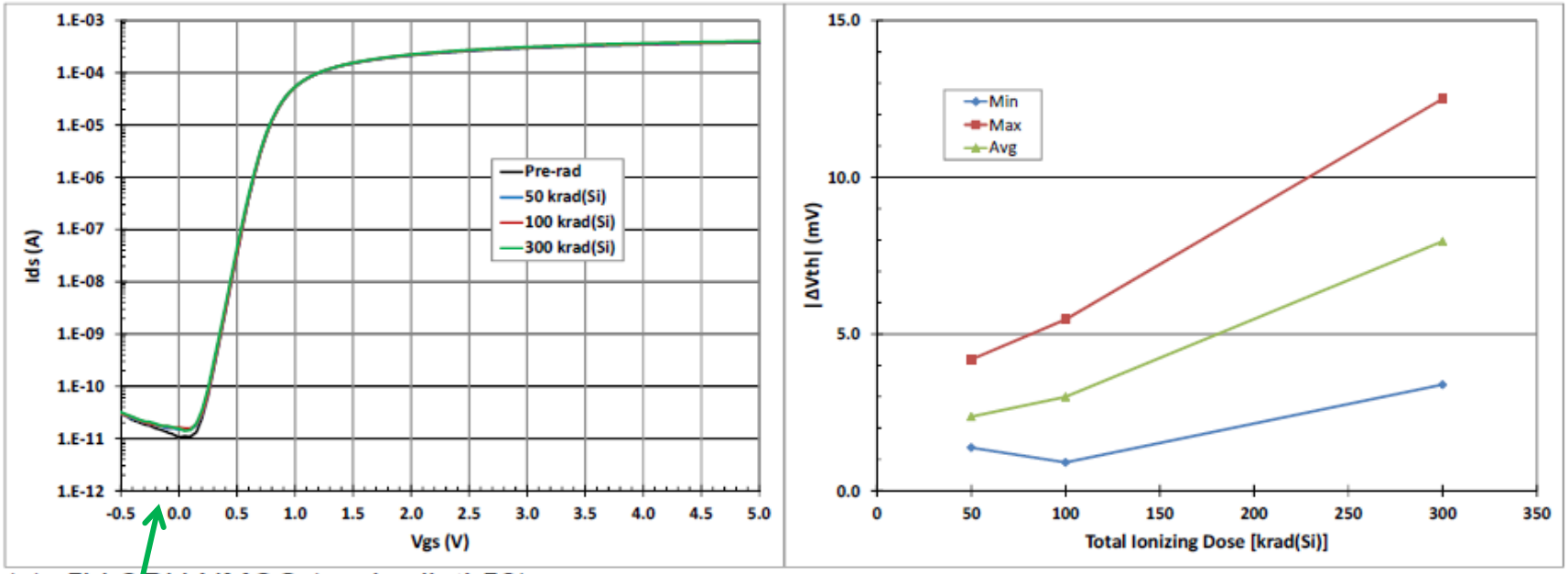


(b) 3.3V PMOS (xpchd)

No appreciable leakage increase up to 300krad(Si)

Threshold voltage shift < 12mV at 100krad(Si).

TID Results: Aeroflex 5V NMOS

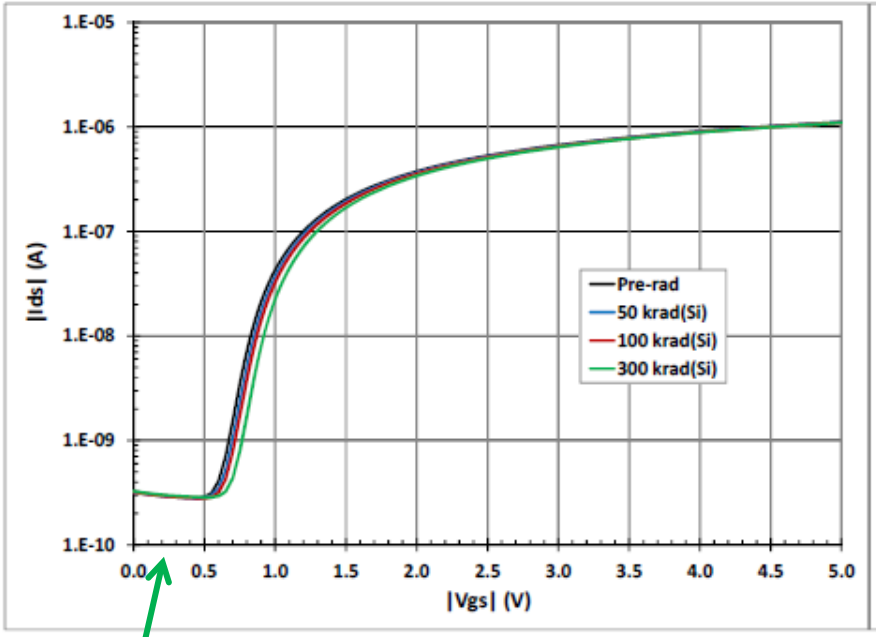


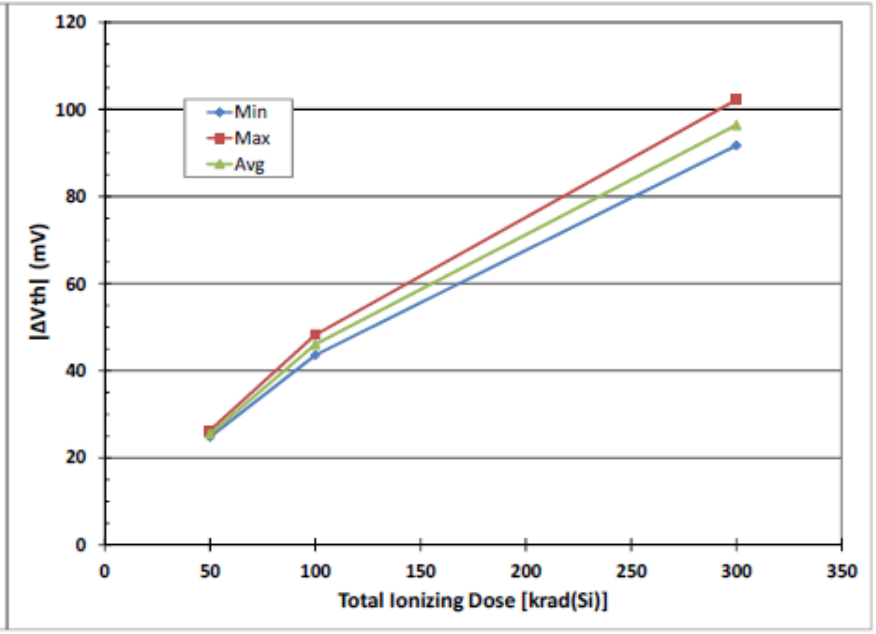
(c) 5V CRH NMOS (xnchadi_tk50)

No appreciable leakage increase up to 300krad(Si)

Threshold voltage shift < 6mV at 100krad(Si).

TID Results: Aeroflex 5V PMOS



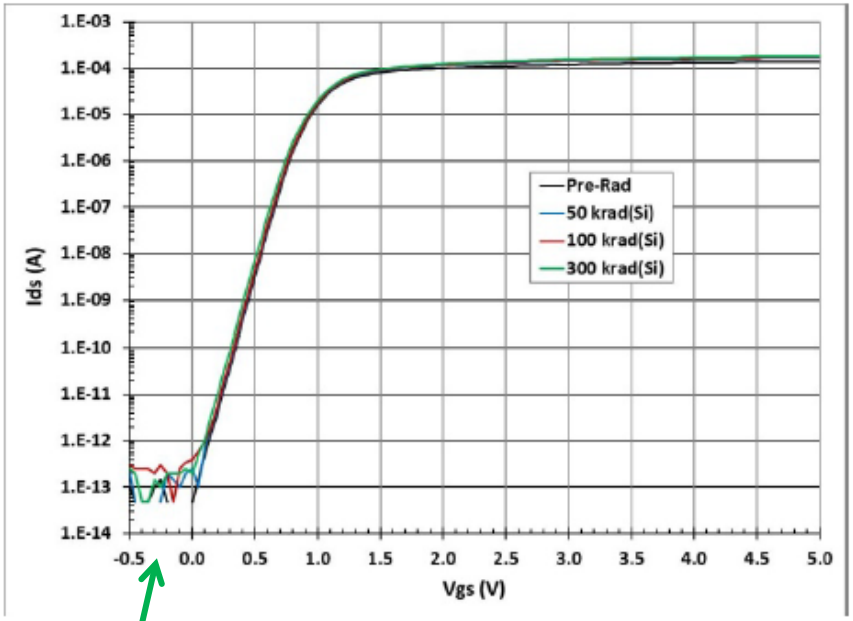


(d) 5V PMOS (xpchd_tk50)

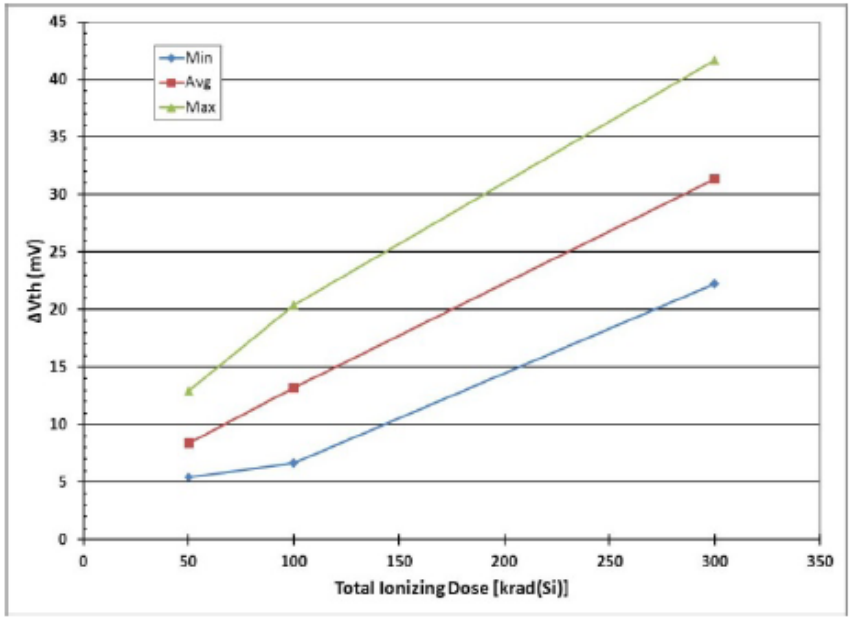
No appreciable leakage increase up to 300krad(Si)

Threshold voltage shift < 50mV at 100krad(Si).

TID Results: Aeroflex 40V nLDMOS



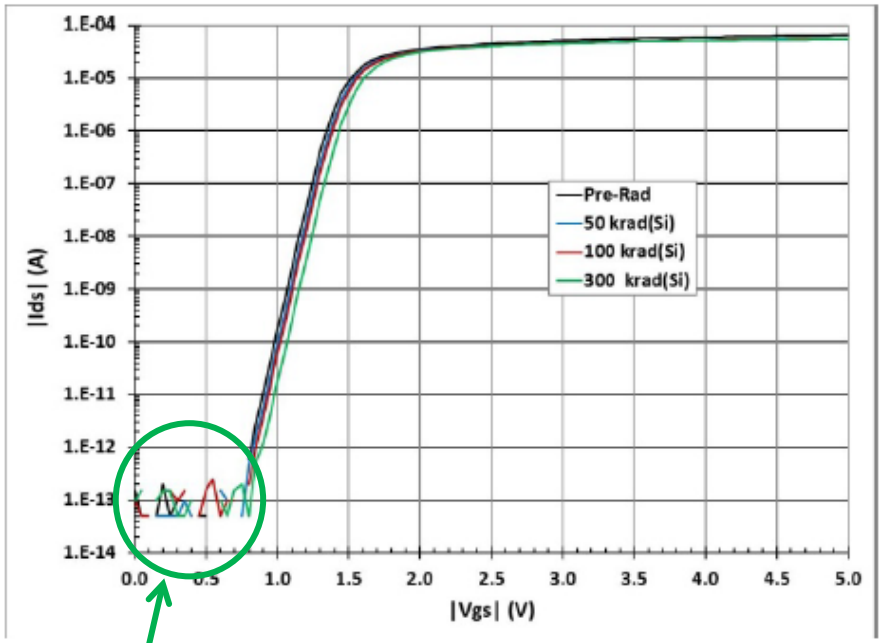
(a) 40V nLDMOS (xnchd_p40)



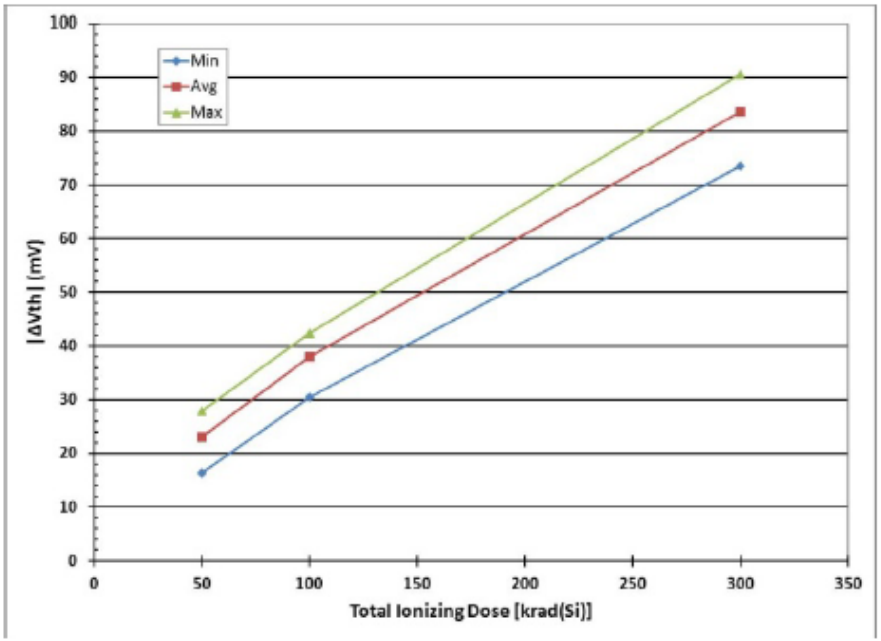
No appreciable leakage increase up to 300krad(Si)

Threshold voltage shift < 21mV at 100krad(Si).

TID Results: Aeroflex 40V pLDMOS



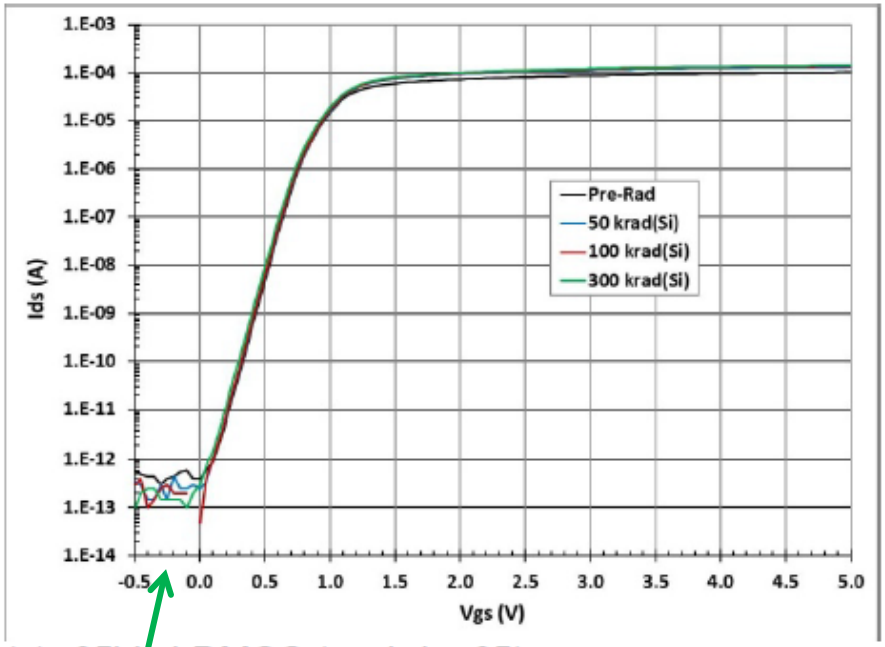
(b) 40V pLDMOS (xpchd_p40)



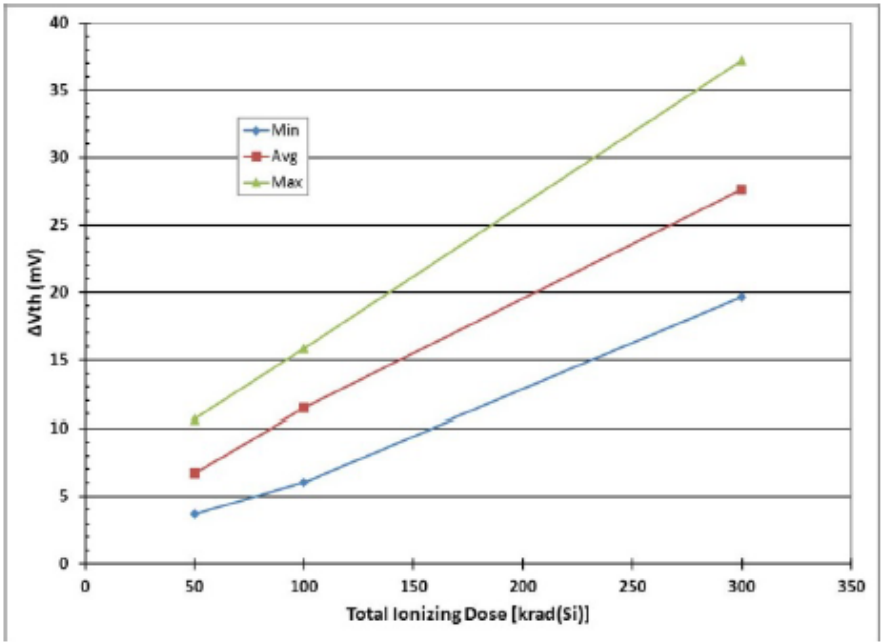
No appreciable leakage increase up to 300krad(Si)

Threshold voltage shift < 42mV at 100krad(Si).

TID Results: Aeroflex 65V nLDMOS



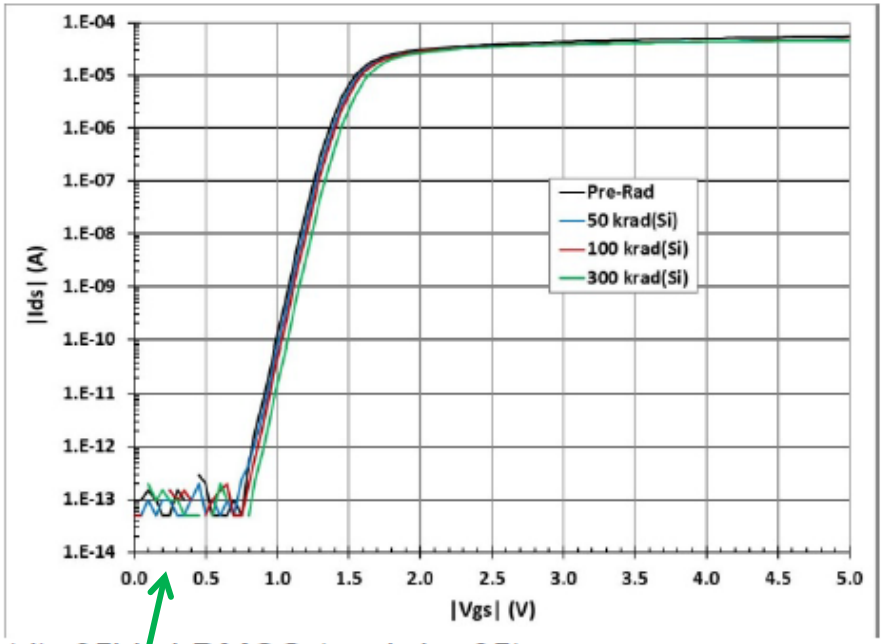
(c) 65V nLDMOS (xnchd_p65)



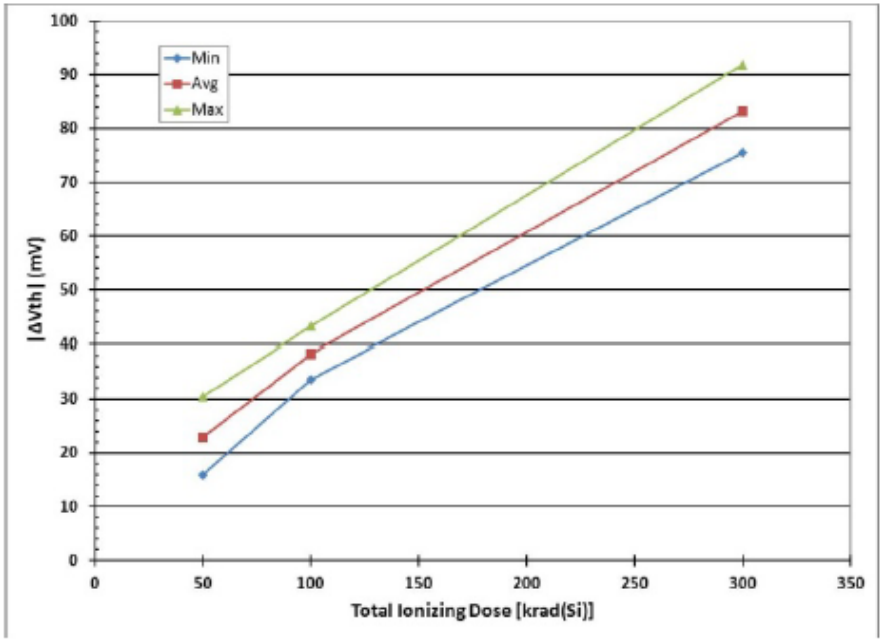
No appreciable leakage increase up to 300krad(Si)

Threshold voltage shift < 16mV at 100krad(Si).

TID Results: 65V pLDMOS



(d) 65V pLDMOS (xpchd_p65)



No appreciable leakage increase up to 300krad(Si)

Threshold voltage shift < 16mV at 100krad(Si).

Single Event Effects

Device Type	W (μm)/L (μm)/M
40V NLDMOS	10/0.2/1
40V PLDMOS	10/0.2/1
65V NLDMOS	10/0.2/1
65V PLDMOS	10/0.2/1

SEE Test Results

Run #	V_{DD} drain (V)	Temp. (ºC)	S/N	Device Type	Ion	Normal LET (MeV·cm²/mg)	Angle (°)	Effective LET (MeV·cm²/mg)	Pre-I_{DS} Current (mA)	Post-I_{DS} Current (mA)	Eff. Fluence (ions/cm²)	Damaged? y/n
1	35.2	125	2	40V PLDMOS	Xe	55.0	60	110	50.6	49.5	1.0E+7	n
2	35.2	125	3	40V NLDMOS	Xe	55.0	60	110	52.0	500.0	1.8E+6	y
3	35.2	125	3	40V PLDMOS	Xe	55.0	60	110	51.0	50.9	1.0E+7	n
4	35.2	125	4	40V PLDMOS	Xe	55.0	60	110	50.8	50.7	1.0E+7	n
5	35.2	125	4	40V NLDMOS	Xe	55.0	60	110	51.9	500.0	5.0E+4	y
6	35.2	125	5	40V NLDMOS	Xe	54.4	48	81	52.2	500.0	5.5E+4	y
7	35.2	125	6	40V NLDMOS	Xe	53.8	0	54	52.2	500.0	1.7E+4	y
8	40.0	125	6	40V PLDMOS	Xe	55.0	60	110	57.8	57.6	1.0E+7	n
9	5.0	RT	7	40V NLDMOS	Xe	55.0	60	110	0.136	0.137	1.0E+7	n
10	10.0	RT	7	40V NLDMOS	Xe	55.0	60	110	0.280	0.281	1.0E+7	n
11	15.0	RT	7	40V NLDMOS	Xe	55.0	60	110	0.430	0.430	1.0E+7	n
12	20.0	RT	7	40V NLDMOS	Xe	55.0	60	110	0.583	0.585	1.0E+7	n
13	25.0	RT	7	40V NLDMOS	Xe	55.0	60	110	0.741	0.742	1.0E+7	n
14	30.0	RT	7	40V NLDMOS	Xe	55.0	60	110	0.899	0.430	1.0E+7	y
15	30.0	RT	8	40V NLDMOS	Xe	55.0	60	110	0.879	0.899	1.0E+7	n
16	35.2	RT	8	40V NLDMOS	Xe	55.0	60	110	1.07	500.0	4.6E+5	y
17	35.2	RT	9	40V NLDMOS	Xe	55.0	60	110	1.1	486.9	3.1E+4	y
18	30.0	RT	11	40V NLDMOS	Xe	53.8	0	54	0.934	0.945	1.0E+7	n
19	32.0	RT	11	40V NLDMOS	Xe	53.8	0	54	1.011	1.018	1.0E+7	n
20	34.0	RT	11	40V NLDMOS	Xe	53.8	0	54	1.085	500.0	2.0E+6	y

SEE Test Results

- Damage depends primarily upon Vds voltage
  - May also depend upon cumulative ion fluence
- Damage occurs at normal incidence and at high angles
  - Vds Voltage more sensitive parameter than LET
- Failing voltage on 40 xLDMOS different (lower) than on 65V xLDMOS
  - Most likely not SEGR, as gate oxide is identical

Radiation Assessment by Market

Device Type	Voltage for Space Market (V)	Voltage for Medical Imaging Market (V)	Voltage for Nuclear Reactor and Radiation Therapy (V)
3.3V NMOS	3.6	3.6	3.6
3.3V PMOS	3.6	3.6	3.6
3.3V i-NMOS	3.6	3.6	3.6
5V NMOS	5.5	5.5	5.5
5V PMOS	5.5	5.5	5.5
5V i-NMOS	5.5	5.5	5.5
40V NLDMOS	< 30	40	TBD
40V PLDMOS	40	40	TBD
65V NLDMOS	TBD	65	TBD
65V PLDMOS	TBD	65	TBD

Life Test Data: Baseline 0.35µm

▼ Extended Life Test Results:

Device	Assembly Lot	Wafer Lot	Date Tested	Temperature (°C)	Life Test Hours	Samples/Failures
YB06B	QL2115	SLC0830R1	7/21/2010	150	2,000	46/0
YB06B	QL2116	SLQ0902	7/21/2010	150	2,000	46/0
YB06B	QL2007	SLR0337R1	7/21/2010	150	2,000	46/0
YA31B	QL3455	SLQ1302	4/29/2011	150	2,000	46/0
YA25B	QL3766	SLD0984	9/1/2011	150	2,000	46/0
TOTAL				**150**	**2,000**	**230/0**
TOTAL	**Equivalent Use Hours**			**125**	**4,195**	**230/0**
TOTAL	**Equivalent Use Hours**			**55**	**60,872**	**230/0**

Life Test Data: Baseline 0.35µm

▼ Long Life Test Results:

Technology	Number of Devices	Number of Device Hours	Device Hours for V_{DD}max, 125°C Use Condition	Device Hours for V_{DD}max, 55°C Use Condition	Number of Fails	Failure Rate, 125°C, FITS (60% UCL)	Failure Rate, 55°C, FITS (60% UCL)	Reliability Goal, Failure Rate at VDDmax, 125ºC Use Condition
MagnaChip 0.35um	784	712,785	1.62E+07	2.67E+08	0	56.6	3.4	10.0

1 FIT = 1 x 10^{-9} failures per hour (1 ppb/hr)

Failure Rate Estimate limited only by statistics.
Zero failures to date → more life testing should yield lower failure rate.

A Note on Recent Changes to US Export Laws

- **Before Jun 27, 2014**
  - **5 radiation criteria *OR* specially designed**
- **After Jun 27, 2014**
  - **5 (new) radiation criteria *AND* specially designed**

Summary

- **Radiation Performance Differences in available BCD devices MANDATE Separate libraries/pdks for different applications.**
- **Baseline 0.35µm CMOS Process:**
  - **300krad(Si) (and higher) up to 5.5V for all market applications**
  - **QML-V Qualification since June 2012**
  - **Demonstrated Failure Rate < 3.4 FITS 55ºC, Max. Vdd**
- **BCD 0.35µm CMOS:**
  - **300krad(Si)) (and higher) for voltages up to 65V**
  - **SEE Results determine max voltage for each market application**
  - **QML-V Qualification 2H 2015**