Mixed-Signal Design Methodology for Various Radiation Environments with Applications to a 0.35μm, 65V Quadruple-Well BCD Technology

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Abstract

There is a need for high voltage (>5V <100V) mixed-signal integrated circuits (ICs) in a variety of applications having ionizing radiation environments, such as satellite/space, medical diagnostic imaging, nuclear power control & monitoring, and radiation oncology therapy. In some of these environments, the ionizing radiation includes ions (space, proton therapy) while in others, there the ionizing electromagnetic radiation is accompanied by neutrons (nuclear power, radiation therapy). Designing to the worse case radiation environment can impose severe design limitations that result in higher power, poorer performance, and higher cost than is really necessary for the intended application. We discuss a unified design flow where different radiation environments are accommodated (but not over-accommodated) by the use of distinct sets of design rules, cell libraries, and design tools.

I. Introduction

After selection of a target wafer fabrication technology, the process of installing market-specific process design kits (pdk) begins with the design and fabrication of a technology characterization vehicle (TCV). The TCV contains at least one (but usually several) instantiations of each active and passive device that are intended to be used by the designers. The fabricated TCV is packaged and electrical test data collected for each device type, e.g. drain current (Id) vs gate voltage (Vg) and Id vs drain voltage (Vd) curves for metal oxide semiconductor (MOS) transistors of various channel lengths (L) and widths (W). Devices are then irradiated using either x-rays or gamma rays to a give total ionizing dose (TID) level, and the same electrical data immediately collected after irradiation.

Sequential digital cells are designed to meet the single event upset (SEU) requirements of the given application environment. The SEU rate is predicted a-priori by the use of two proprietary design tools, Qsim and SETsim, that were described previously [1,2]. The SEU rate is then validated by irradiating the TCV containing such cells, typically configured in large memory arrays, with heavy ions and/or protons as appropriate at various values of linear energy transfer (LET) up to ~110 MeV cm^2/mg. Several, distinct libraries are then created, each having a TID and single event latch-up (SEL) rating for each cell, a digital single event transient (DSET) for each non-sequential cell, and an SEU rating for each sequential cell. In this way, each of the distinct libraries has an overall rating for radiation environment.

Neutron testing is also performed for cells to validate their use in nuclear reactor environments. Analog/Mixed-Signal cells are designed to meet certain recovery times for analog SET (ASET). An analog-to-digital converter (ADC) might have a design target of ASETs having duration of less than two sample clocks for an LET < 40 MeV cm^2/mg. Comparators may be rated by the on-set LET that causes a false reading when the input is within, e.g. 10mV of the trip-point, etc.

Using the a-priori rating system (with validation by TCV testing), completed mixed-signal libraries are formed, labeled and segregated as to their possible radiation environments. The program manager and product development team select the proper mixed-signal library based upon the specification for the mixed-signal IC.

Throughout the rest of this paper, we use the example of a 65V quadruple-well, 4 level metal (4LM) Bipolar-CMOS-DMOS (BCD) process, containing isolated 3.3V CMOS devices in addition to 40V and 65V LDMOS devices.

II. TID Test Procedures

The radiation source used for this testing is an Aracor 4100 X-ray irradiation source and microprobe station. This system produces X-rays with energies ranging from 10 keV to 60 keV a peak energy at 10 keV with dose rates ranging from 2 to 200k rad(Si)/min.. Irradiations for this study occurred at 3,000 rad(Si)/sec. Four high voltage TCV devices were irradiated and tested at room temperature (T = 22 °C ± 6 °C) as shown in Table I. All devices were tested within one hour after X-ray exposure. Stepped X-ray total ionizing dose (TID) values were 50 krad(Si), 100 krad(Si), and 300 krad(Si). All MOS devices were biased statically during X-ray exposure with 110% of the nominal, maximum Vgs applied to the device. NMOS devices used accelerated gate-to-body (gate-to-channel) biasing in a MOSCap type configuration. PMOS devices used the "inverter off" configuration with the gate, body and source tied to 110% of the nominal Vdd and the drain grounded.

Table I: High Voltage TCV Devices

Device Type	W (μm)/L (μm)/M
40V NLDMOS	10/0.2/1
40V PLDMOS	10/0.2/1
65V NLDMOS	10/0.2/1
65V PLDMOS	10/0.2/1

III. TID RADIATION TEST RESULTS

Figure 1 shows Id-Vg data for the Aeroflex-designed 40V NLDMOS devices in a 0.35 µm quadruple-well BCD technology for TID levels of 0, 50, 100, and 300 krad(Si). The minimum, average, and maximum threshold voltage shift from the population of devices irradiated as a function of TID is shown in Figure 2. Figures 3 and 4 show the Id-Vg and the minimum, average, and maximum threshold voltage shifts for the 40V PLDMOS device respectively. Figures 5 and 6 show the Id-Vg and the minimum, average, and maximum threshold voltage shifts for the 65V NLDMOS device respectively. Figures 7 and 8 show the Id-Vg and the minimum, average, and maximum threshold voltage shifts for the 65V PLDMOS device respectively.

As can be seen for Figures 1, 3, 5, and 7, there is no appreciable change in the subthreshold slopes of any of the Id-Vg curves, and that the transistor off leakage (Idoff) is essentially the same as the pre-irradiation values of leakage for all four high voltage device types.

As can be seen in Figures 2, 4, 6, and 8, the threshold voltage shifts for the PLDMOS devices is about twice as great as for the NLDMOS devices. The maximum NLDMOS threshold voltage shifts was less than 25 mV for both the 40V and 65V devices, while the maximum PLDMOS threshold voltage shift was less than 95 mV for both the 40V and 65V devices.

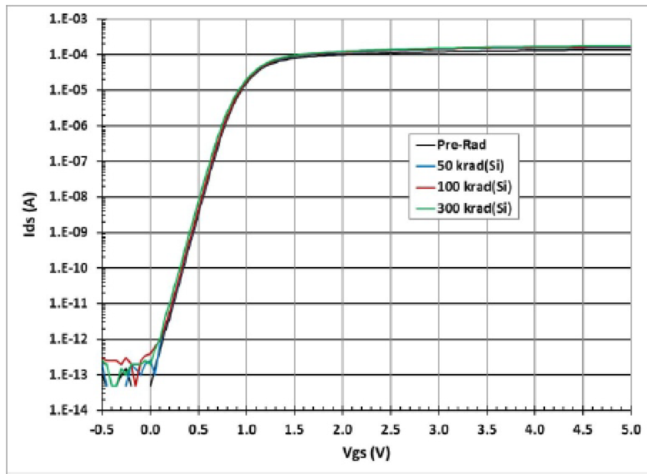

Figure 1: Id-Vg Curves for the 40V NLDMOS Device

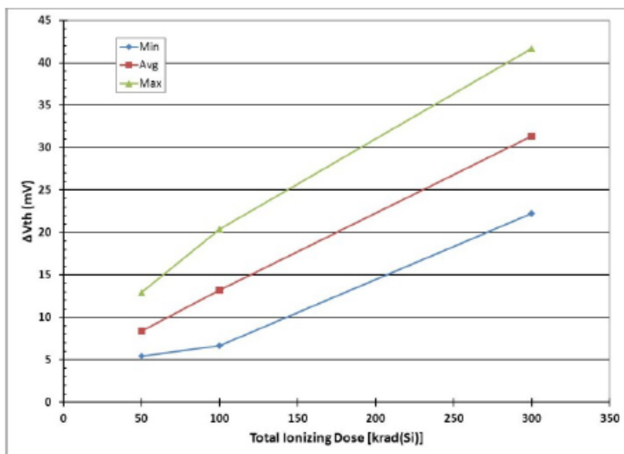

Figure 2: Minimum, Average, and Maximum Threshold Voltage shift in the 40V NLDMOS Device

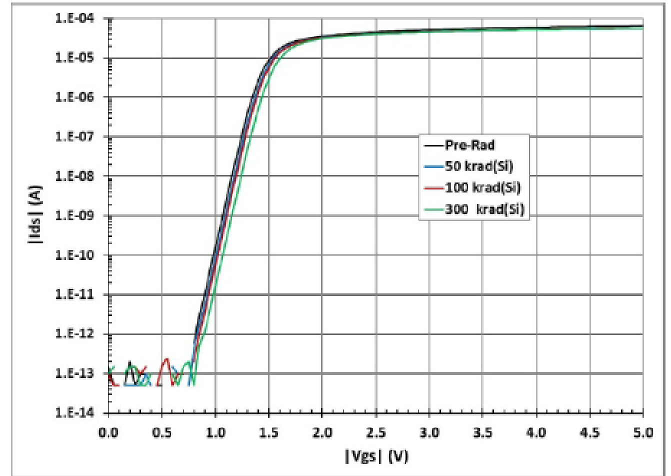

Figure 3: Id-Vg Curves for the 40V NLDMOS Device

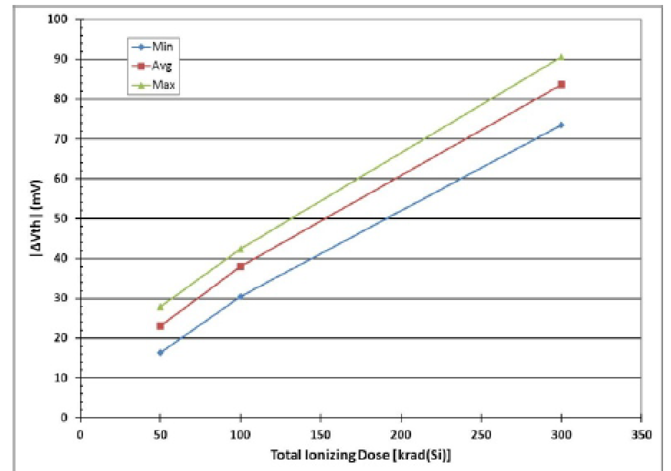

Figure 4: Minimum, Average, and Maximum Threshold Voltage shift in the 40V PLDMOS Device

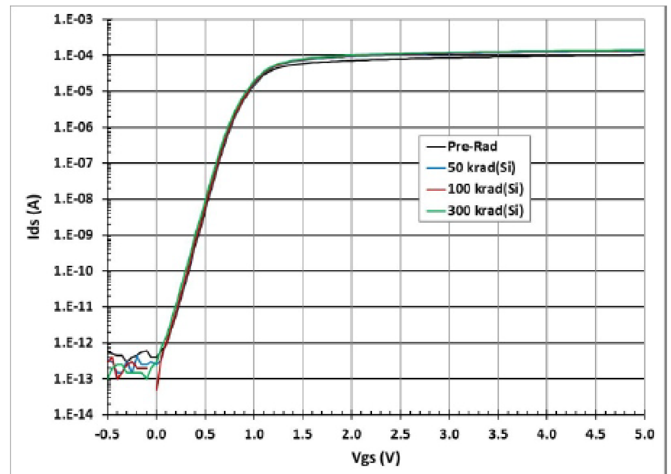

Figure 5: Id-Vg Curves for the 65V NLDMOS Device

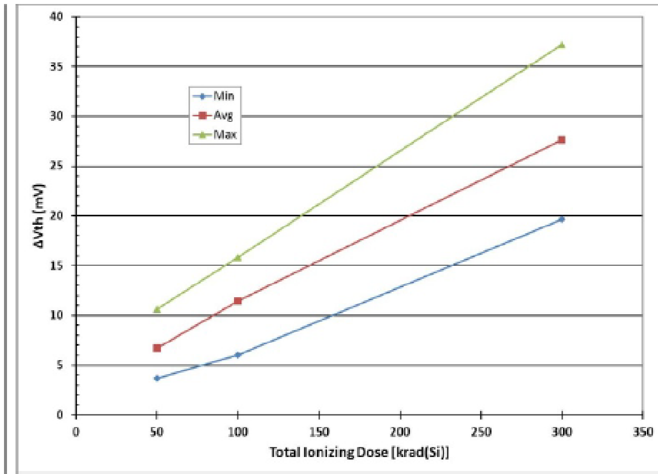

Figure 6: Minimum, Average, and Maximum Threshold Voltage shift in the 65V NLDMOS Device

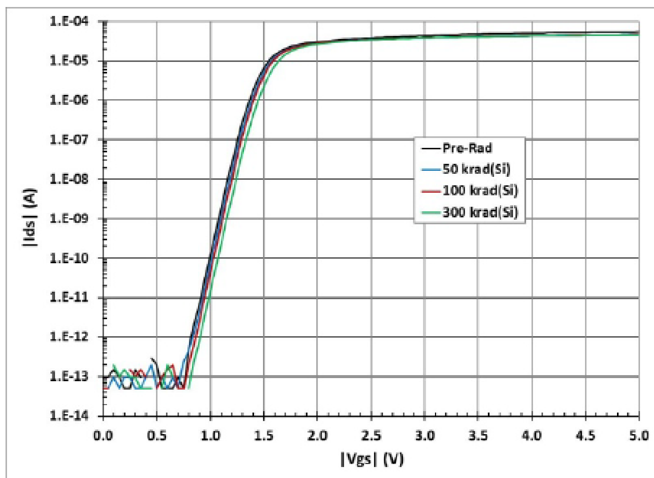

Figure 7: Id-Vg Curves for the 65V PLDMOS Device

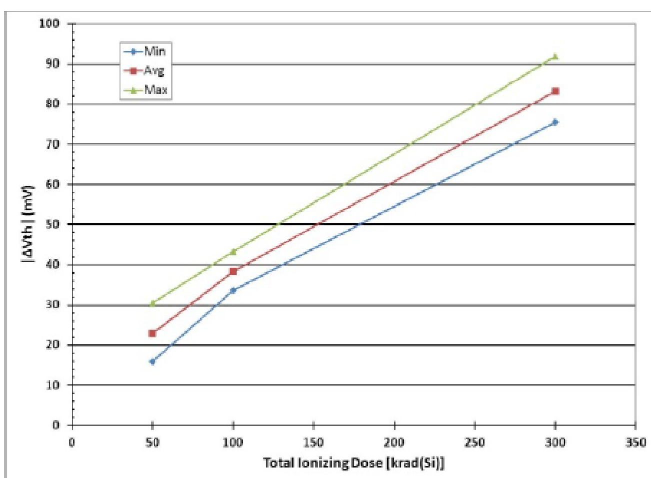

Figure 8: Minimum, Average, and Maximum Threshold Voltage shift in the 65V PLDMOS Device

III. Single Event Effects (SEE) Testing

SEE testing was performed at the Texas A&M University Cyclotron Facility on February 25, 2014. The 40V NLDMOS and PLDMOS were irradiated with broad-beam Xe ions for various drain voltages at either 125ºC or at room temperature (RT). The angle of the beam with respect to the device under test (DUT) normal was varied to vary the effective LET. The results are shown in Table II. As can be seen, all of the 40V PLDMOS devices performed well with a drain voltage of 35.2 and 40V (runs 1, 3, 4, and 8). The n-channel LDMOS devices (runs 2, 5, 6, 7, and 9 through 20), failed at drain voltages greater than 32V for a LET of 55 MeV cm_2/mg, and at voltages greater than 30V for a LET of 110 MeV cm_2/mg. (It should be noted that serial number 7, a 40V NLDMOS device, was irradiated six times to a fluence of 1E7 ions/cm^2 each irradiation, before it failed at a drain voltage of 30V with a LET of 110 MeV cm^2/mg and a cumulative fluence of 6E7 ions/cm^2. However a fresh device irradiated at a drain voltage of 30V with an effective ion LET of 110 MeV cm^2/mg to a fluence of 1E7 ions/cm^2 passed just fine.

IV. Discussion

The analysis of TID results in this technology indicates that the TID performance is acceptable for almost any market including medical imaging, space/satellite, nuclear reactor monitoring, etc. However, the 40V SEE data indicates that, while the 40V PLDMOS can operate up to its nominal value of 40V at the maximum LET of 110 MeV cm^2/mg, the NLDMOS is limited to ~30V or less for the space/satellite markets. Preliminary results on the 65V devices, still in test, indicate that some sort of de-rating for use in space is required.

Table III shows the available libraries in this technology, along with maximum voltages. While neutron testing has not yet been completed, we do not expect the same type of failures of the high voltage devices as seen with heavy ions.

Table III: Voltages by Market for 0.35 μm BCD Technology

Device Type	Voltage for Space Market (V)	Voltage for Medical Imaging Market (V)	Voltage for Nuclear Reactor and Radiation Therapy (V)
3.3V NMOS	3.6	3.6	3.6
3.3V PMOS	3.6	3.6	3.6
3.3V i-NMOS	3.6	3.6	3.6
5V NMOS	5.5	5.5	5.5
5V PMOS	5.5	5.5	5.5
5V i-NMOS	5.5	5.5	5.5
40V NLDMOS	30	40	TBD
40V PLDMOS	40	40	TBD
65V NLDMOS	TBD	65	TBD
65V PLDMOS	TBD	65	TBD

IV. References

[1] D.B. Kerwin, A. Wilson, Y. Lotfi, K. Merkel, and A. Zanchi, “MIXED-SIGNAL DESIGN METHODOLOGY USING A PRIORI SINGLE EVENT TRANSIENT RATE ESTIMATES”, *4th*

International Workshop on Analog and Mixed Signal Integrated Circuits for Space Applications (AMICSA 2012), 26 - 28 August 2012 ESA/ESTEC, Noordwijk, The Netherlands.

[2] D.B. Kerwin, A. Zanchi, A. Wilson, K. Merkel, J. Colley, “ADVANCES IN RADIATION HARDENED MIXED-SIGNAL TECHNOLOGY”, *4th International Workshop on Analog and Mixed Signal Integrated Circuits for Space Applications (AMICSA 2012),* 26 - 28 August 2012 ESA/ESTEC, Noordwijk, The Netherlands.

Table II: Summary of 40V N- and PLDMOS SEE Testing

Run #	V_{DD} drain (V)	Temp. (ºC)	S/N	Device Type	Ion	Normal LET (MeV·cm^2/mg)	Angle (°)	Effective LET (MeV·cm^2/mg)	Pre-I_{DS} Current (mA)	Post-I_{DS} Current (mA)	Eff. Fluence (ions/cm^2)	Damaged? y/n
1	35.2	125	2	40V PLDMOS	Xe	55.0	60	110	50.6	49.5	1.0E+7	n
2	35.2	125	3	40V NLDMOS	Xe	55.0	60	110	52.0	500.0	1.8E+6	y
3	35.2	125	3	40V PLDMOS	Xe	55.0	60	110	51.0	50.9	1.0E+7	n
4	35.2	125	4	40V PLDMOS	Xe	55.0	60	110	50.8	50.7	1.0E+7	n
5	35.2	125	4	40V NLDMOS	Xe	55.0	60	110	51.9	500.0	5.0E+4	y
6	35.2	125	5	40V NLDMOS	Xe	54.4	48	81	52.2	500.0	5.5E+4	y
7	35.2	125	6	40V NLDMOS	Xe	53.8	0	54	52.2	500.0	1.7E+4	y
8	40.0	125	6	40V PLDMOS	Xe	55.0	60	110	57.8	57.6	1.0E+7	n
9	5.0	RT	7	40V NLDMOS	Xe	55.0	60	110	0.136	0.137	1.0E+7	n
10	10.0	RT	7	40V NLDMOS	Xe	55.0	60	110	0.280	0.281	1.0E+7	n
11	15.0	RT	7	40V NLDMOS	Xe	55.0	60	110	0.430	0.430	1.0E+7	n
12	20.0	RT	7	40V NLDMOS	Xe	55.0	60	110	0.583	0.585	1.0E+7	n
13	25.0	RT	7	40V NLDMOS	Xe	55.0	60	110	0.741	0.742	1.0E+7	n
14	30.0	RT	7	40V NLDMOS	Xe	55.0	60	110	0.899	0.430	1.0E+7	y
15	30.0	RT	8	40V NLDMOS	Xe	55.0	60	110	0.879	0.899	1.0E+7	n
16	35.2	RT	8	40V NLDMOS	Xe	55.0	60	110	1.07	500.0	4.6E+5	y
17	35.2	RT	9	40V NLDMOS	Xe	55.0	60	110	1.1	486.9	3.1E+4	y
18	30.0	RT	11	40V NLDMOS	Xe	53.8	0	54	0.934	0.945	1.0E+7	n
19	32.0	RT	11	40V NLDMOS	Xe	53.8	0	54	1.011	1.018	1.0E+7	n
20	34.0	RT	11	40V NLDMOS	Xe	53.8	0	54	1.085	500.0	2.0E+6	y