Contribution ID: **31** Type: **Oral**

Mixed-Signal Design Methodology for Various Radiation Environments with Applications to a 0.35 μm, 65 V Quadruple-Well BCD Technology

Monday 30 June 2014 12:10 (20 minutes)

There is a need for high voltage (>5V <100V) mixed-signal integrated circuits (ICs) in a variety of applications having ionizing radiation environments, such as satellite/space, medical diagnostic imaging, nuclear power control & monitoring, and radiation oncology therapy. In some of these environments, the ionizing radiation includes ions (space, proton therapy) while in others, there the ionizing electromagnetic radiation is accompanied by neutrons (nuclear power, radiation therapy). Designing to the worst possible radiation environment can impose severe design limitations that result in higher power, poorer performance, and higher cost than is really necessary for the intended application. We discuss a unified design flow where different radiation environments are accommodated (but not over-accommodated) by the use of distinct sets of design rules, cell libraries, and design tools.

The process starts with technology selection and the design and fabrication of a technology characterization vehicle (TCV). The TCV contains at least one (but usually several) instantiations of each active and passive device that are intended to be used by the designers. The fabricated TCV is packaged and electrical test data collected for each device type, e.g. Id-Vg and Id-Vd curves for MOS transistors of various channel lengths (L) and widths (W). Devices are then irradiated using either x-rays or gamma rays to a give total ionizing dose (TID) level, and the same electrical data immediately collected after irradiation. For the first time Id-Vg data is measured for a 65 V NLDMOS in a 0.35 μm quadruple-well bipolar-CMOS-DMOS (BCD) technology for TID levels of 0, 50, 100, and 300 krad(Si), along with the minimum, average, and maximum threshold voltage shift from the population of devices irradiated as a function of TID. This type of data is used to generate compact transistor models that can be used in design simulations for various TID levels. Heavy ion data on these same transistors is used to define the safe operating area (SOA) for use in a space environment. For lower voltage transistors that would be used in the digital portion of a mixed-signal IC, a similar procedure is followed to generate models. In the final paper, we will present TID and single event effects data, for the first time, for 40V and 65V NLDMOS and PLDMOS devices fabricated in a 0.35 μm quadruple-well, 4LM BCD technology, showing SOA, SEL, and calculated ASET rates for select analog cells.

Sequential digital cells are designed to meet the single event upset (SEU) requirements of the given application environment. The SEU rate is predicted a-priori by the use of two proprietary design tools, Qsim and SETsim, that were described previously [1]. The SEU rate is then validated by irradiating the TCV containing such cells, typically configured in large memory arrays, with heavy ions and/or protons as appropriate at various values of linear energy transfer (LET) up to ˜110 MeV cm2/mg. Several, distinct libraries are then created, each having a TID and single event latch-up (SEL) rating for each cell, a digital single event transient (DSET) for each non-sequential cell, and an SEU rating for each sequential cell. In this way, each of the distinct libraries has an overall rating for radiation environment.

Neutron testing is also performed for cells to validate their use in nuclear reactor environments.

Analog/Mixed-Signal cells are designed to meet certain recovery times for analog SET (ASET). An analog-to-digital converter (ADC) might have a design target of ASETs having duration of less than two sample clocks for an LET < 40 MeV cm2/mg. Comparators may be rated by the on-set LET that causes a false reading when the input is within, e.g. 10mV of the trip-point, etc.

Using the a-priori rating system (with validation by TCV testing), completed mixed-signal libraries are formed and labeled as to their possible radiation environments. The program manager and product development team select the proper mixed-signal library based upon the specification for the mixed-signal IC. Verification that the expected radiation response will be achieved is accomplished using commercial and proprietary simulation tools, and validated by performing radiation testing on the prototype silicon. Several examples of products will be shown in the final paper.

[1] D.B. Kerwin, A. Wilson, Y. Lotfi, K. Merkel, and A. Zanchi, "MIXED-SIGNAL DESIGN METHODOLOGY USING A PRIORI SINGLE EVENT TRANSIENT RATE ESTIMATES", 4th International Workshop on Analog and Mixed Signal Integrated Circuits for Space Applications (AMICSA 2012), 26 - 28 August 2012 ESA/ESTEC, Noordwijk, The Netherlands.

Primary author: Mr KERWIN, David (Aeroflex)

Co-authors: Dr ZANCHI, Alfio (Aeroflex); Mr WALZ, Dale (Aeroflex); Dr MERKEL, Ken (Aeroflex)

Presenter: Mr KERWIN, David (Aeroflex)

Session Classification: Radiation Hardened Technology for Mixed-Signal IC

Track Classification: AMICSA 2014