RCADA - 65nm 12b 3Gspc Rad Hard dual ADC dual DAC

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Abstract

The RCADA mixed signal chip is currently under development by Ramon Chips and Silantrix, combining the rad-hard RadSafe™ libraries and methodologies from Ramon Chips and Silantrix proprietary architecture for data converters.

The extreme wideband capabilities of RCADA require very high performance digital processing, as well as high bandwidth digital communication capabilities. The digital processing capability will be provided by RC64, Ramon Chips' many-core DSP processor, which is under development. The two devices will be integrated in a multi-chip module (MCM). The key capabilities of RC64 will be presented [1].

RCADA will be provided either as standalone device, or integrated with RC64 in a single MCM package, to form is a multi-purpose data converter that aims to support the majority of high performance applications in advanced space missions including telecommunication, SAR, beam forming, navigation and earth observation.

RCADA integrates two matched ADC cores, 1.5Gsps 12b each, which can be interleaved, forming a single 3.0Gbps 12b ADC. Similarly, it includes two DAC cores, which can be configured as either a dual 1.5Gbps 12b DAC or as a single 3.0Gbps DAC. It can also be configured as a single ADC and a single DAC, 1.5Gbps 12b each, operating simultaneously. Within the MCM, RCADA interfaces RC64 via 48 pairs of bi-directional LVDS buffers, operating at 750Mbps each. RCADA will be fabricated using 65nm CMOS technology. It will operate with 1.2V and 2.5V supplies. Target power consumption is less than 500mW. It will provide very high immunity to TID and to latchup and no sensitivity to single event effects.

I. INTRODUCTION

Data converters are needed for wide range of space applications. Some applications require high sampling rate, which typically consume high power, and some require high resolution. Since the space market is relatively small, data converters that provide solution for wide range of applications is highly desired.

Analog circuits, such as used in data converters, might demonstrate degradation of performance due to TID stress. The advanced silicon technologies, such as 65nm, are more prone to these effects due to the use of thin gate oxide and thin STI between devices. However, this advanced process is more sensitive to NBTI effect, which might degrade the performance after aging. Self calibration capability complements the mitigation of these effects by performing periodic correction of INL/DNL inaccuracies, extending the effective lifetime of the devices.

In typical RF systems, the high speed electronics is placed close to the antennas, and long transmission lines, carrying analog signals, which are sensitive to noises and interferences, connecting them to the data converters in the main system board. By converting the high speed analog signals to digital close to the antennas, and compressing the digital data by high performance digital processor, it is possible to transfer the digital data with limited number of traces, to long distance, without degradation of signal quality. Mixing the RC64 - high performance DSP, with high performance data converter will enable such application.

Current high speed data converters for space are processed with fairly obsolete process flows, and the high speed capabilities are achieved by using Bipolar or BiCMOS technologies, or by using high speed circuit techniques, such as CML. These techniques consume a significant amount of power. For improved INL/DNL performance it is necessary to use a large device, which increases the area, thus limit the bandwidth, and high current is necessary to compensate for that. The use of advanced process technology, such as 65nm CMOS, enables very fast digital processing and conventional digital design flow. Implementing the analog core with smaller devices, provide higher speed and reduced INL/DNL accuracy. However, complementary digital mechanism that corrects these inaccuracies in the analog circuits provides the optimum solution, and exceeding the traditional Figure Of Merit (FOM) rules for data converters.

The use of 65nm cell libraries, complemented by proprietary RadSafe™ Rad Hard By Design (RHBD) libraries, which provides very high immunity to all radiation effects, enables high speed, low power and high immunity to radiation effects.

Most of the data converters available today are using one type of converter, DAC or ADC, and uni-directional data flow. The integration of ADC and DAC in the same die enables the self calibration, enables configuring the direction of the data flow between the data converter and the processor, thus providing unified solution for wide range of applications. In addition, it enables optimizing the cost of inventory to the system companies, and unified screening and qualification flow to the component vendor.

II. Micro architecture of RC64

The RC64 processor micro-architecture is described in Figure 1. It is currently at advanced design phase. It integrates 64 DSP cores, with can operate simultaneously, as controlled and scheduled by as S/W controlled scheduler. Each one of the cores can access to any of the 256 shared memory banks. When operating with clock frequency of 250MHz it can reach the peak performance of 16GIPS (???).

The RC64 can interface other systems by either 12 ports of 3.125Gbps SERDES, DDR2/3 I/F, configurable direction LVDS port, 2 SpaceWire ports and synchronous and asynchronous Flash I/F. In addition, it integrated JTAG I/F for testing.
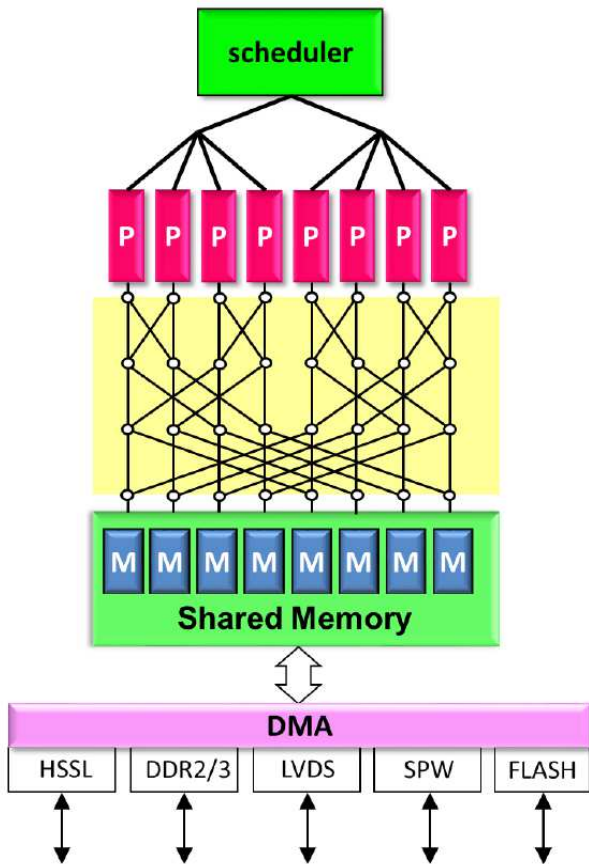
III. Micro architecture of RCADA

The micro architecture of RCADA is described in Figure 2. 48 LVDS signal pairs, with configurable direction, will connect the RCADA to the processor, such as RC64. The data rate is 750Mbps/pair in DDR mode, or 375Mbps in SDR mode. The maximum transfer rate is 36Gbps, or 3Gsps with 12 bit resolution.

Two ADC cores, 1.5Gsps 12b each, are connected to external terminated pairs. Both are sharing the same voltage and timing references, and same resistor ladders, thus provide fully matched and synchronized digital outputs. Such matching is necessary, for example, when sampling the I and Q channels in RF communication. When shorting the inputs of both ADC pairs, and configuring the ADC to operate in interleaving mode, ADC0 will sample at clock rising edge, and ADC1 will sample at clock falling edge, doubling the data rate.

Similarly, the DAC can operate at either dual 1.5Gsps, or single 3Gsps when shorting the two DAC output pairs. It is possible to activate ADC0 and DAC1 simultaneously, thus enabling single ADC/single DAC operation, at 1.5Gsps each.

The key features of the ADC are:

- Muxing of parallel data by 1X/2X/4X @interleave mode
- Maximum data rate – 3Gsps
- Maximum data rate on LVDS outputs - 750Mbps/pair
- Resolution - 12 bit; ENOB - >10 bit
- Power @3Gsps - <500mW

The key features of the DAC are:

- Muxing of parallel data by 1X/2X/4X @interleave mode
- Maximum data rate - 3Gsps
- Maximum data rate on LVDS inputs - 750Mbps/pair
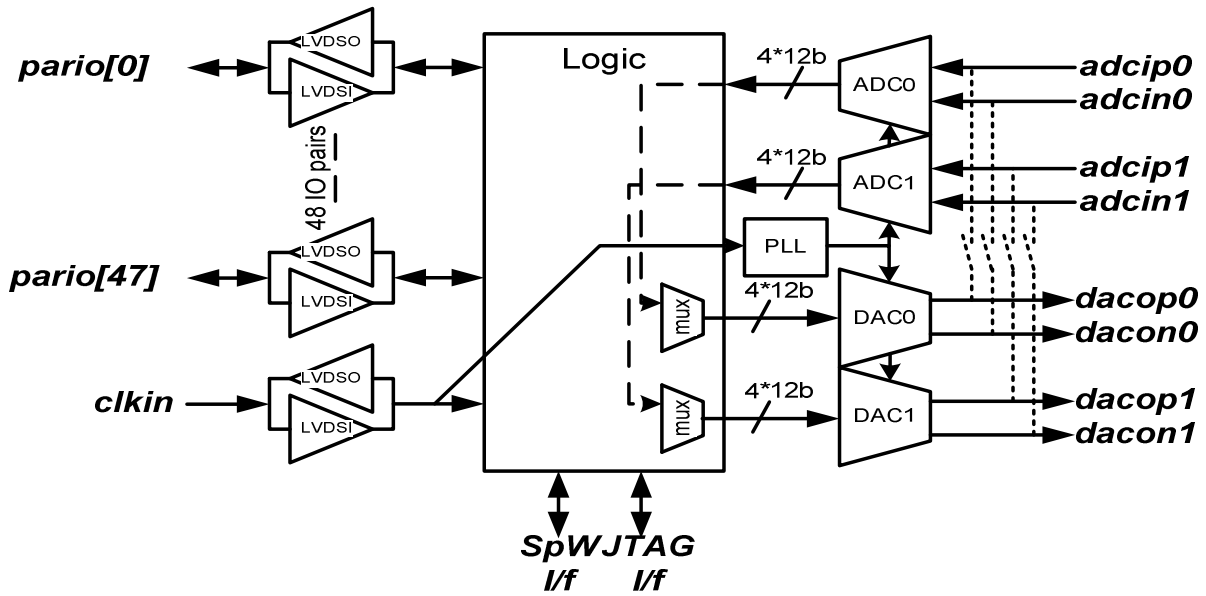- Resolution - 12 bit; ENOB - >10 bit
- Power @3Gsps - <500mW

Figure 2: Micro-architecture of RCADA

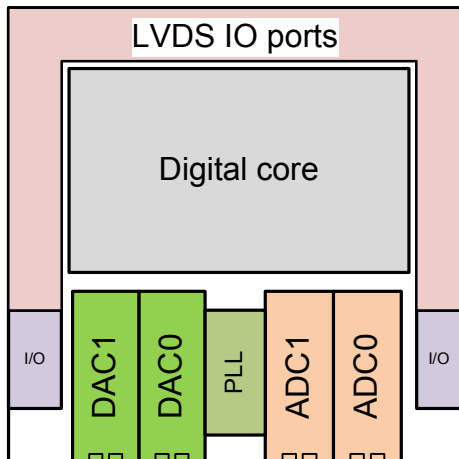The floor plan of the RCADA is presented in Figure 3.

Figure 3: Floor plan of RCADA chip

The DAC0 and DAC1 are placed adjacent to each other to enable sharing the references for improved matching. Similarly, ADC0 and ADC1 are also adjacent to each other. The PLL is multiplying the clock reference to the desired sampling frequency. The frequency of the ADC and DAC is the same, to enable the periodic self calibration.

IV. DIGITAL MODEL INVERSION

The use of Digital Model Inversion (DMI), which is a proprietary technology by Silantrix Ltd., is mandatory for achieving the high performance data conversion process.

In conventional ADCs, the sampler is providing an accurate conversion of each analog sample to its digital equivalent. This requires very small variance of transistor's parameters, and also very low capacitance, which are conflicting requirements. With DMI, the sampler can be less accurate, compromising the performance for speed, power and area. The digital representation of the input analog signal can be calculated. There is no need to calibrate the sampler for

inaccuracy of its devices, since it is done digitally. This characteristic can compensate not only for process variations, but also to stress related changes in device parameters, such as NBTI or TID. More specifically, the gains and offsets of the sampler are not modified in order to achieve digital representation of the sampled analog signals featuring better accuracy. There is still need for some calibration, but only for insuring those values are in their proper range.

The digital processor, which is part of the digital core, reconstructs the signal from the inaccurate analog sampler, providing accurate results. The reconstruction algorithm, which uses mostly adders, is design by conventional design flow. The use of 65nm process, with high speed rad-hard cell library, operating at 1.2V, provides the low power, high speed, noise insensitive, fully testable solution.

V. COMPETITIVE ANALYSIS

The expected performance of the RCADA is compared to the existing available data converters available in the market. The highest performance ITAR free data converters for space available today are from E2V. The comparison table between the existing components and the expected performance of RCADA is presented in Table 1.

Table 1: Comparison between existing data converters and RCADA

	EV10AS180AGS	EV10AS180AGS	RCADA (target)
Function	ADC	DAC	2*ADC+2*DAC
# of bits	10	12	12 (each)
ENOB	8÷8.4	8.6÷9	>10
Sample rate	1.5Gbps	3Gbps	2*1.5Gbps /3Gbps (each)
Power	1.75W	1.3W	<0.5W

VI. Mitigation of radiation effects

The impact of TID on 1.2V devices of 65nm is expected to be very low. It is affecting mostly the digital logic. The analog circuits, which are powered mostly at 2.5V, are well guard ringed. In addition, the self calibration mechanism will compensate for variations caused by NBTI or TID.

SEL is not expected at 1.2V domains when using 65nm process technology and libraries with taps in each cell. In the 2.5V domains, the guard rings are expected to provide the required immunity.

SEU/SET in the logic parts are mitigated by using RadSafe^{TM} library, which is well protected for these effects. The analog sampler of the ADC might be affected by SET. This effect will be partially mitigated by the digital processing. The fact that the data is temporary makes SEU related errors less critical. In communication channels, such errors are corrected and/or detected by using the error handling mechanisms embedded in the communication protocols.

VII. Summary

RCADA is a high performance rad-hard dual ADC and dual DAC device, with significantly higher performance than the existing available data converters.

It will be offered either as stand alone, or integrated with RC64 many-core DSP processor in a single MCM package. It will enable significant optimization of space systems, like SAR, beam forming and more.

VIII. References

[1] R. Ginosar et al, DASIA 2012, "RC64: A many-core high-performance digital signal processor for space applications"

[2] US20060222128 patent, Aug 2004, " Analog Signal Sampler Providing Digital Representation Thereof"