CMOS Analog Front End Design for Particle Energy Measurement in Space Environment

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Abstract

In situ studies of the geospace environment, including space weather monitoring, is mainly based on the measurements of particles and fields. The particle content of the Earth's magnetosphere is studied with electron and ion detectors in various energy ranges, from the cold and dense eV solar wind to the MeV radiation belts. Here, the in situ high-energy (50 keV to 725keV) electron measurement is targeted. The design and development of space embedded electronic equipment require a specific approach. An Analog-Front-End (AFE) design methodology is proposed to optimize noise, bandwidth, consumption, crosstalk and radiation hardness performances of such AFEs for Si semiconductor detectors. The conception of an Analog-Front-End optimized in noise, bandwidth, consumption, crosstalk and radiation hardness, dedicated to a silicon (SiA) detector. Each channel includes an 8 bits successive approximation register (SAR) ADC in order to digitize

the incident electron energy. The chip was designed in a 0.35 µm HV CMOS process. The ASIC measurements have shown that for a charge range of 0.6 fC to 32 fC , the charge-to-voltage conversion gain is approximately 60 mV/fC. The equivalent noise charge (ENC) is 3119 e- for 40pF input parasitic capacitance while consuming 2.5 mW. The circuit can perform measurements up to a 650 kHz rate. The next step is to characterize the ASIC associated with the SC detector in a vacuum chamber. Furthermore, the total ionisation dose (TID) and the single event effect (SEE) tolerances must also be evaluated.

I. INTRODUCTION

Particle instruments incorporate sensors that are used to convert particle energy into quantifiable electrical charges. These sensors with their corresponding analog electronics circuits, also called Analog-Front-End (AFE), form detection channels called "sensor heads" [1-3]. The necessity to improve both spatial and spectral resolutions requires the design of multichannel integrated electronics. Thus, space-borne detectors with Application Specific Integrated Circuits (ASICs) should be developed. These integrated circuits allow not only to perfectly adapt the readout circuits to each sensor in order to optimize performances but also to benefit from the various advantages inherent to the use of monolithic technologies: reduced power consumption, smaller size, shorter transit time signals [4] and higher integration [5].

However, specific design methodology should be employed in order to withstand constraints due to space applications. The radiation environments can especially damage electronic systems on spacecraft and orbital satellite [6-7;16]. Nowadays, instead of using CMOS technologies dedicated to space (such as specific BiCMOS or SOI) in order to improve the radiation hardness of integrated circuits, it seems appropriate to use specific design techniques (radiation hardening by design (RHBD)) [7-8] applied on standard CMOS technologies which are less expensive [9], provide higher performances and for which parasitic effects are studied and well known [10-11]. Knowing the duration of the mission as well as its corresponding radiative environments, an 0.35 µm CMOS technology was chosen because it can naturally withstand more than 50 krad [8] and provide high enough dynamic ranges as its standard operating supply voltage is 3.3V. Note that a previously designed AFE allowed us to assess the TID behaviour of this technology [17]. The tests showed that the ASIC tolerates doses up to 360 krad without any relevant impact on the performance (degradation of the amplifier by the increase of leakage currents). In addition, to protect circuits from latchup, the extensive use of guard rings is required. Furthermore, in order to minimize crosstalk which can cause faulty detections, reduce the ASIC sensitivity, and improve power supply rejection, isolated-well technology process option was used. This feature is usually provided by High Voltage (HV) technologies where the transistors have almost the same characteristics as the ones used in the standard technology. Therefore, a 0,35 µm CMOS HV technology has finally been chosen.

Once the technology is chosen, it is necessary to perfectly understand the detector and propose an equivalent electrical model of the detector before design the ASIC. With this aim, the GEANT4 simulator is used to model the various physical effects associated with particles interacting within semiconductor detectors. The number of generated electron-hole pairs can thus be estimated as a function of the incident particle energy. Further, the main electrical characteristics of the sensor such as its charge collection time, its parasitic capacitance as well as its leakage current, can also be retrieved to correctly create an equivalent electrical model of the detector. With this aim, a sensor based on semiconductors (SCs) is presented in section 2.

Then, a description of the designed AFE that should linearly quantify the amount of detected charges in order to reconstruct the electron energy spectrum is given in section 3.

Finally, in section 4, ASIC experimental results are presented.

II. THE DETECTOR MODEL

The detector is an electron energy spectrometer based on semiconductors. This instrument is intended to analyze the atmosphere-ionosphere-magnetosphere interactions during Transient Luminous Events (TLE) that can occur during atmospheric storms, in order to understand the physical mechanisms responsible for vertical impulsive coupling between the atmosphere and the ionosphere. The final aim is to assess the impact of these phenomena on the earth environment [12]. The purpose of the instrument is to provide a high resolution electron energy spectrum with its corresponding angle distribution. It is designed to measure electron energy in a wide range of fluxes. For instance, these fluxes can range from ~1 to 106 $cm^{-2}.s^{-1}$ for the 70-100 keV energy level inside the low altitude radiation belt, including the South Atlantic Anomaly, and from 1 to 5.10^{2} $cm^{-2}.s^{-1}$ for the 4 MeV energy level which are reached during terrestrial gamma flashes (runaway electron beams). The instrument consists of two spectrometers, each having a maximum view angle of 30°x150°. The instrument is covered with an aluminium foil of 6 µm thickness to stop any incoming stray photons (~ 100% and 70% mitigation of respectively 1 keV and 5 keV soft x-rays). This foil also stops the protons with energies below 600 keV.

In order to detect the particle energy within this range, the use of semiconductors (SCs) of different kinds is necessary. By using different ionization energy SCs as well as different semiconductor thicknesses, each particle within the required energy range can be stopped while providing a linear charge amount. Therefore, stacking different kind of SCs allows not only to analyze a larger energy spectrum but also to use the method of coincidence in order to determine the direction of arrival of the particle. Here, the detection heads are made of two superposed plates of SCs to measure both the energy and the trajectory direction of electrons. The top plate is made of silicon (Si) and the bottom one of Cadmium Telluride (CdTe) with ionization energy per e/h pair of 3.6 and 5 eV respectively. The use of these two SCs allows to characterize the electrons over the whole energy range (from 60 keV to 4 MeV). Si can detect energies from 10 keV to 500 keV and CdTe starts stopping energetic particles beyond 500 keV up to 4 MeV.

The Si detector is divided in five cells: four large cells called Si A (10 mm × 10 mm) and one smaller cell called Si B (0.4 mm × 10 mm) placed in the centre. This SiB cell is required to avoid saturating the instrument in the South Atlantic Anomaly and to improve the determination of the electron trajectory when the detector is working in coincidence mode between Si and CdTe. The CdTe detector consists of 64 CdTe cells of 10 mm x 10 mm. This CdTe matrix is used to detect the electrons that completely traverse the Si plate.

The complete response of a given semiconductor to an energetic electron beam is difficult to predict because many physical effects occur (probabilistic domain). However, GEANT4 software (for GEometry ANd Tracking) [13-14], developed by CERN, can be used to predict all these interactions. Both the SCs geometry and thickness are key input parameters for GEANT 4. The amount of electron-hole pairs produced by incident electrons can be obtained using Monte Carlo simulations over the whole electron energy range. The GEANT4 results are presented in the following paragraph.

A. *Simulation results*

The 3D and cross sectional views of the detector are represented in figure 1.

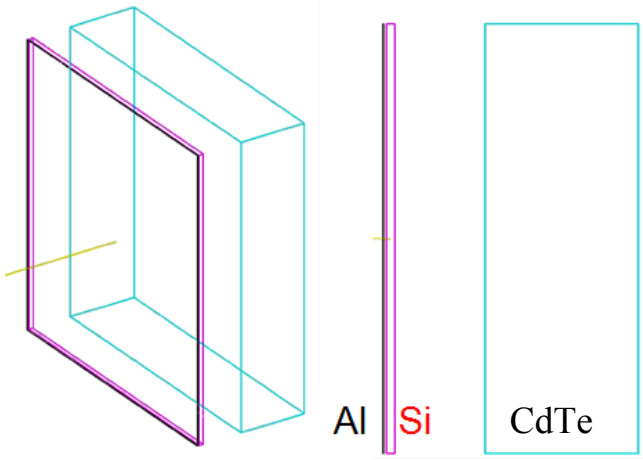


Figure 1: 3D (left) and sectional (right) diagrams of both cells forming the SCs detector and covered by aluminium foil.

Once the design of the detector is completed, Monte Carlo simulations are run to assess its performances for different incident electron trajectory angle and energy. These simulations allow to take into account all the physical phenomena that can occur along the particle path through detector. The thicknesses of both kinds of SCs can thus be tuned in order to obtain the required energy detection ranges [6]. The Si and CdTe thicknesses are d=0.3 mm and d=5 mm respectively. Note that electrons with an energy level lower than 10 keV cannot cross the aluminium foil. From energy higher than 500 keV, electrons traverse the Si and start to lose their remaining energy in the CdTe. Up to 4 MeV, the CdTe captures completely the electrons. For energy levels higher than 4 MeV, the bremsstrahlung effect starts to be significant [15]. For the most energetic electrons > 6 MeV, the emission of bremsstrahlung is dominant and as a result, the electrons can pass through the CdTe. Note also that the simulations take into account the effects of the photons generated by electrons (Compton scattering, photoelectric effect...). However, such events are too rare at these energy levels to noticeably influence the detector response. The number of electron-hole pairs, $n_{e\text{-}h}$ generated in the semiconductors by an incoming electron that transmits an energy E_{lost} to the semiconductor, is given by:

$$n_{e-h} = \frac{E_{lost}}{E_I} \qquad (1)$$

with E_I the ionization energy (energy per pair) of the absorbent material.

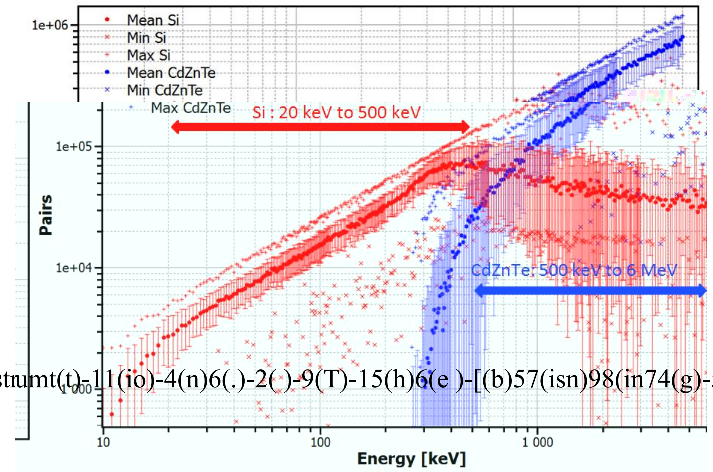
B. *Output response*

Using GEANT4, the energy loss along the incoming electron path can be computed for each SC. Consequently, using eq.(1), the total n_{e-h} generated within each SC can be deduced. As GEANT4 uses physics probabilistic models, Monte Carlo simulations need to be run in order to statistically characterize n_{e-h} as a function of the incident electron energy ranging from 10 keV to 6 MeV. In Fig. 2, the mean, standard deviation, maximum and minimum number of pairs generated in each SC are represented with Si and CdTe thicknesses of d=0.3 mm and d=5 mm respectively. It can be observed that the semiconductor response to incoming electrons is sufficiently linear to retrieve the electrons incident energy from the number of pairs generated in the detector in specific ranges. The linear energy range of the Si is [20 keV - 500 keV] (Fig. 2). Within this range for d=0.3 mm, the average number of pairs n_{pairs_Si} generated is defined as:

$$n_{pairs\_Si} = 166\, E_{in} - 683 \qquad (2)$$

where E_{in} is the energy of the incident electron in keV.

To define the charge input range of the AFE, the minimum and maximum values observed for each SC are taken into account to avoid any loss of information. Si can generate 1.10^4 to 2.10^5 electron-hole pairs.



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the holes at the cathode and the electrons at the anode. Table 1 summarizes the estimated characteristics of the SiA detectors found.

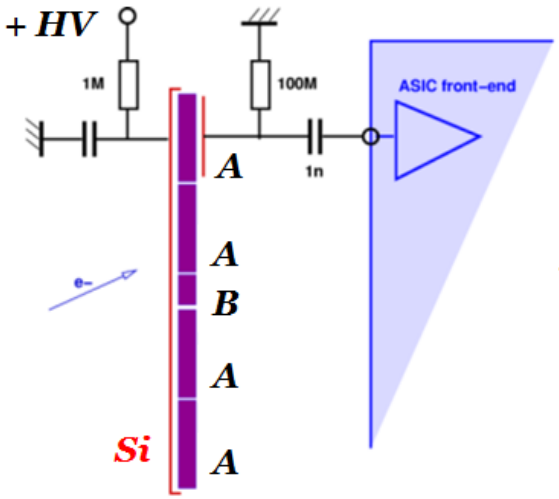

Figure 3: Biasing circuit of the Si cell (type A) and connection to the electronic "front-end".

Based on the previous detector analysis, Si cells can be modelled by a pulse current source I_{det} to simulate a charge injection Q_{in} in parallel with the equivalent capacitor C_{det} of the cell. Also, leakage current I_0 estimated is included in this model by a constant current source at this value.

Table 1 : Characteristics of the Si detectors used in the instrument

Characteristic	Symbol	Si A
Size (mm)	$L \times l \times d$	10×10×0.3
Pairs range (e^- ou e^+)	-	$1{,}4\times10^4$ to 2×10^5
Equivalent charge (fC)	Q_{in}	2.2 to 32
Collection time (ns)	t_c	50
Equivalent capacitor (pF)	C_{det}	34.8
Leakage current (nA)	I_0	2
Anodes number	-	4

III. ANALOG FRONT END DESIGN

The first step is to convert charge into a voltage using a charge preamplifier (CPA). The CPA consists of a transconductance amplifier (OTA) with a feedback capacitance C_f to perform the charge integration. Then, in order to improve the Signal-to-Noise Ratio (SNR), the CPA output voltage is filtered by a circuit called pulse shaper (PS). These two blocks are widely used in the type of application [1-3; 18]. Therefore, the analog-to-digital converter (ADC) input signal noise is reduced, which thus decreases the detection threshold level and increases the AFE achievable precision. To save power as well as reduce the influence of any external parasitic signals, analog-to-digital conversions of the CPA+PS output should be performed within the same chip. Thus, each channel has the following architecture: a CPA+PS, a comparator with an adjustable threshold voltage level, a peak detector (PD) and an 8 bits Successive Approximations Register (SAR) ADC. To summarize, the CPA+PS converts the incident charge into a proportional voltage and the comparator detects if the incoming charge is higher or lower than the desired threshold level. Note that the minimum detection threshold level can be obtained by setting the threshold voltage of the comparator just above the noise floor. The PD is used to store the maximal peak value of the PS output voltage, which is proportional to the electron energy. This stored voltage is then digitized by the SAR ADC. A control logic block of the system is also designed to manage the communications between the blocks. The AFE schematic is represented in Fig.4 and the design of the SiA AFE has been detailed in [19].

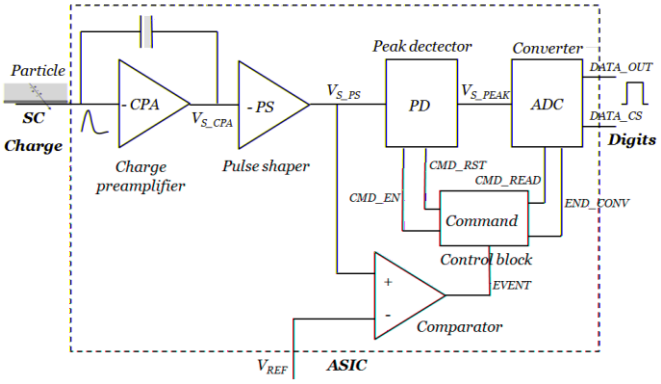

Figure 4: AFE conversion system to measure the transmitted energy by an incident electron in a SC detector.

IV. MEASUREMENTS AND PERFORMANCES

The AFE have been implemented in a CMOS HV 0.35 µm technology. Fig. 5 shows the layout view of the SiA channel (CPA+PS (1), discriminator (2) and ADC (3)). Each channel occupies a surface area of approximately 0.21 mm². To reduce crosstalk, analog and digital circuit wells are separated from each other and the corresponding circuits have their own power supplies VDD and GND (implementation of insulated wells, only available in BiCMOS or HV technologies).

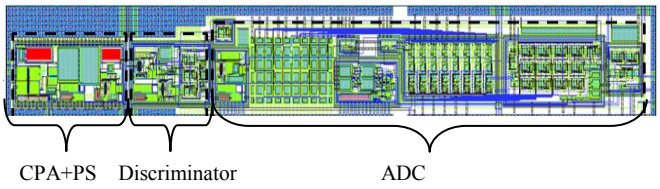

Figure 5: Die layout of the SiA channel implemented in a CMOS HV 0.35 µm technology.

On the analog test blocks, the measured value of the shaping time is 105 ns. Also the measured power consumption for one Si channel is 2.5 mW including static and dynamic power consumption of CPA+PS, discriminator and ADC.

The linearity of the system can be evaluated by analyzing the ADC output. Its dynamic range is 44 dB with a linearity

error of less than 0.32 %. Then the particle detection delay, which corresponds to the time between the arrival of the charge and the start of its conversion at the output of the ADC (DATA_CS = '1'), can be estimated by observing the outputs of the SiA channel (DATA_OUT and DATA_CS) for a 50 ns (T_(C_MAX)) input charge of 22.35 fC (see Fig. 6)corresponding to the digital output '10101001'. The measured detection delay is equal to 320 ns. The ADC conversion time is 1 µs and the reset time of the digital blocks is 200 ns. So, the final effective operating frequency of the chains is approximately equal to 650 kHz.

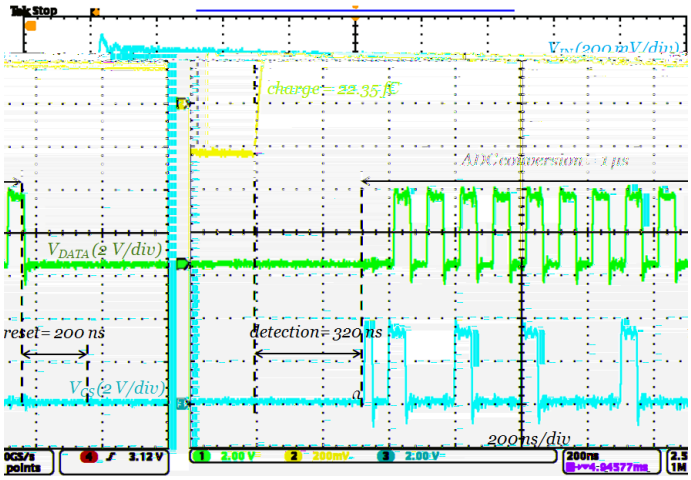

Figure 6: ADC outputs measurement (DATA_OUT and DATA_CS) of the Si A channel conversion for a 50 ns input charge of 22.35 fC and C_{det} = 40pF.

The linearity is plotted in Fig. 7 obtained for 50 acquisitions for each charge step and averaged over three different ASICs. The conversion gain is 57.7 mV.fC^{-1} with an ENC of 3119 e$^-$ (or 0.5 fC) in the linear region and the saturation value is approximately 32 fC for linearity errors less than 0.81%. The minimum detectable value is approximately 0.6 fC which is different from the measured ENC values. That is explained by the fact that the detection thresholds are affected by the noise mass supply of the PCB.

Crosstalk measurements similar to those made in [17] have shown that crosstalk is non-existent. So using an isolated-well technology (HV) and a differential pair in the CPA bring a major interest in the integration on a multichannel same chip.

In Table 2, the specifications, the simulated and measured data are summarized for the SiA channel. Measurements are very close to simulations which validate our design methodology.

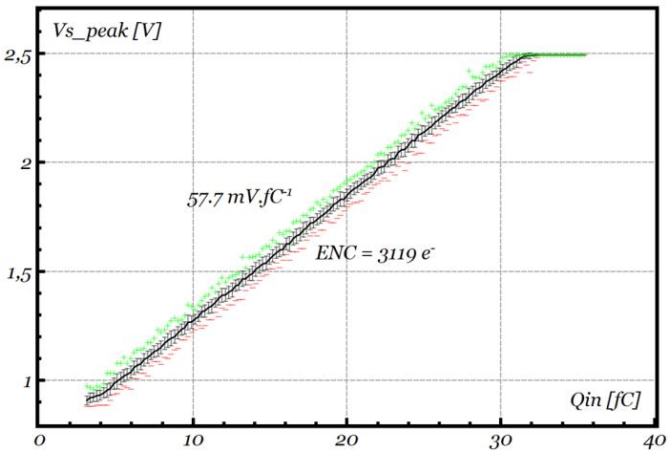

Figure 7: Linearity of the SiA channel deduced from the output of the 8-bit ADC, for 50 acquisitions, 3 ASICs and Q_{in} varying between 0.6 fC and 35 fC (C_{det} = 40pF). Averages (line), standard deviations (error bars), maximum (green +) and minimum (red -) values of 50 measures by step.

Table 2 : Summarize of SiA instrumentation channels performances

	Specifications		Measurements
Input charge range (fC)	0,6 to 32	0.53 to >32	0.6 to 32
Detector capacitance (pF)	40		

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