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Radiation-Tolerant High-Voltage ASIC Library Evaluation for Space Applications

Airbus DS / ID-MOS / CNES

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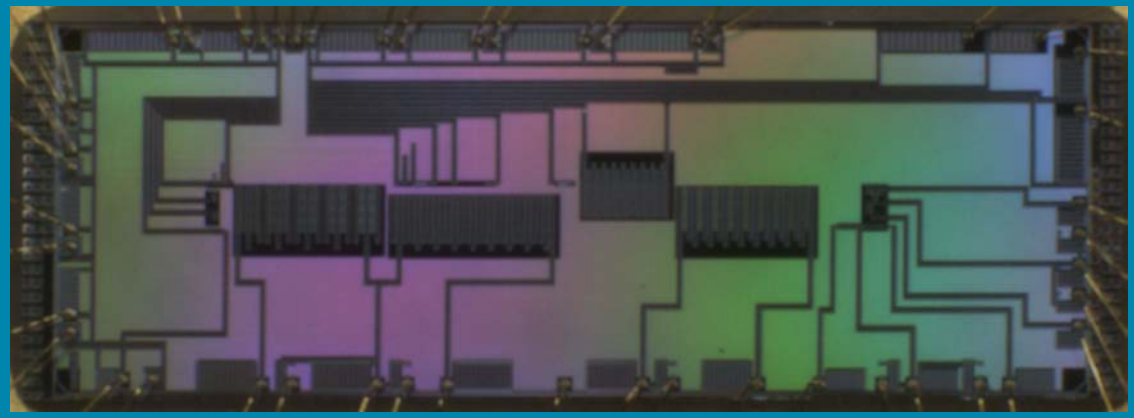

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Content

- This research and development project is performed for the Neosat project under a CNES contract with Airbus DS as prime contractor and ID-MOS as partner for ASIC design

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Context

- Objective: To reduce weight, cost and volume of platform electronics for observation and telecom satellites by integrating recurrent functions in mixed ASIC

- Airbus DS selected, with partners and CNES, the XFAB XH035 mixed-signal technology for its modularity and high-voltage extensions.

- This technology targets automotive, telecommunication and power management markets; therefore it has been widely used and tested for various applications and is a mature technology with a good perenniality

- A rad-tolerant library has already been designed for the XH035 standard LV (Low Voltage) process by IDMOS under a previous CNES contract.

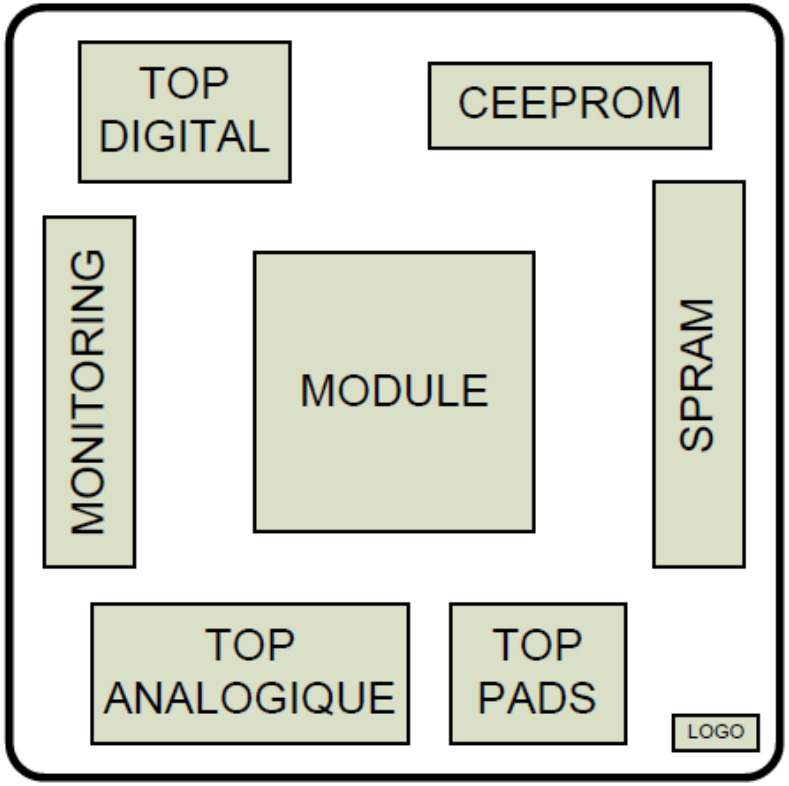
The HV process vs the LV process

- The HV process has the same design rules as the LV process for low voltage structures as the digital cells (< 3,3V).

- But the XH035 HV process differs from the standard process by:
  – A thick or medium gate oxide .
  – its deep epitaxial layer

→ It is necessary to re-test the digital cells against SEL and TID because of the epitaxial layer change.

- This has been done using the same test vehicle as LV contract but manufactured with HV process



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Design of the rad tolerant HV transitors and pads

- 22 N and P transistors have been selected in XFAB library amongst the various types :
  - 14 NMOS (nmos, nha, nmva, nhv, ngmmv, ndha, nmosia, ndhc, ndhe, ndhg, nhvg1, ndhc1, ndhe1,ndhg1)
  - 8 PMOS (pmos, pmva, phv, pgmmv, pmosia, phvb, phvd, phvf)

- These transistors have been hardened using an enclosed layout (ELT) and guard rings. Structures have also been used to break leakage paths.

- The medium gate oxide should be less sensitive than the thick gate oxide against TID effect. But the thick gate oxide has been chosen due to its better expected immunity to SEGR (Single Event Gate Rupture).

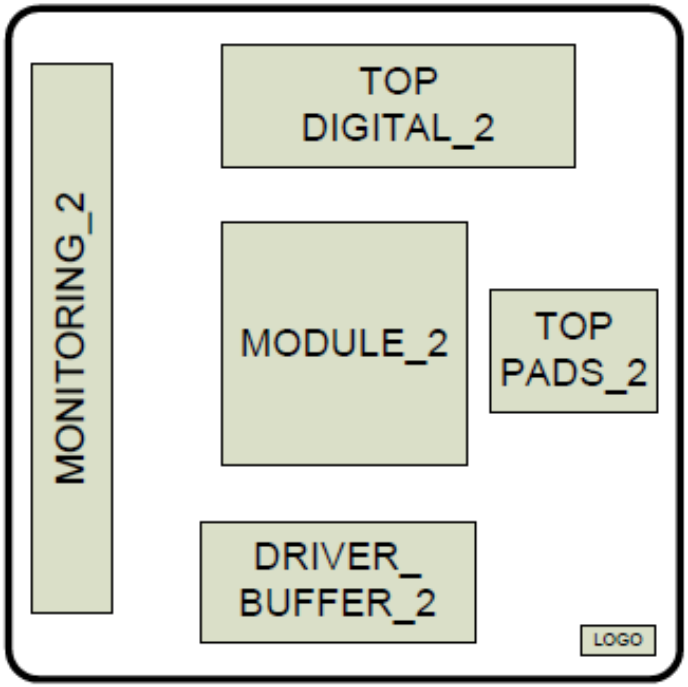
- Other structures have been designed and hardened:
  - Power output buffers (18 V, 45 V, 70V, 90 V), with 100 mA current driving capacity & their associated driver
  - Logic isolated basic cells (Not, Nand gates, etc…),
  - Logic isolated structures (Ring Oscillator),
  - PADs (HV and LV PADs),

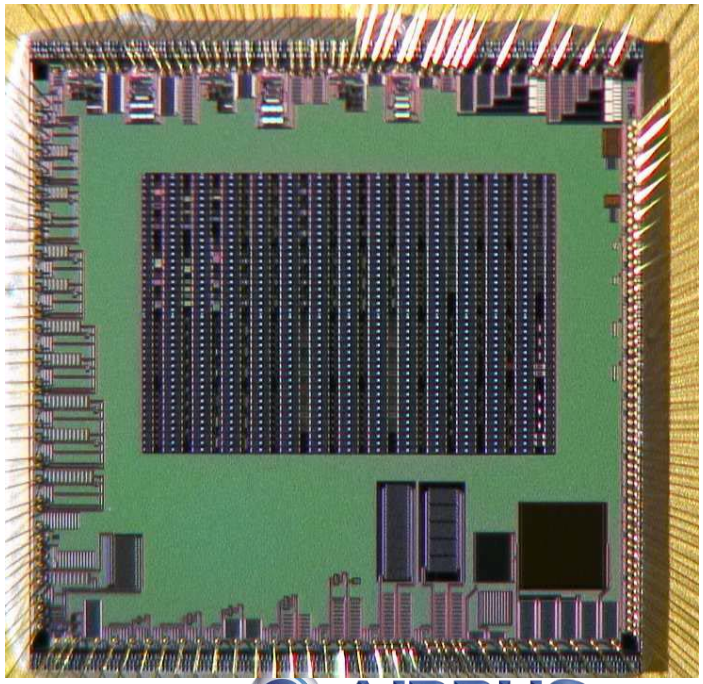
Test vehicle 2

- Test Vehicle 2 has been designed for TID and SEE tests

- It is composed of five different blocks hardened against radiations :
  - TOP_DIGITAL_2 : 3.3V isolated digital cells
  - TOP_PADS_2 : 3.3V isolated digital pads and HV analog pads
  - DRIVER_BUFFER_2 : Buffers with high output current.
  - MODULE_2 : HV and/or isolated transistors for modeling
  - MONITORING_2 : HV and/or isolated transistors, resistor, Capacitor

MODULE_2 can be accessed only by probe. It will be used for analog transistors characterization to make accurate simulation models (taking into account ELT design and TID) in the next phase.





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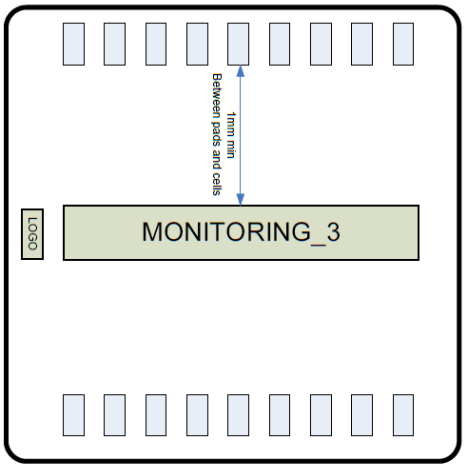
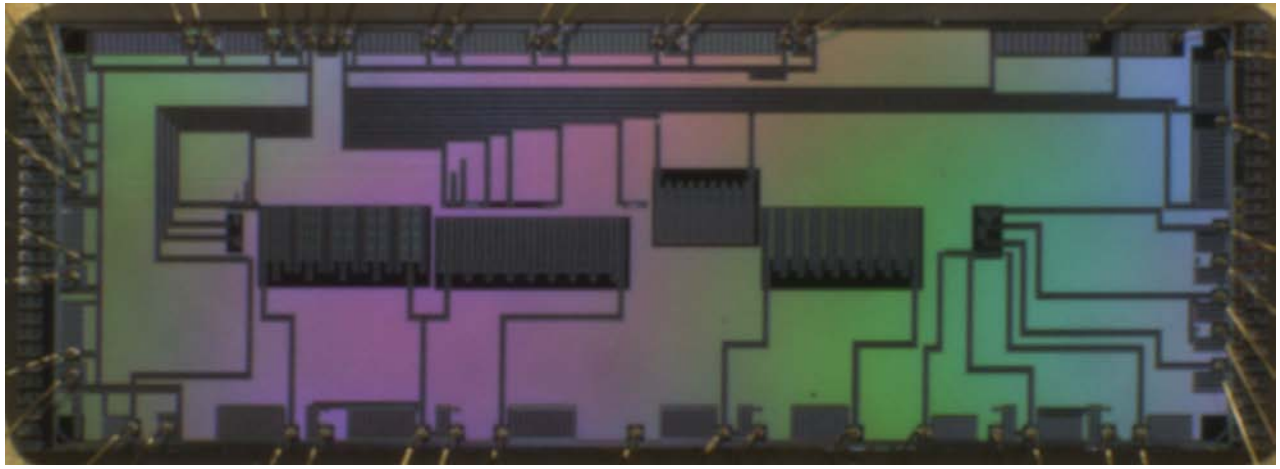
Test vehicle 3

- Test Vehicle 3 has been designed for SEB/SEGR tests
- It is composed of one block of hardened HV N & P transistors with different designs and voltages, non-isolated or isolated
- The block is in the center of the die at about 1 mm from the pads. This geometry allows focusing the ion beam on the transistors and not the pads.





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Description of the tests

- The Total Ionisation Dose tests have been carried out with a Cobalt 60 source on 6 test vehicles #1 and #2 up to 100 krads at a low dose rate of 310 rad/h. A post irradiation annealing of 24h/25°C plus 168 h/100°C has been then performed.

- The SEL tests have been performed on test vehicle #1 and #2 at RADEF (Jyväskylä, Finland) using Xenon ions with energy of 1217 MeV and a LET on die surface of 60 MeV.cm²/mg at a temperature of 125°C.

- The SEB/SEGR tests have been performed using test vehicle #3 at RADEF (Jyväskylä, Finland). Krypton ions with a LET of 37 MeV.cm²/mg and Xenon ions with a LET on die surface of 65 MeV.cm²/mg have been selected. The SOA (Safe Operating Area) has been measured using [1 and 2]. SEGR has been characterized with PIGS (Post irradiation Gate Stress) method.

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Results test #1 – Low voltage structure – digital lib

- TID tests have shown no functional or parametric problems up to 100 krads on hardened structures. The non-RT E2PROM fails in read at 14 krads for biased parts and at 30 krads for unbiased parts. The non-hardened oscillator and counter experience an important increase of their supply current.

- No SEL has been observed on the Rad-Tolerant cells.

- SELs were observed on the non-hardened counter, the non-hardened oscillator and the non-hardened E2PROM. It justifies the necessity to implement protections against SEL

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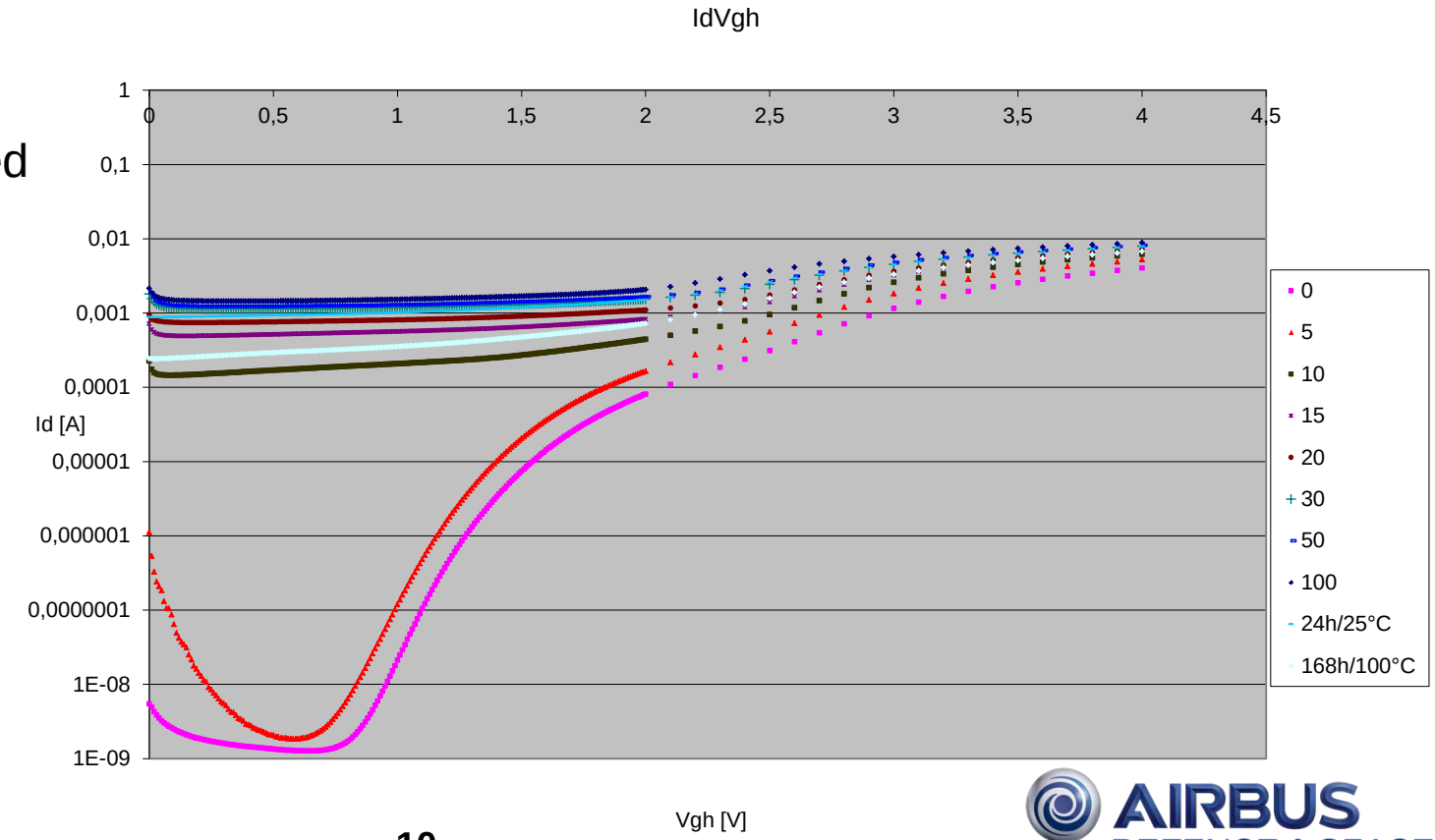
Results test #2 – HV elements TID & SEL

- All the PMOS HV transistors keep their electrical characteristics up to 100 krads.

- The NMOS HV transistors have a behaviour that depends on their design. The hardened NMOS NDHE NDHG NDHG1 have major changes in their characteristics at 10 krads, the leakage current is increased by 10^5 factor, these transistors cannot be switched off anymore. The other hardened NMOS transistors have a better behaviour and can be used up to 100 krads.

- No SEL has been detected on test vehicle #2



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Results test #3 – High voltage structures – SEB/SEGR

- SEGR was characterized at V_{GS}= 0 V for NMOS and max rating for PMOS.

- N-Channel MOSFETs are sensitive to SEB and SEGR. Even for small voltages the SOA is smaller than VDS max. As an example, the highest safe rating is 72 V for a 100 V NMOS transistor.

- P-Channel MOSFETs are sensitive to SEGR, but transistors below 45V are immune. The highest safe rating is 45V for a 45V PMOS transistor.

- Pads are sensitive neither to SEB nor to SEGR.

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Results test #3 – High voltage structures – SEB/SEGR

Device IM466A3			Kr (38 MeV)
Device type	Max Voltage (V)	tested devices	SOA (V)
N MOSFET	100	Nhvg1	**72**
	90	Ndhg	**40**
		Ndhg1	**40**
	70	Ndhe	**37**
		Ndhe1	**62**
	45	Ndha	**17**
		Ndhc	**22**
		Ndhc1	**45**
		Nhv	**22**
	18	Nmva	**18**
	14	Ngmmv	**14**
P MOSFET	90	Phvf	**40**
		Phvf_std	**40**
	70	Phvd	**45**
	45	Phvb	**45**
	40	Phv	**40**
	18	Pmva	**18**
	14	Pgmmv	**14**
Pad	92	Hvp11	**92**
	90	Hvdd12	**90**
	50	Hvdd7	**50**
		Hvp6neia	**50**

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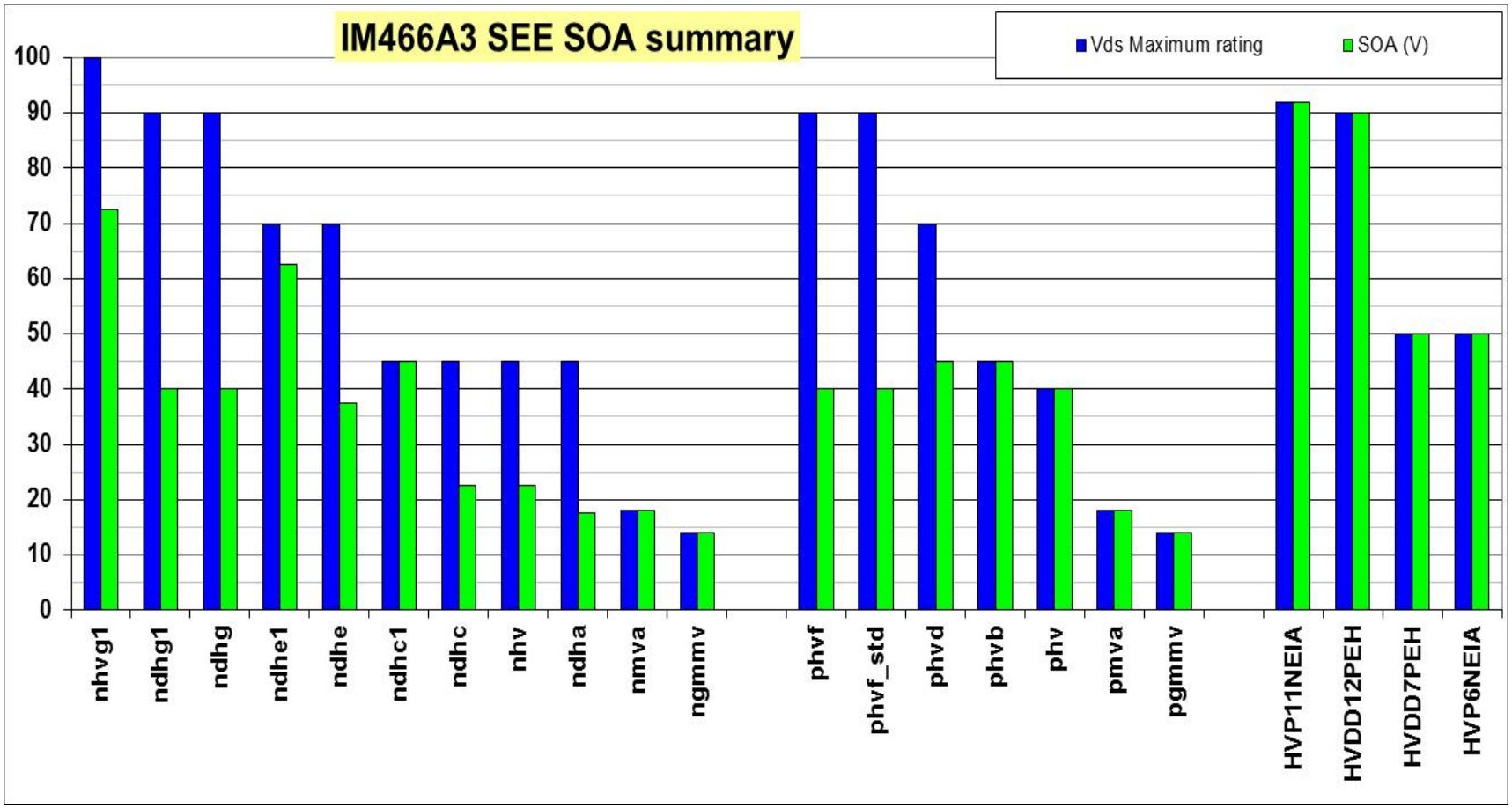
Results test #3 – High voltage structures – SEB/SEGR



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Conclusion

- This project has succeeded in designing radiation tolerant high voltage transistors and in characterizing them against TID, SEL and SEB/SEGR.

- A very good behaviour has been obtained for most of them against TID. No SEL has been detected. PMOS have a good protection against SEGR up to 45V.

- NMOS are sensitive to SEB and a higher design margin will have to be applied for them.

- In the next phase, the transistors will be electrically characterized to generate the DK and the PDK.

Thank you for your attention