Radiation-Tolerant High-Voltage ASIC Library Evaluation for Space Applications

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Abstract

This research and development project is performed for the Neosat project with Airbus DS as prime contractor and is under CNES contract, with ID-MOS partner for ASIC design

Increasing needs for low costs, low space occupancy and reduced weight in the space industry have made ASIC integration of recurrent functions mandatory. Today, ASICs are mainly used for digital applications, but the use of mixed ASIC would increase the integration of the platform equipment that are designed and manufactured by Astrium Elancourt. Such designs require an ASIC process having high voltage capabilities up to 100V. Airbus DS has selected with partners and CNES the XH035 HV process. A LV rad-tolerant digital library has already been designed under a previous contract. The aim of this activity is to develop a set of rad-tolerant High Voltage transistors and to test them against TID, SEL and SEB/SEGR.

I. INTRODUCTION

Airbus DS selected the XFAB XH035 mixed-signal technology for its modularity and high-voltage extensions. This technology targets automotive, telecommunication and power management markets; therefore it has been widely used and tested for various applications and is a mature technology. Furthermore, digital and mixed-signal ASICs for space applications have already been designed in this technology and their radiation tolerance has been tested but, to our knowledge, the high-voltage functionalities have never been used in this context.

The XH035 HV process mainly differs from the standard process by its deep epitaxial layer and a thick gate oxide..

The rad-tolerant library has already been designed for the XH035 standard LV process by IDMOS under a previous CNES contract. This library has been tested against TID and SEL and could be re-used with the XH035-HV process since the design rules are the same for the low voltage structure. But the change of the epitaxial layer leads to re-run the TID and SEL tests using the same test vehicle with the HV process to check whether the electrical performance, the SEL insensitivity and the TID characteristics are still acceptable.

The tasks performed in this contract are the following:

- Design a rad-tolerant library of HV N and P transistors, with protection pads, and isolated logic cells.
- Design a test vehicle (#2) to test the HV structures against TID and SEL
- Design a test vehicle (#3) to test the HV structures against SEB and SEGR
- Implement the test vehicle (#1) already designed for the low voltage digital library on the HV process
- Manufacture the 3 test vehicles
- Perform assembly of the 3 test vehicles
- Perform the TID tests on #1 and #2 vehicles
- Perform the SEL/SEE tests on #1 and #2 vehicles
- Perform the SEB/SEGR test on #3 vehicle
- Analyze and synthetize the results
- Prepare next phase

II. MATERIAL AND METHODS

A. Design of the HV transistors and cells

To fulfil Airbus DS needs, a HV radiation-tolerant library has been designed. Its target is to be functional and characterized up to 100 krads.

22 N and P transistors have been selected in XFAB library amongst the various types :

- 14 NMOS (nmos, nha, nmva, nhv, ngmmv, ndha, nmosia, ndhc, ndhe, ndhg, nhvg1, ndhc1, ndhe1,ndhg1)
- 8 PMOS (pmos, pmva, phv, pgmmv, pmosia, phvb, phvd, phvf)

These transistors have been hardened using an enclosed layout (ELT) and guard rings. Structures have also been used to break leakage paths. Although the medium gate oxide should be less sensitive than the thick gate oxide against TID effect, the thick gate oxide has been chosen due to its better expected immunity to SEGR (Single Event Gate Rupture).

Other structures have been designed and hardened:

- Power output buffers (18 V, 45 V, 70V, 90 V), with 100 mA current capability, and associated driver
- Logic isolated basic cells (Not, Nand gates, etc…),
- Logic isolated structures (Ring Oscillator),
- PADs (HV and LV PADs),

B. Description of the test vehicles

1) Test Vehicle #1 – High Voltage Structure

Test Vehicle #1 has been previously designed to test the low voltage logic elements of the XH035 standard process. It is

unchanged except that the wafer has a deep epitaxial layer. It contains mainly digital elements (Input & Output pads and cells). In order to have a reference, a counter and an oscillator are implemented both in tolerant and non-tolerant version. An unhardened E2PROM is also implemented (only the charge pump is hardened).

2) Test Vehicle #2 – High Voltage Structure

Test vehicle #2 is mainly composed of high voltage and/or isolated transistors hardened against radiations.
The package is a PGA 256 and die size is 8.7mm x 8.5mm.
Some transistors can be connected via bonding and pins for TID and SEL tests. But others will only be accessible by internal test points for measurements using probes. These transistors will be used at a later development stage to create the transistor models for analog simulation of TID-induced drifts.

3) Test Vehicle #3 – High Voltage dedicated to SEB SEGR

The test vehicle n°3 is only composed of high voltage and/or isolated transistors hardened against radiations. It is dedicated to the SEB/SEGR test. It contains mainly a block of transistors in the center of the die at about 1 mm from the pads. This geometry allows focusing the particles on the transistors and not the pads.

C. Description of the tests

The Total dose tests have been carried out with a Cobalt 60 source on 6 test vehicles #1 and #2 up to 100 krads at a low dose rate of 310 rad/h. An annealing of 24h/25°C plus 168 h/100°C has been performed.

The SEL tests have been performed on test vehicle #1 and #2 at RADEF (Jyväskylä, Finland) using Xenon ions with energy of 1217 MeV and a LET on die surface of 60 MeV.cm²/mg at a temperature of 125°C.

The SEB/SEGR tests have been performed using test vehicle #3 at RADEF (Jyväskylä, Finland). Krypton ions with a LET of 37 MeV.cm²/mg and Xenon ions with a LET on die surface of 65 MeV.cm²/mg have been selected. The SOA (Safe Operating Area) has been measured using [1 and 2]. SEGR has been characterized with PIGS (Post irradiation Gate Stress) method.

III. Results

A. Test Vehicle #1 – Low voltage Logic

TID tests have shown no functional or parametric problems up to 100 krads on hardened structures. The non-RT E2PROM fails in read at 14 krads for biased parts and 30 krads for unbiased parts. The non-hardened oscillator and counter experience an important increase of their supply current.

No SEL has been detected on the Rad-Tolerant cells.
SELs were observed on the non-hardened counter, the non-hardened oscillator and the non-hardened E2PROM. It justifies the necessity to implement protections against SEL.

A. Test Vehicle #2 – High Voltage Structure

The PMOS HV transistors keep their electrical characteristics up to 100 krads.

The NMOS HV transistors have a behaviour that depends on their design. The hardened NMOS NDHE NDHG NDHG1 have a deep change in their characteristics at 10 krads, the leakage current is increased by 10^5, these transistors cannot be switched off any more. The other hardened NMOS transistors have a better behaviour and can be used up to 100 krads.

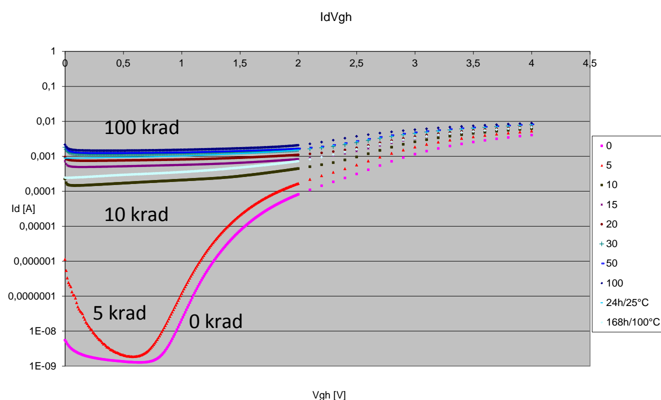

Figure 1 : NDHE HV NMOS losing its switching-off capability at 10 krads

The HV output buffers exhibit an increase of their rise time of about 20% at 15 krads because their design include sensitive N transistors.

No SEL has been detected on test vehicle #2. The HV transistors are correctly protected against latch-up.

B. Test Vehicle 3 – High Voltage for SEB SEGR

Since this is an ASIC technology, overblocking is not possible and SEGR was characterized at V_{GS}=0V for NMOS and max rating for PMOS.
N-Channel MOSFETs are sensitive to SEB and SEGR. Even for small voltages the SOA is smaller than VDS max. The highest safe rating is 72V for a 100V NMOS transistor.
P-Channel MOSFETs are sensitive to SEGR, but transistors below 45V are immune. The highest safe rating is 45V for a 45V PMOS transistor.
Pads are sensitive neither to SEB nor to SEGR.
The results are provided in Figure 2. In order to be in agreement with Radiation Hardness Assurance requirements, only the SOA obtained with heavy ions having LET ≈ 38 MeV.cm²/mg is displayed here.

Device IM466A3			Kr (38 MeV)
Device type	**Max Voltage (V)**	**tested devices**	**SOA (V)**
N MOSFET	100	Nhvg1	**72**
	90	Ndhg	**40**
		Ndhg1	**40**
	70	Ndhe	**37**
		Ndhe1	**62**
	45	Ndha	**17**
		Ndhc	**22**
		Ndhc1	**45**
		Nhv	**22**
	18	Nmva	**18**
	14	Ngmmv	**14**
P MOSFET	90	Phvf	**40**
		Phvf_std	**40**
	70	Phvd	**45**
	45	Phvb	**45**
	40	Phv	**40**
	18	Pmva	**18**
	14	Pgmmv	**14**
Pad	92	Hvp11	**92**
	90	Hvdd12	**90**
	50	Hvdd7	**50**
		Hvp6neia	**50**

Figure 2 : SOA of HV transistors and pads

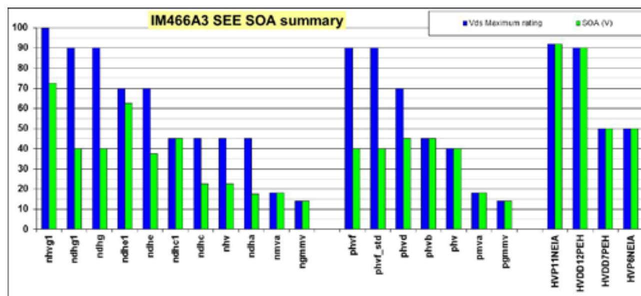

Figure 3 : Summary of SOA of HV transistors and pads

IV. Conclusion

This project has succeeded in designing radiation tolerant high voltage transistors and in characterizing them against TID, SEL and SEB/SEGR. A very good behaviour has been obtained for most of them against TID. No SEL has been detected. PMOS have a good protection against SEGR up to 45V. NMOS are sensitive to SEB and a higher design margin will have to be applied for them.

In the next phase, the transistors will be electrically characterized to generate the DK and the PDK.

V. References

[1] Single event effects test method and guidelines ESA/SCC basic specification N°25100 Iss 1, oct 95

[2] Single Event Burnout and Single Event Gate Rupture, MIL-STD-750E, Method 1080