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Radiation-hardened high-voltage ASIC technology qualification for space application.

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Increasing needs for low costs, low space occupancy and reduced weight in the space industry have made ASIC integration of recurrent functions mandatory. Today, ASICs are used only for digital applications, but for the next satellite platform generation, ASIC integration will also be needed for analogue, mixed-signal and high-voltage applications.

Airbus DS selected the XFAB XH035 mixed-signal technology for its modularity and high-voltage extensions. This technology targets automotive, telecommunication and power management markets; therefore it has been widely used and tested for various applications and considered to be a mature technology. Furthermore, digital and mixed-signal ASICs for space applications have already been designed in this technology and their radiation tolerance has been tested but, to our knowledge, the high-voltage functionalities have never been used in this context. Lastly, the cost of a foundry run is compatible with our cost reduction needs, thanks to the selected technology node.

The current activity builds on the previous ID-MOS/CNES development dealing with the hardening of the standard Low Voltage XH035 process, by including the high voltage capability. The XH035 High Voltage technology requires a deep epitaxial layer that has an impact on the cell design and thus influences the radiation tolerance of the digital library. All the HV transistors have to be hardened and tested against radiation.

To fulfill Airbus DS needs, especially in terms of radiation tolerance, a High Voltage radiation-hardened library has been developed with the XH035 HV technology and is currently under evaluation. For a full characterization and qualification process, a test vehicle has been designed; this test vehicle contains: digital cells, analogue functions and high-voltage transistors (NMOS and PMOS ranging from 15V to 90V). Radiation-hardening consists of implementing ELTs (Enclosed Layout Transistors) surrounded by Guard Rings and with additional spacing between PMOS and NMOS banks.

Up to now, SEL (Single Event Latchup), SEB (Single Event Breakdown) and SEGR (Single Event Gate Rupture) tests have been performed and TID (Total Ionizing Dose) and Life tests are underway. After this radiation qualification phase, a precise electrical characterization of the designed cells will be performed to improve the device models.

This research and development project is performed for the Neosat project with Airbus DS as prime contractor and is under CNES contract and with ID-MOS for ASIC design.

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