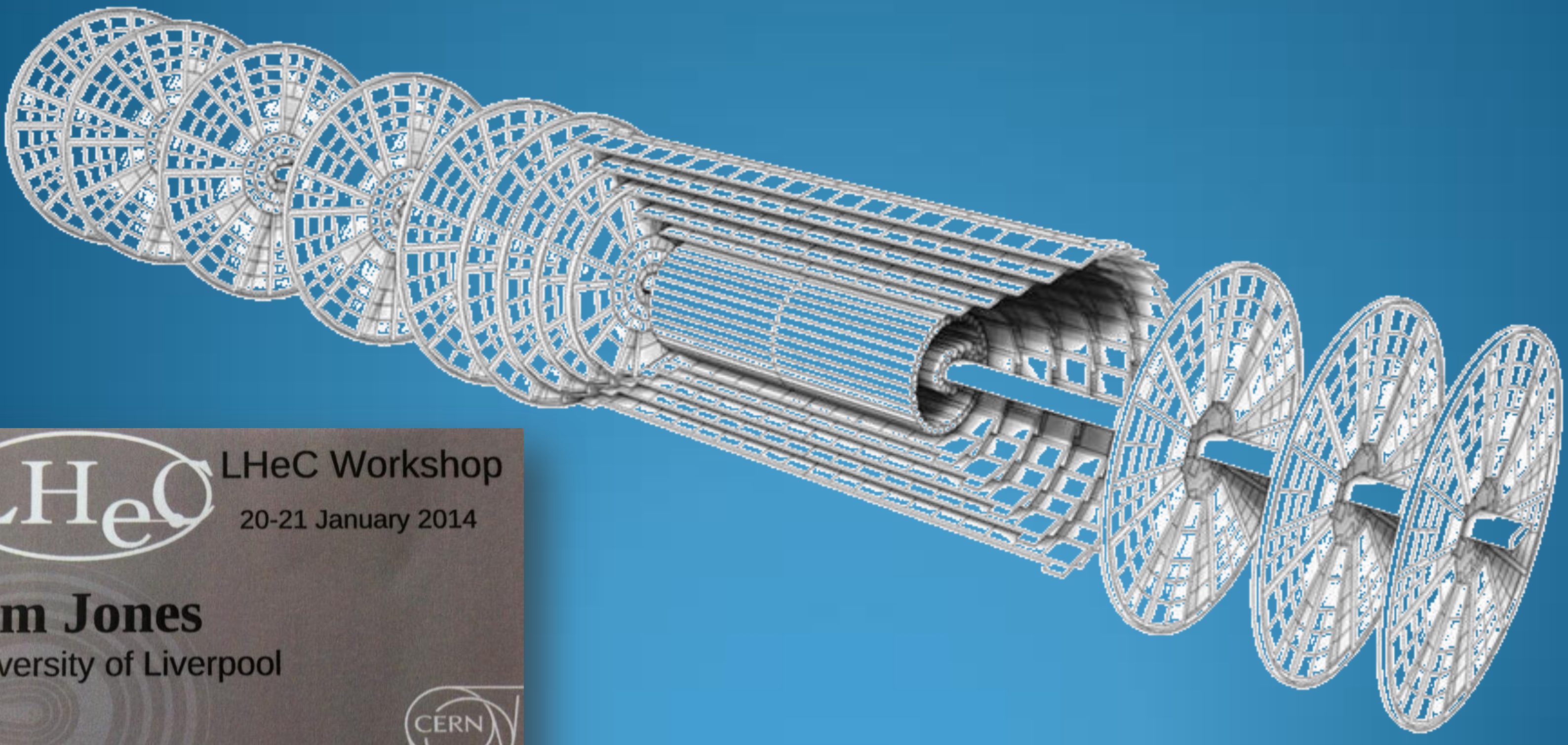
First Thoughts on the Silicon Tracker



LHeC Workshop
20-21 January 2014
Tim Jones
University of Liverpool
CERN

Overview

- Tracking System Requirements
  - CDR ‘snap-shot’
- ATLAS Phase-2 Tracker Development
  - Local Supports
  - Pixels
  - Central Strip Tracker
  - Forward Strip Tracker
  - (HV)CMOS
- Conceptual LHeC Tracker Geometrical Design
  - 3D CAD model
  - Areas, Module Counts, Channel Counts
- Global Design Issues
- Summary & Conclusions

CDR Detector Performance Requirements

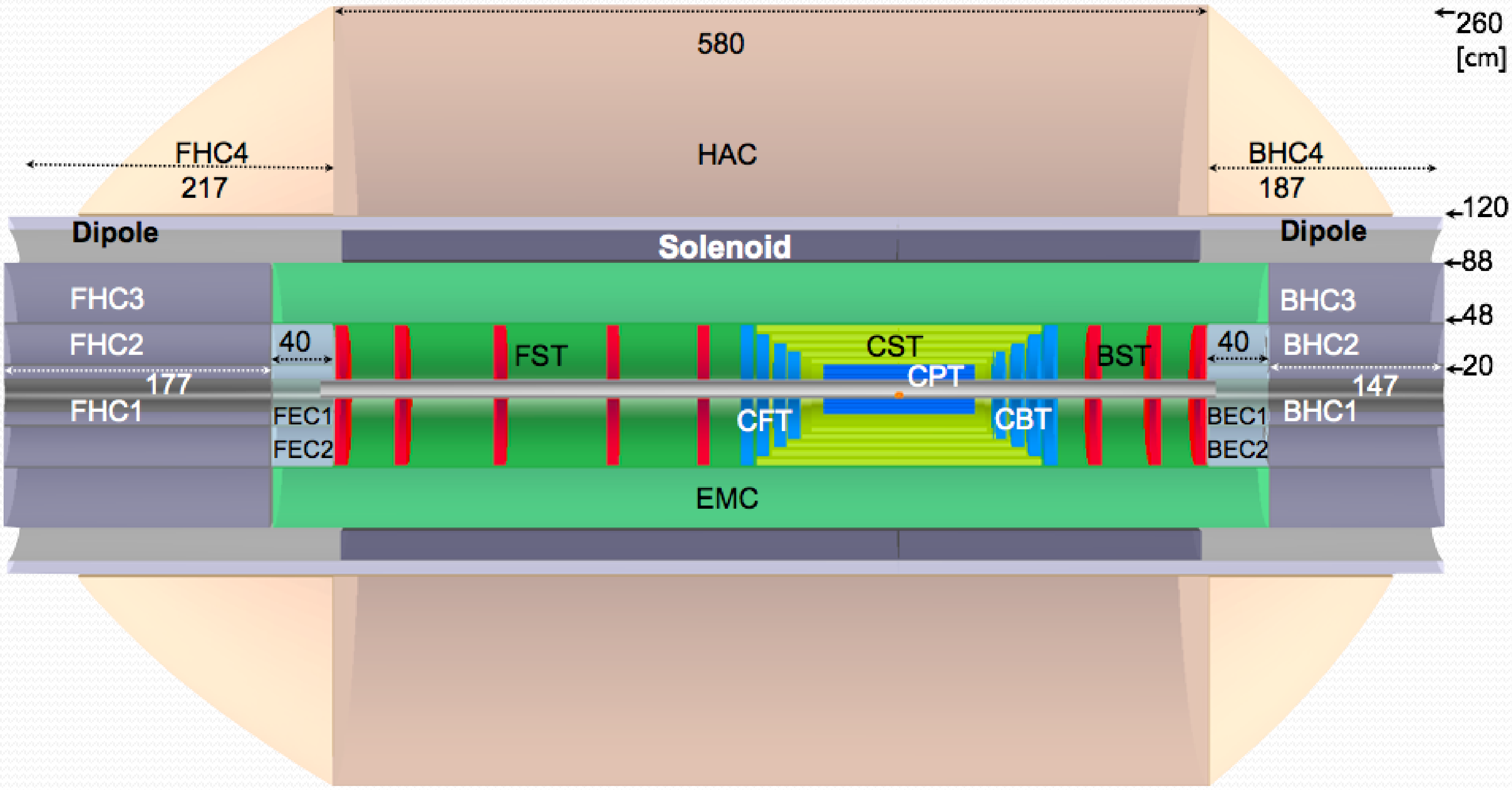
- High resolution tracking system
  - excellent primary vertex resolution
  - resolution of secondary vertices down to small angles in forward direction for high x heavy flavor physics and searches
  - precise p_t measurement matching to calorimeter signals (high granularity), calibrated and aligned to 1 mrad accuracy

- The Calorimeters
  - electron energy to about 10%/ √ E calibrated using the kinematic peak and double angle method, to 0.1% level

    Tagging of γ's and backward scattered electrons - precise measurement of luminosity and photo-production physics
  - hadronic energy to about 40%/√ E calibrated with p_{t_e} /p_{t_h} to 1% accuracy
  - Tagging of forward scattered proton, neutron and deuteron - diffractive and deuteron physics

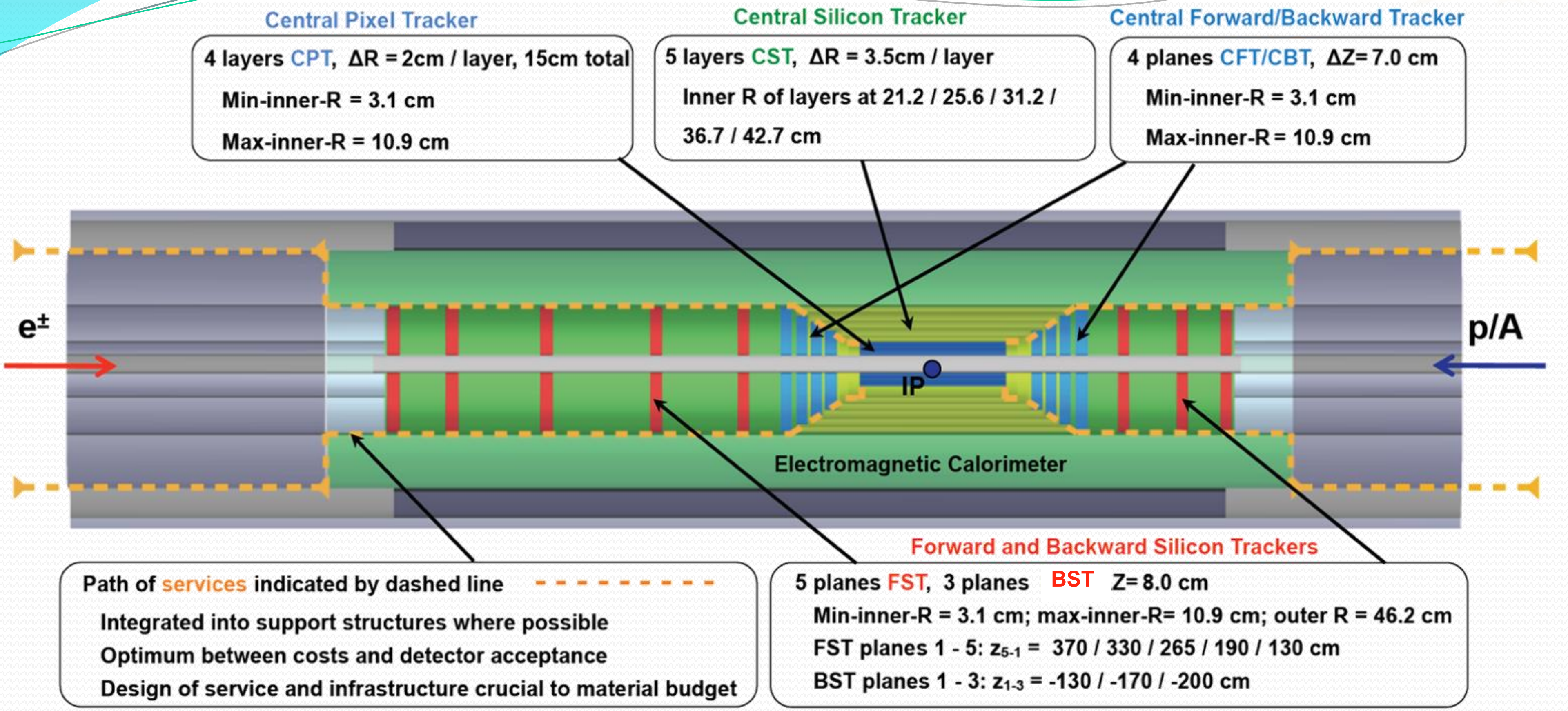
- Muon System

Baseline Detector (CDR)



- High acceptance Silicon Tracking System
- Liquid Argon EM Calorimeter inside solenoid
- Iron-Scintillator Hadronic Calorimeter
- Forward Backward Calorimeters: Si/W Si/Cu

Compact Silicon Tracking



- Very compact design, contained within the electromagnetic calorimeter:
  - small radius due to constraints from the magnet
- More coverage in the proton direction:
  - dense forward jet production (down to 1° in θ)
- Services and Infrastructure need detailed engineering design

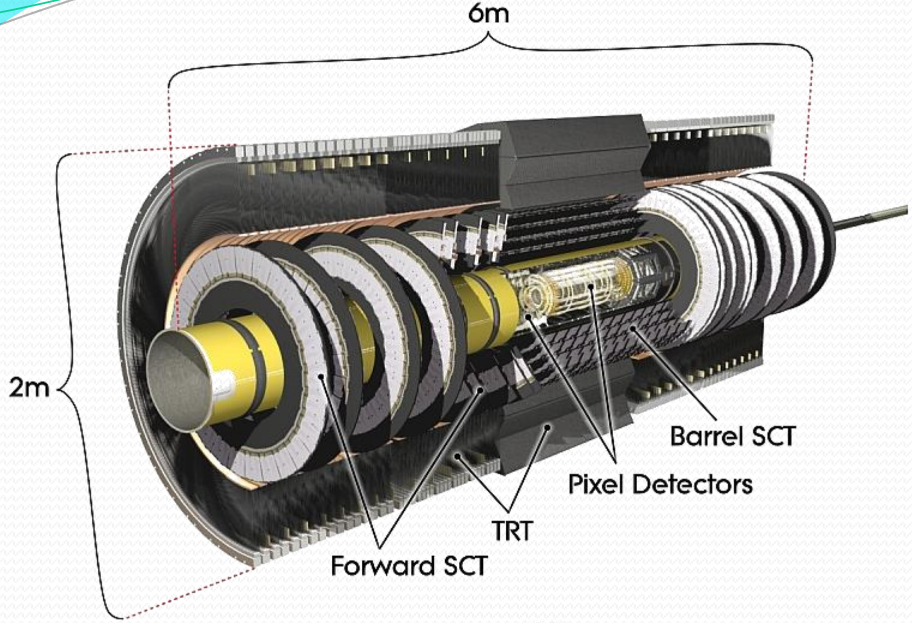
CDR Tracking System Geometry

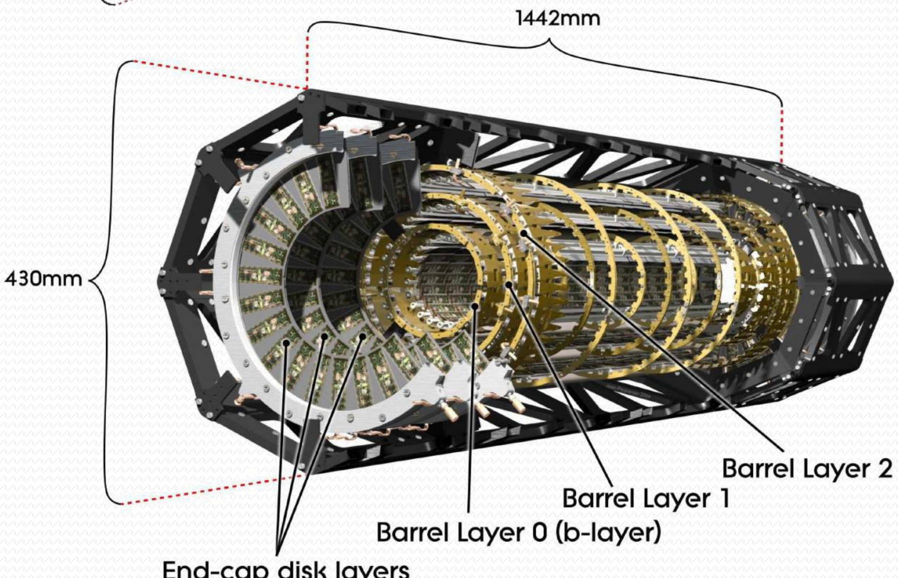
Central Barrel	CPT1	CPT2	CPT3	CPT4	CST1	CST2	CST3	CST4	CST5
Min. Radius R $[cm]$	3.1	5.6	8.1	10.6	21.2	25.6	31.2	36.7	42.7
Min. Polar Angle $\theta[^0]$	3.6	6.4	9.2	12.0	20.0	21.8	22.8	22.4	24.4
Max. $\|\eta\|$	3.5	2.9	2.5	2.2	1.6	1.4	1.2	1.0	0.8
ΔR $[cm]$	2	2	2	2	3.5	3.5	3.5	3.5	3.5
$\pm z$-length $[cm]$	50	50	50	50	58	64	74	84	94
Project Area $[m^2]$	1.4				8.1				
Central Endcaps	**CFT4**	**CFT3**	**CFT2**	**CFT1**		**CBT1**	**CBT2**	**CBT3**	**CBT4**
Min. Radius R $[cm]$	3.1	3.1	3.1	3.1		3.1	3.1	3.1	3.1
Min. Polar Angle $\theta[^0]$	1.8	2.0	2.2	2.6		177.4	177.7	178	178.2
at z [cm]	101	90	80	70		-70	-80	-90	-101
Max./Min. η	4.2	4.0	3.9	3.8		-3.8	-3.9	-4.0	-4.2
Δz $[cm]$	7	7	7	7		7	7	7	7
Project Area $[m^2]$	1.8					1.8			
Fwd/Bwd Planes	**FST5**	**FST4**	**FST3**	**FST2**	**FST1**		**BST1**	**BST2**	**BST3**
Min. Radius R $[cm]$	3.1	3.1	3.1	3.1	3.1		3.1	3.1	3.1
Min. Polar Angle $\theta[^0]$	0.48	0.54	0.68	0.95	1.4		178.6	178.9	179.1
at z [cm]	370	330	265	190	130		-130	-170	-200
Max./Min. η	5.5	5.4	5.2	4.8	4.5		-4.5	-4.7	-4.8
Outer Radius R $[cm]$	46.2	46.2	46.2	46.2	46.2		46.2	46.2	46.2
Δz $[cm]$	8	8	8	8	8		8	8	8
Project Area $[m^2]$	3.3						2.0		

ATLAS Phase-2 Tracker Upgrade

- Geometry & basic parameters
  - Current ATLAS & Phase-2 Inner Detector upgrade
- Concept of "local supports"
- Overview of technical development for:-
  - Barrel Pixel staves
  - Forward Pixel Disks
  - Barrel Strip Staves
  - Forward Strip Disks
- Brief comment on (HV)CMOS

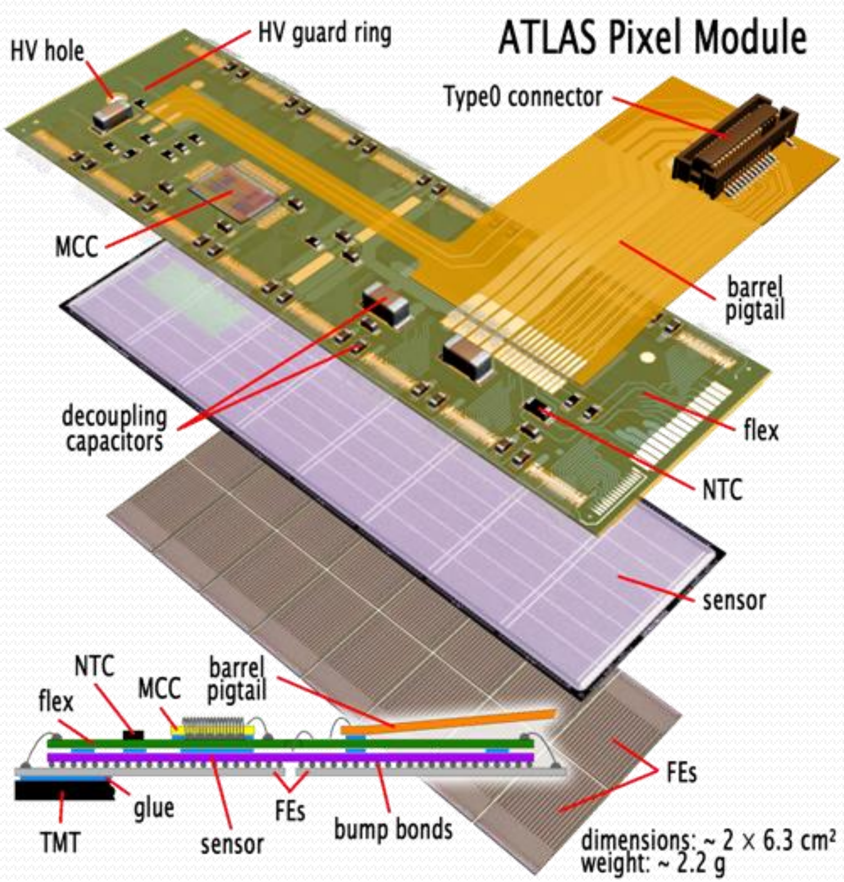
Current ATLAS Tracking

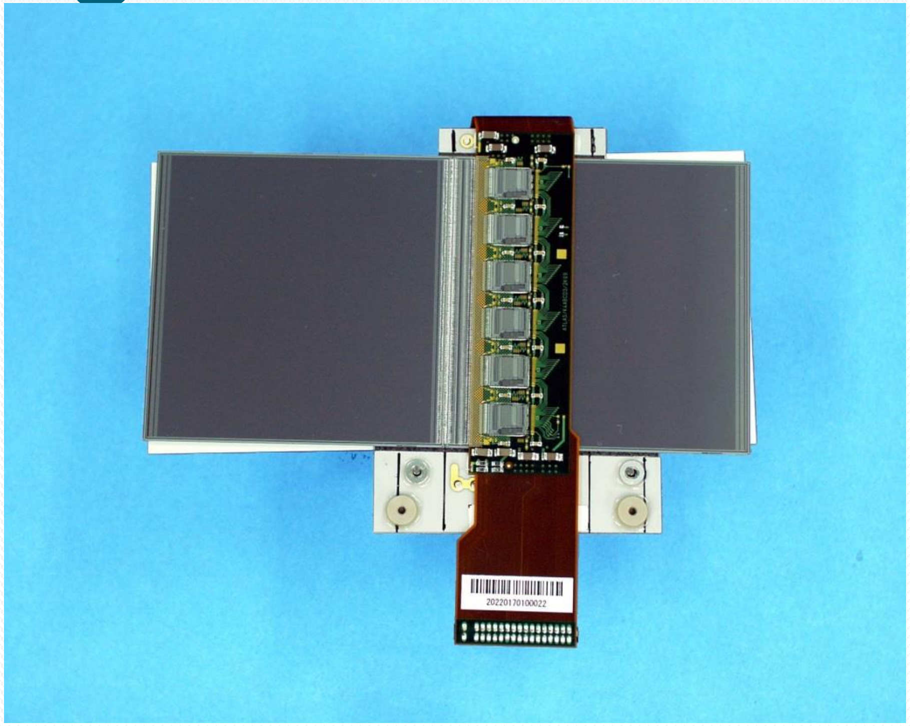




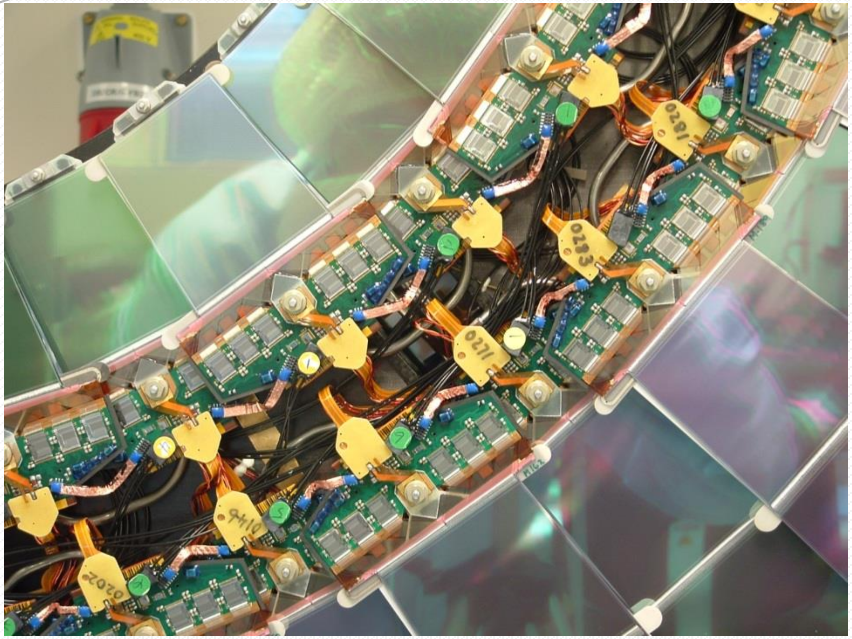
- SCT
  - **61m²** of silicon with 6.2 million readout channels
  - **4088** silicon modules arranged to form 4 Barrels and 18 Disks (9 each end)
  - Barrels : 2112 modules (1 type) giving coverage $|\eta| < 1.1$ to 1.4
  - Endcaps : 1976 modules (4 types) with coverage 1.1 to $1.4 < |\eta| < 2.5$
  - 30cm < R < 52cm
  - Space point resolution r ~16μm / Z~580μm
- Pixels
  - **1744** Pixel Modules on three barrel layers and 2 x 3 discs covering **1.7m²**
  - 80M readout channels

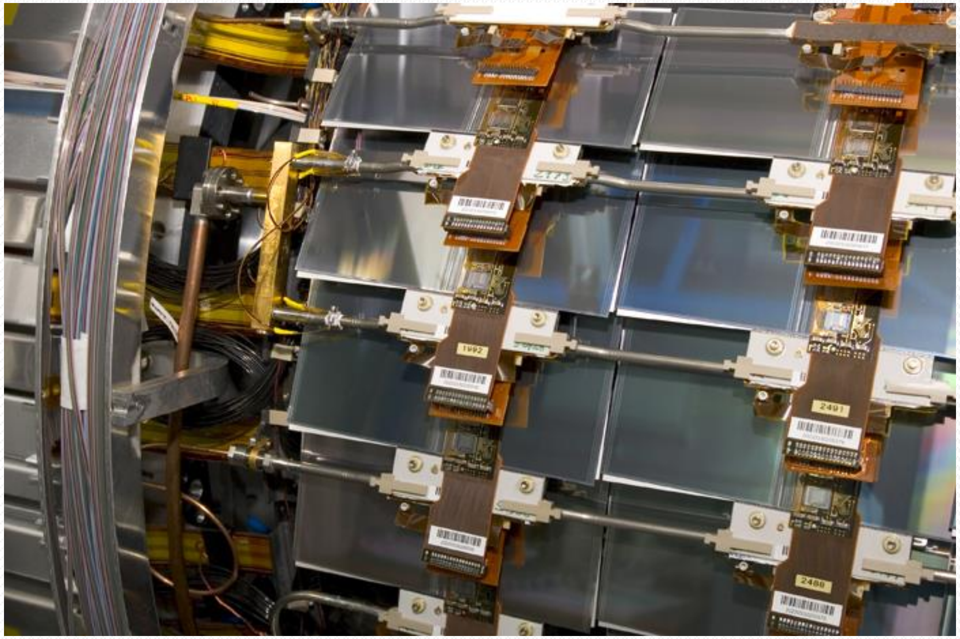
Module Technologies

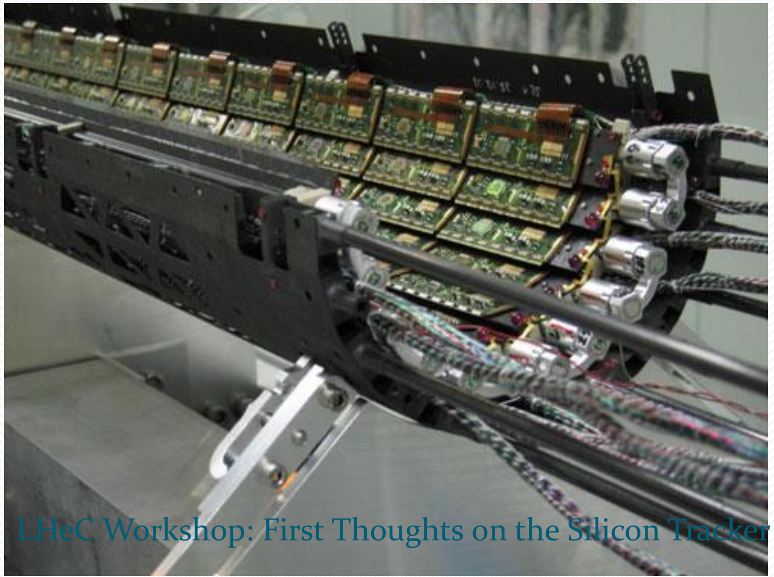




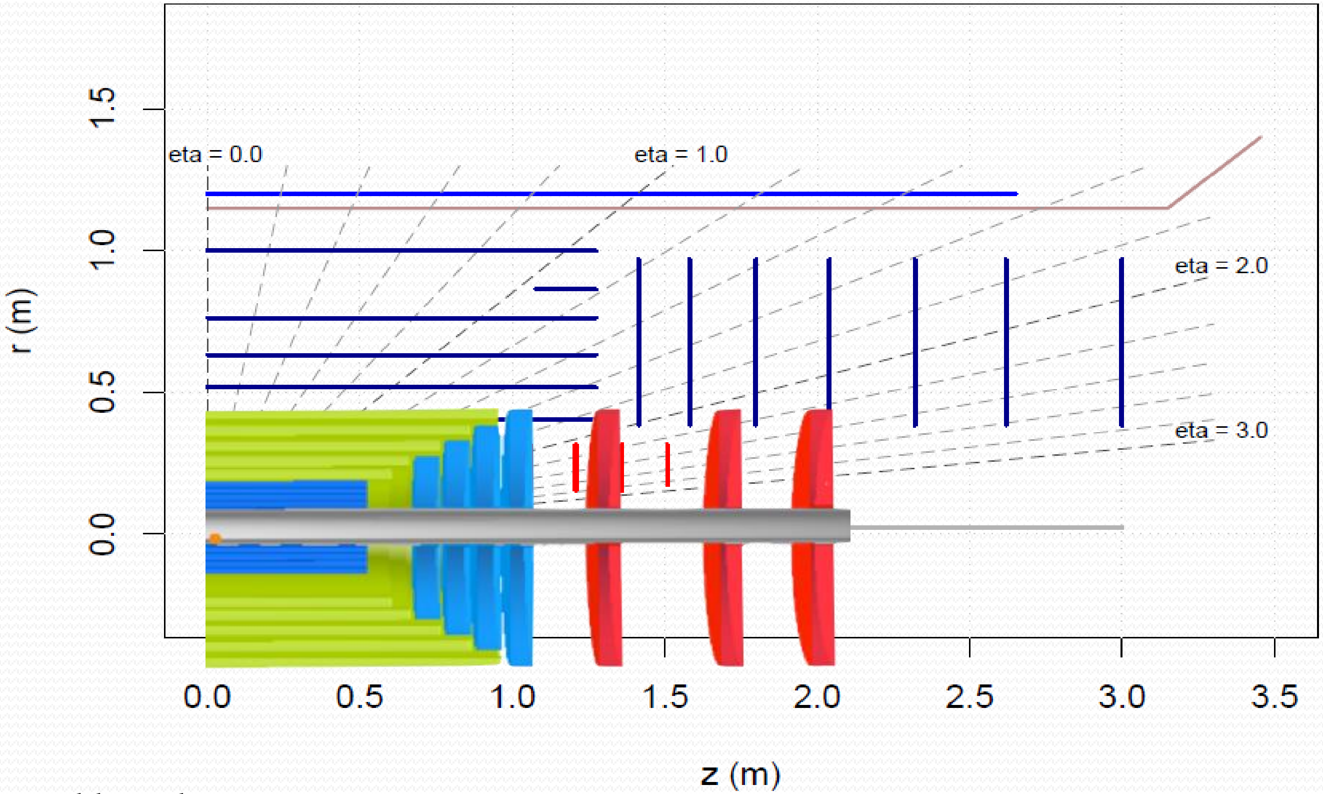
Mechanics & Services





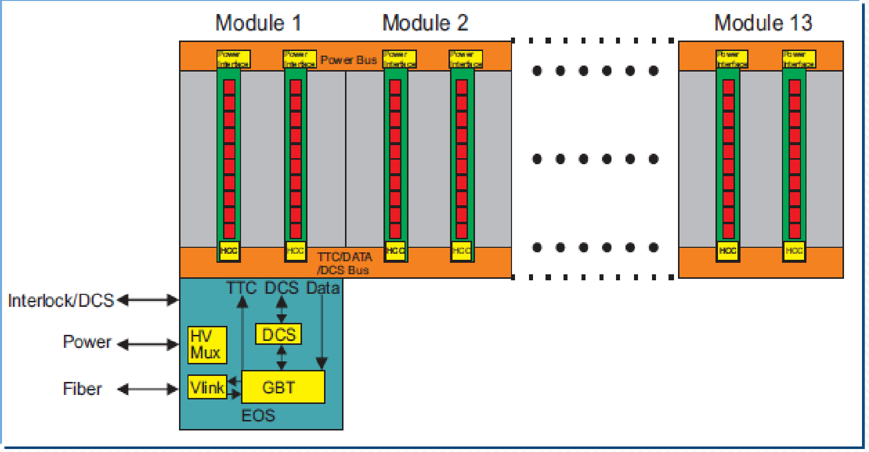


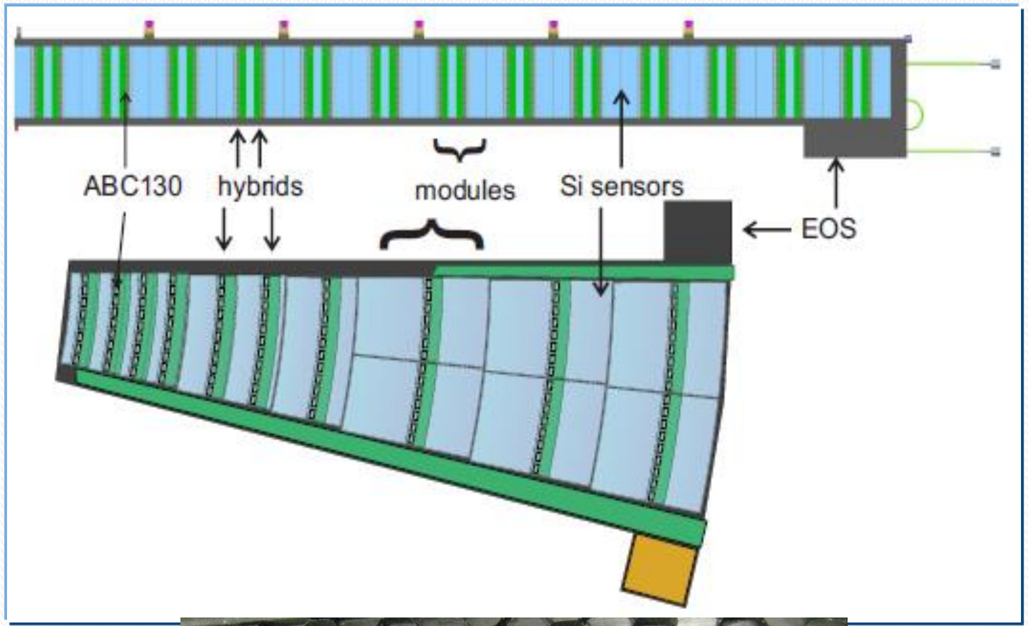
Phase-2 Developments

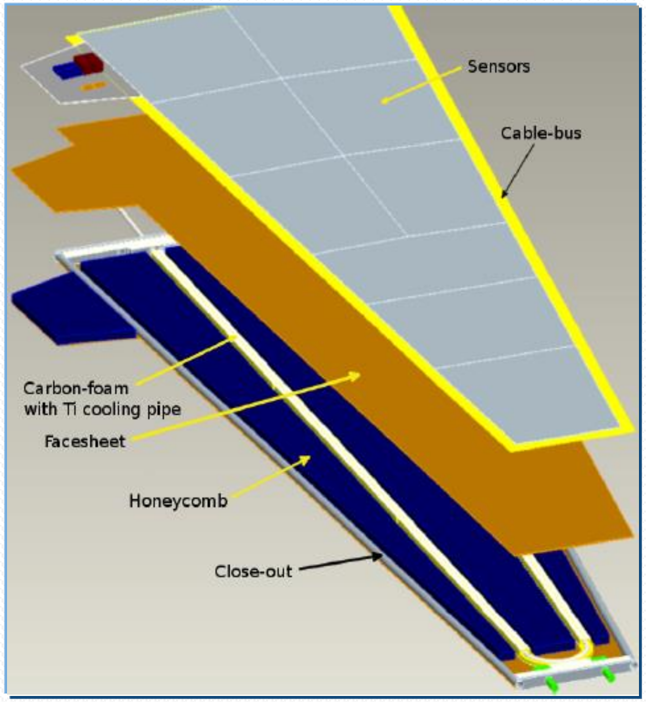


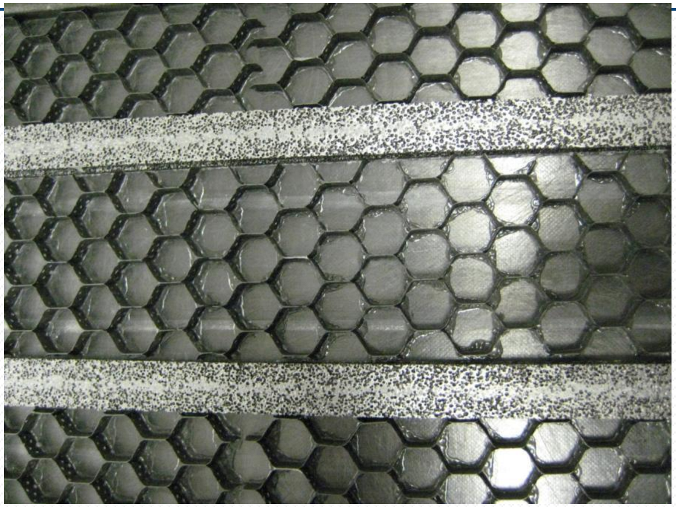
- All silicon Inner Detector
  - 4(pixel) + 5(strip-pairs) = 14 hits
  - Strips: 200m² (5 ½ barrel layers + 2x7 disks) (**x3.3**)
  - Pixels: 8 m² (**x4.7**)

Local Supports

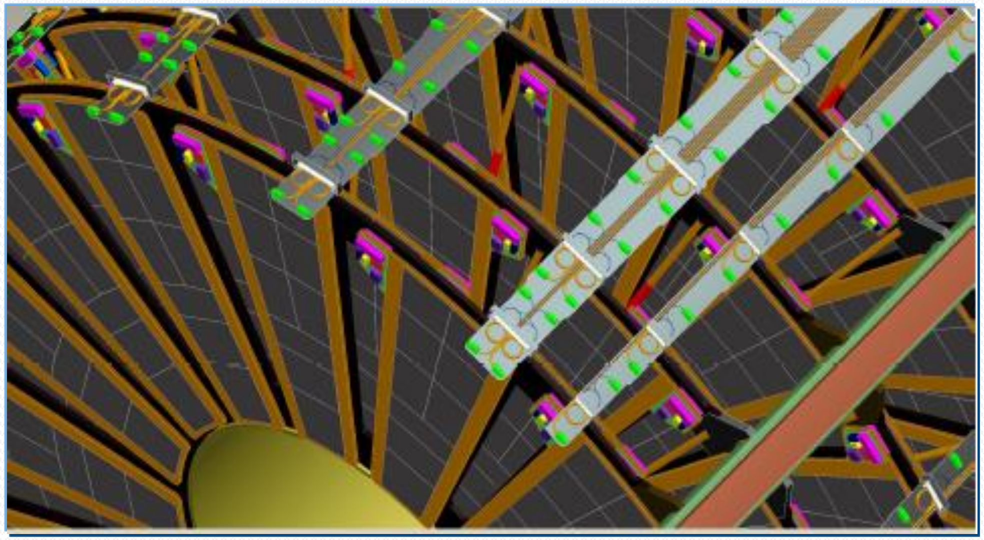


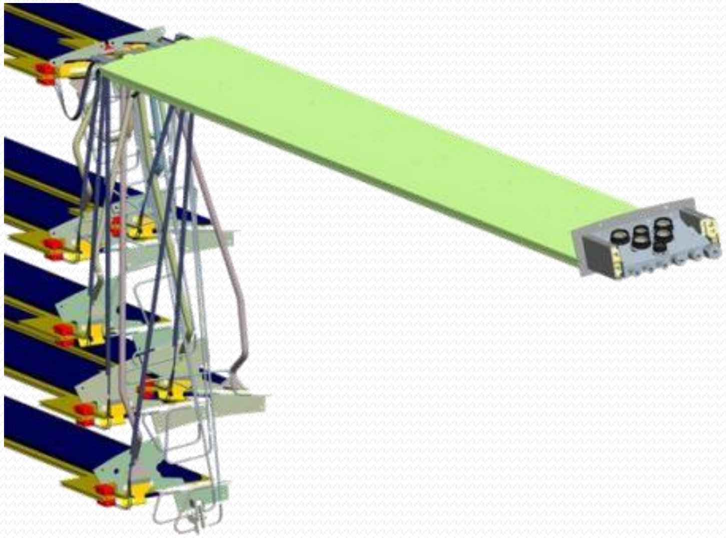


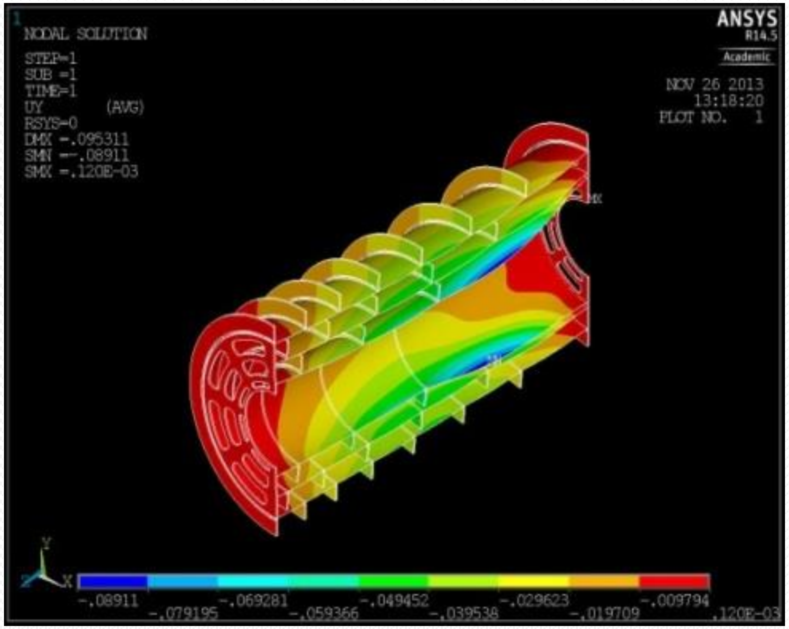




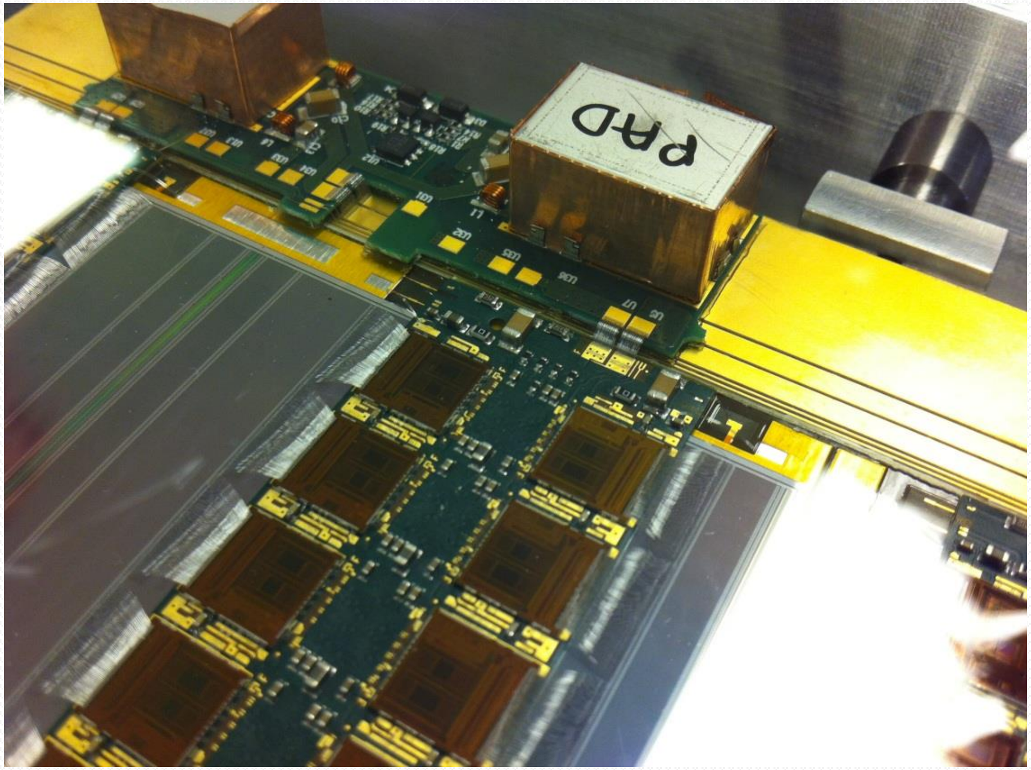
Global Supports & Services





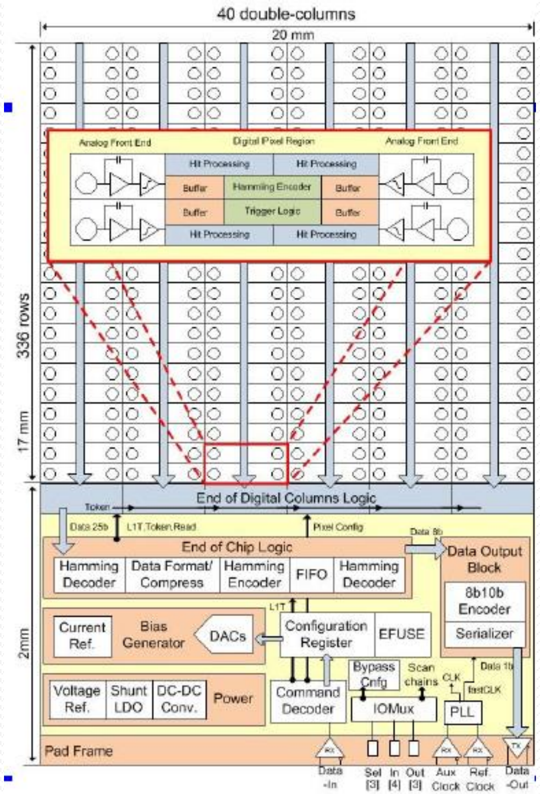


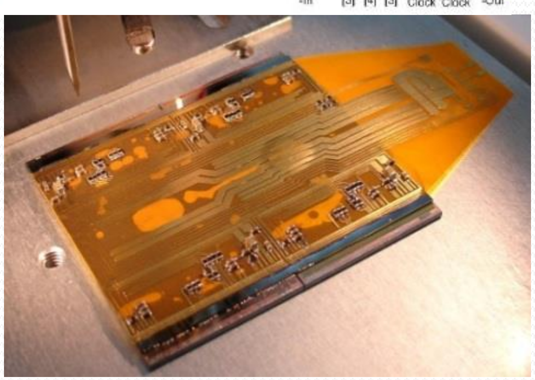
Stave Prototyping



- 12-module stave (with DCDC powering) completed December 2013

Pixels

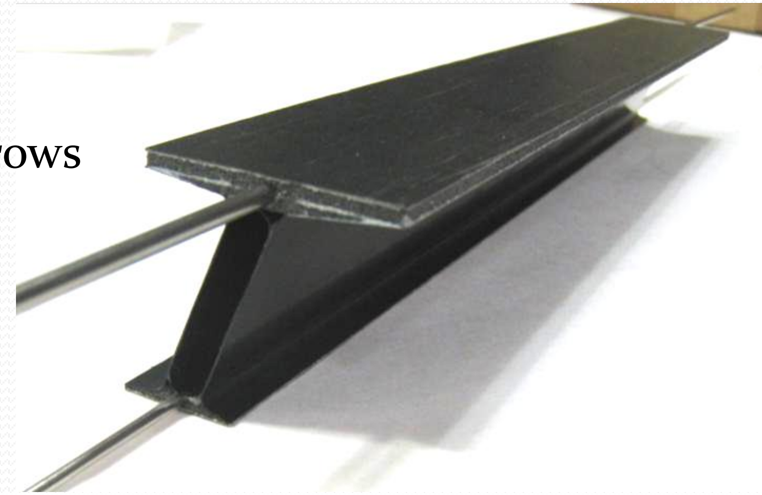


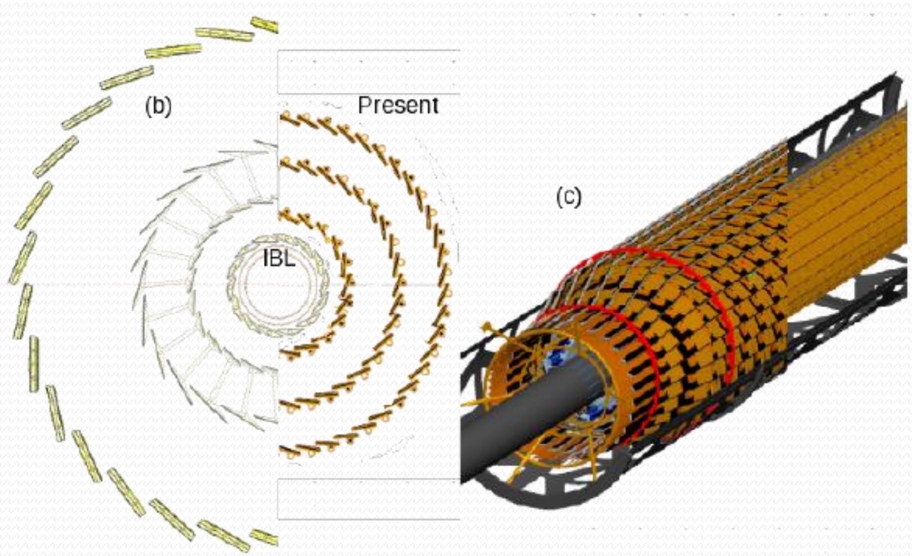


FE-I4 pixel ASIC
- 20 x 17mm
- 80 columns x 336 rows

Double-module
- 2 x FE-I4

Quad Module
- 4 x FE-I4





(HV)CMOS

Daniel Muenstermann
AUW- Nov '13

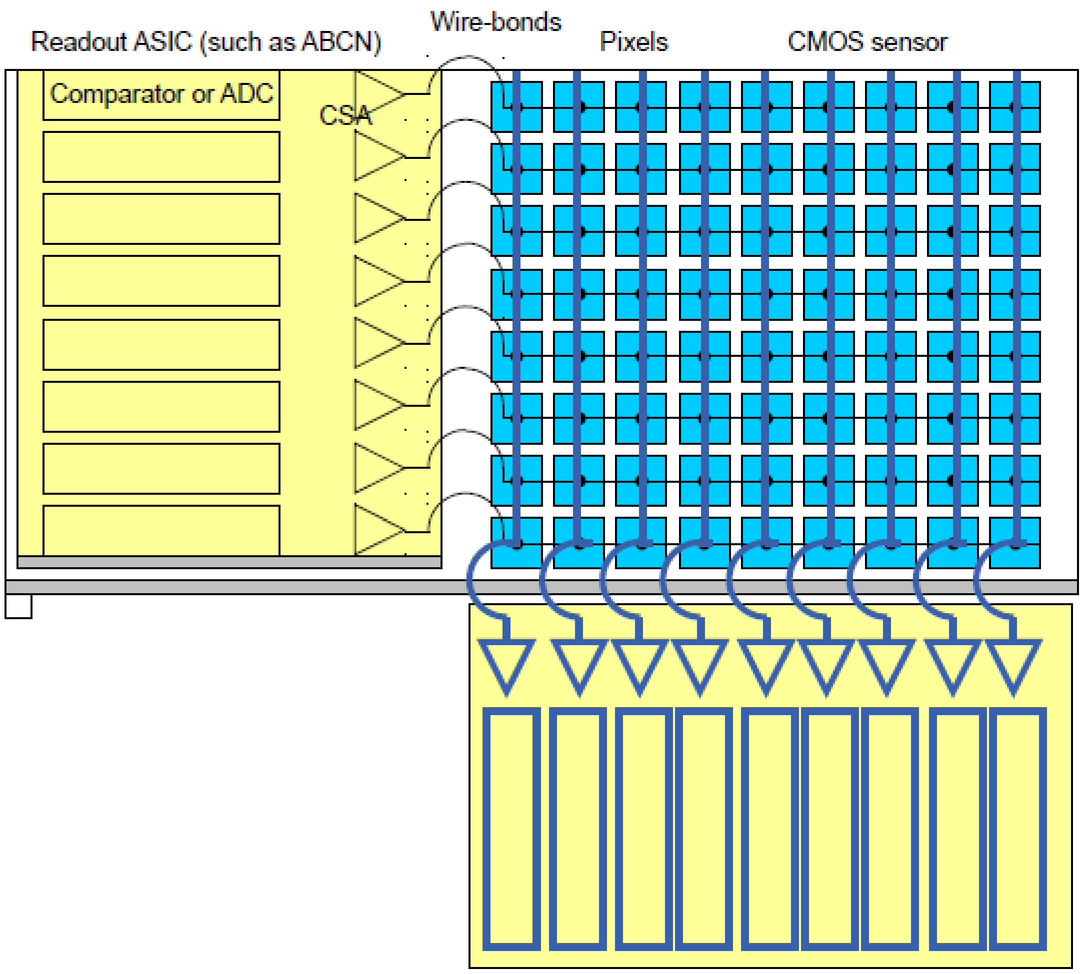
- 'Hot Topic' within ATLAS (cost reduction)
  - industrialised processes
  - large wafer sizes
  - Cheap(er) interconnection technology

- Idea: explore industry standard CMOS processes as sensors
  - commercially available by variety of foundries
  - large volumes, more than one vendor possible
  - but: application of **drift field** required for sufficient rad-hardness
    - ➔ requires careful choice of process and design
  - 8" to 12" wafers
    - low cost per area: "as cheap as chips" for large volumes
    - wafer thinning quite standard
  - usually p-type Cz silicon
    - thin active layer, helpful to disentangle tracks in boosted jets and at high eta
    - requires low capacitance → small pixel

- Basic requirement: Deep n-well (→ allows high(er) substrate bias)
  - existing in many processes, e.g. even 65nm (!)

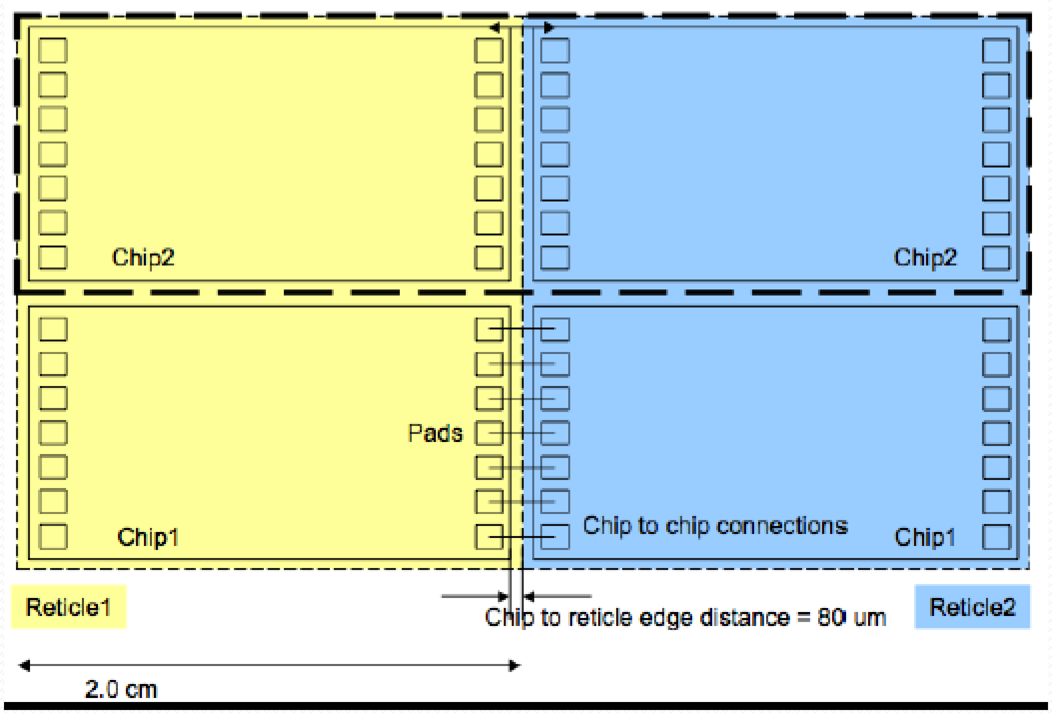
Strip-like Readout

- Signals are digital so multiple connections are possible, e.g.
  - "crossed strips"
  - strips with double length but only half the pitch in r-phi
- Multiple combinations to resolve ambiguities – pixel precision
  - with only ~4N
  - channels instead of N^2



Stitching

- Future Reticule sizes limited to ~ 20 x 25mm
- Viable large area devices require 'stitching'
  - Multiple instances of same circuit
  - Low complexity should ensure very high yield



(HV)CMOS Outlook

- Task-force established late 2013 to assess whether it is likely that HVCMOS technologies could be developed in time for ATLAS mass production (2016-2020)
  - Financial Resources
  - Effort
  - How to keep current programme going until HVCMOS is demonstrated fully

- Looks tight for ATLAS but I would expect (HV)CMOS will be a mature technology for experiments building in the 2020s
  - Likely to have a major impact on detector implementation!

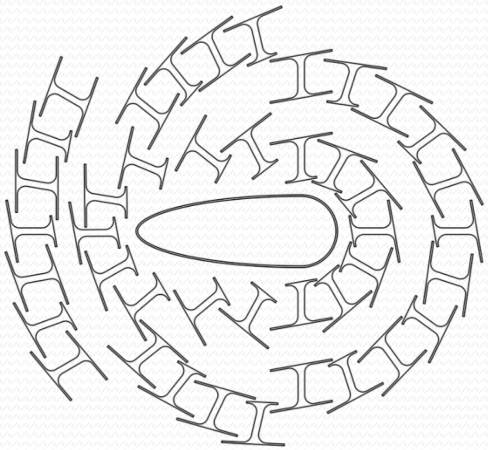
Conceptual LHeC Tracker Realisation

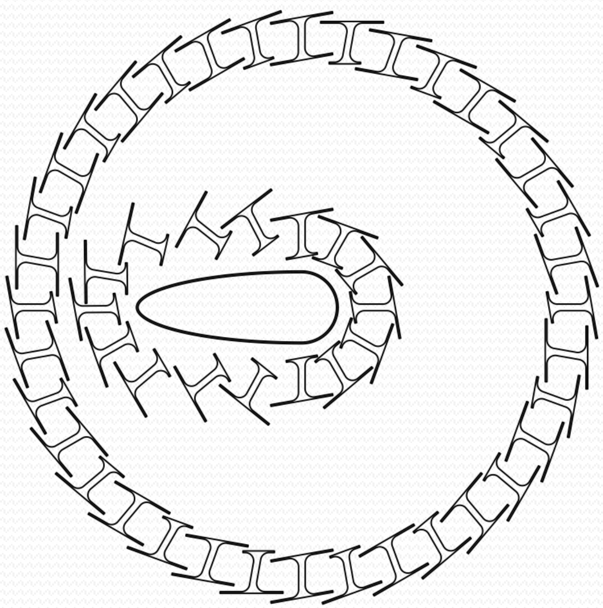
- Constraints
  - Use ATLAS Phase-2 tracker candidate detector technologies and map onto LHeC CDR geometry
  - In particular explore concept of ‘local supports’

- Describe details of
  - Central Pixel Tracker (CPT)
  - Central Strip Tracker (CST)
  - Central Forward/Backward Tracker (CFT/CBT)
  - Forward and Backward Silicon Trackers (FST/BST)

- Summarise area, modules, etc… compare to current ATLAS and upgrade. Point out differences to CDR.

Central Pixel Tracker (CPT)

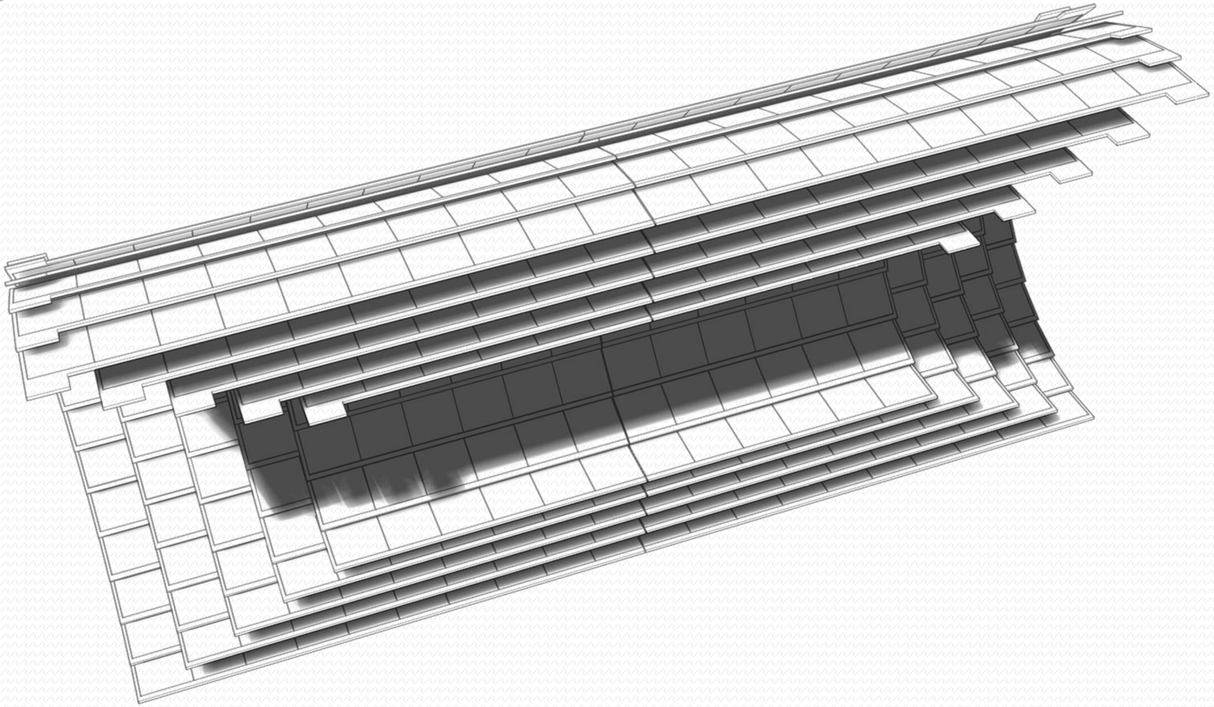


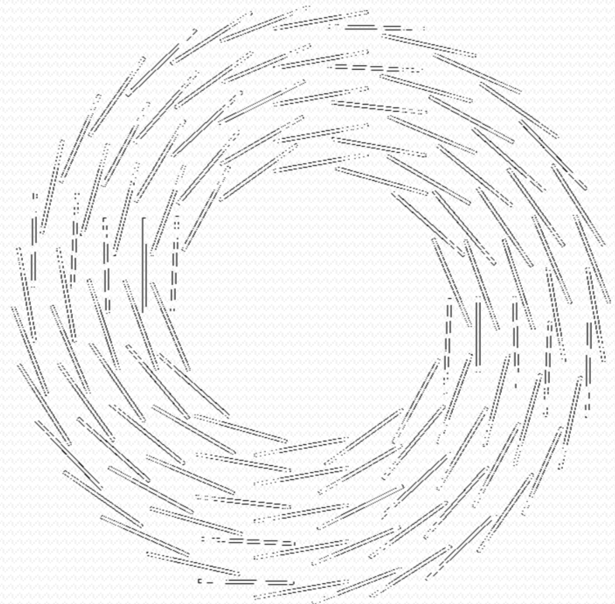


- Based on emerging ATLAS pixel design employing "I-beam" structures
  - Quad/doublet I-beam optimal if R2/R1 ~ 2
  - Mix of 2-types of stave
    - quad/quad and quad/doublet modules
  - R-phi overlaps can be significant

- 2 options studied
  - 4 incomplete concentric ring
    - 42 staves / 2.5m² / 7000 FE-I4
  - 2 complete rings
    - 52 staves / 3.1m² / 8700 FE-I4 (24% more area)

Central Strip Tracker (CST)





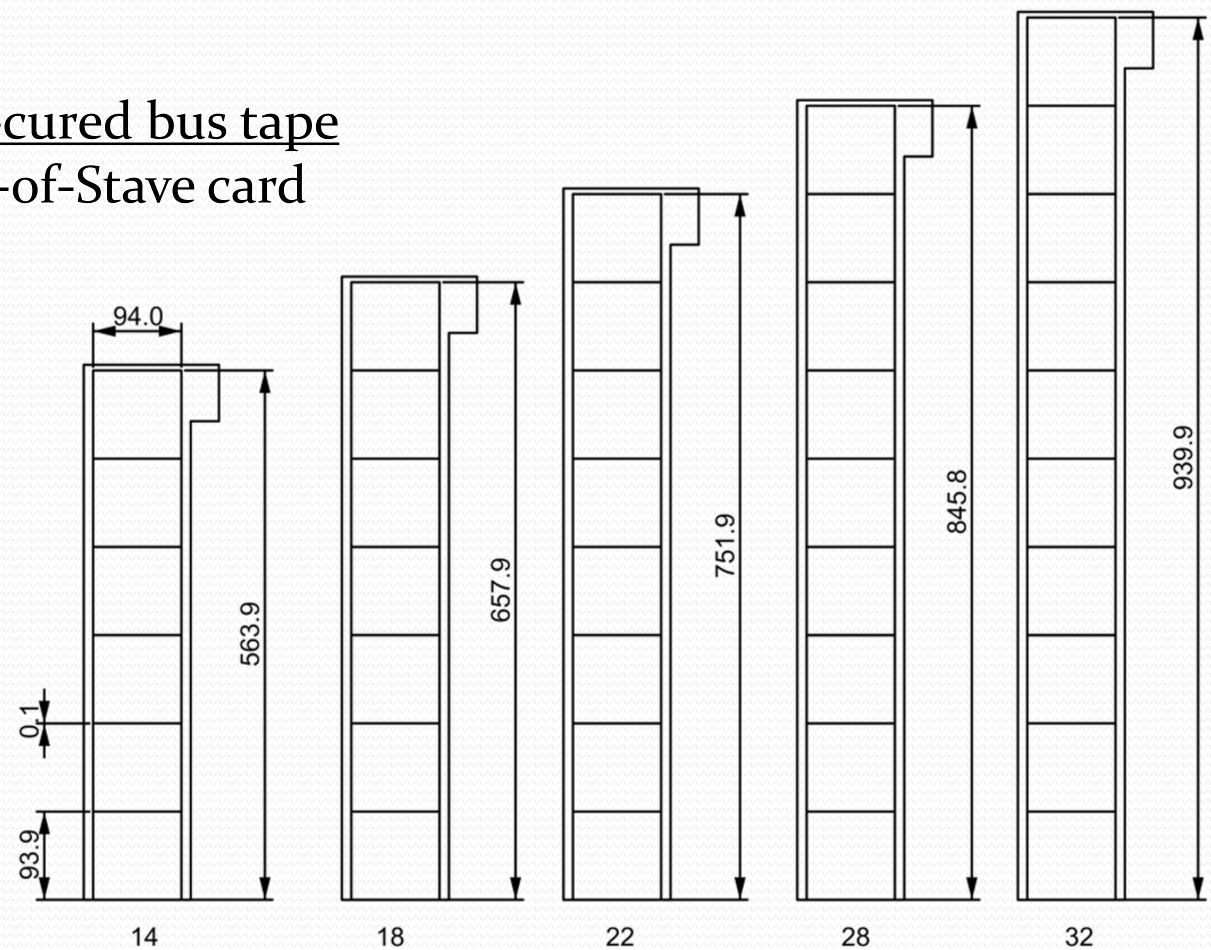
- 5 layer design based on emerging ATLAS strip stave development (without considering global supports & services!)
  - 14, 18, 22, 28 & 32 staves / end x 2 ends = 228 (1/2 ATLAS)
    - Non-quadrant symmetry!
  - Side-mounted End-of-Stave readout to minimise Z gaps

Central Strip Tracker (2)

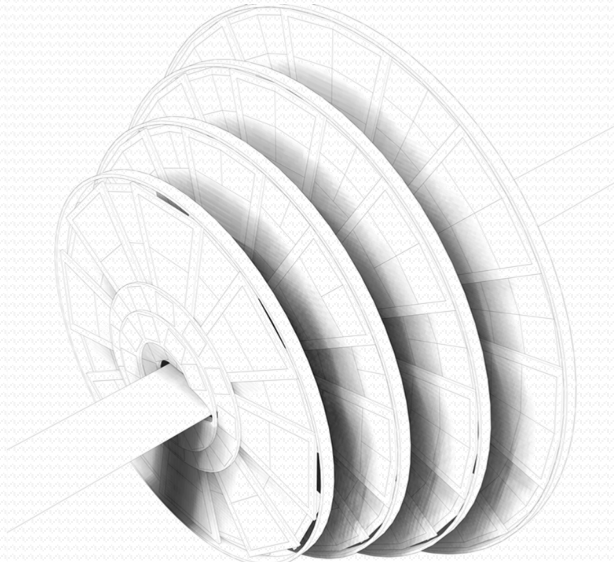
- Z coverage through integer numbers of identical modules on both sides
  - Axial / stereo
  - 94x94mm sensors
  - Power & I/O via co-cured bus tape
  - Side-mounted End-of-Stave card

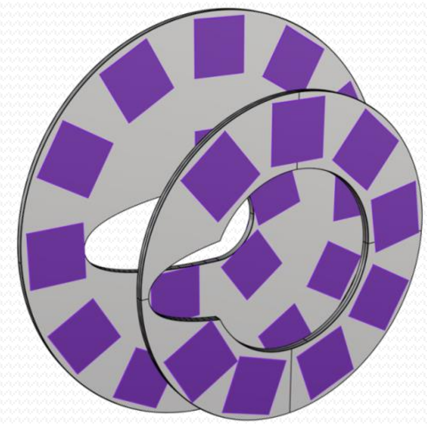
- Statistics
  - 228 staves
  - 3,832 modules
  - Area = $34 m^2$

- NB
  - L1 too short
  - L2-4 too long
  - L5 OK !

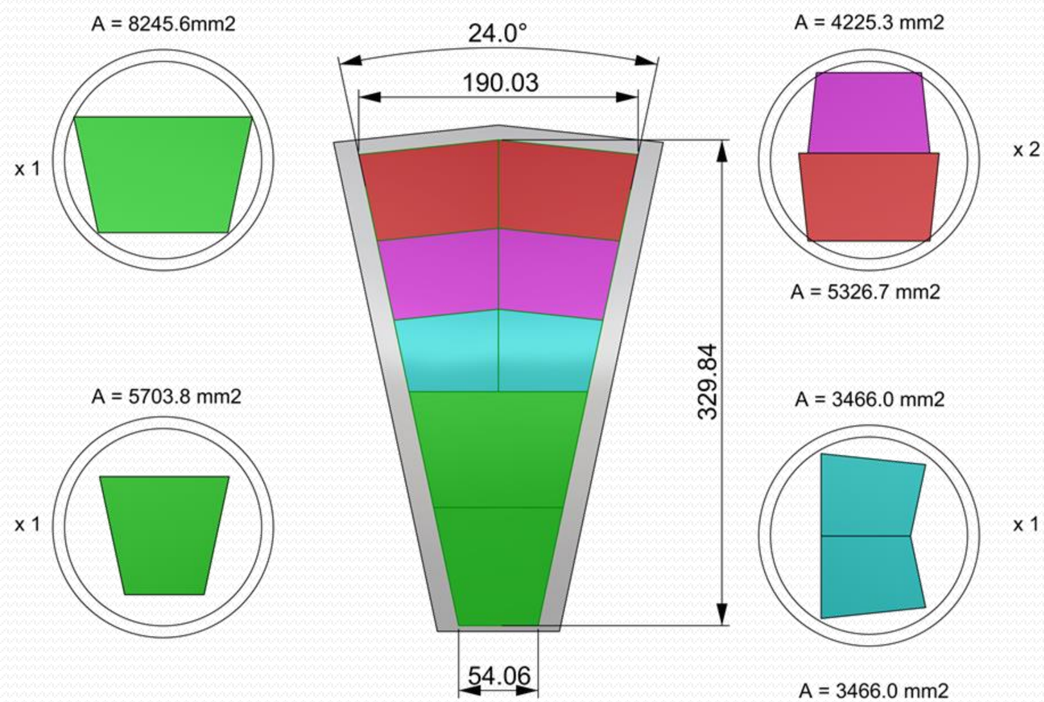


Central Forward (Backward) Tracker (CFT/CBT)

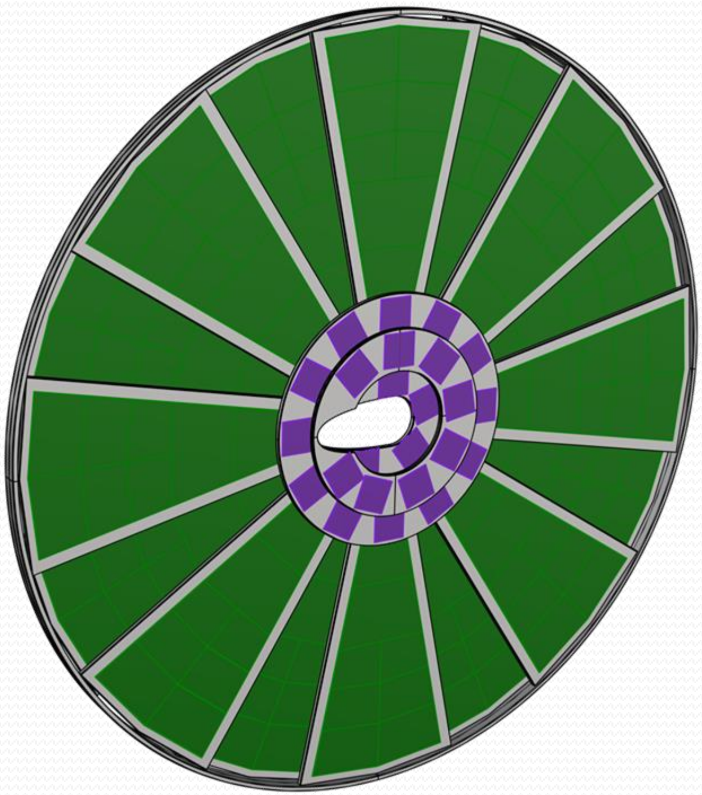




- Split in to 2 parts
  - Inner pixels (r<149mm)
    - quad modules
    - 3 rings: 8, 16, 24 modules
    - Area: 0.28m² / end
  - Outer strips (r> 132mm)
    - 18 double-sided petals
    - 2 to 5 rings
    - Area: 3.75m² / end

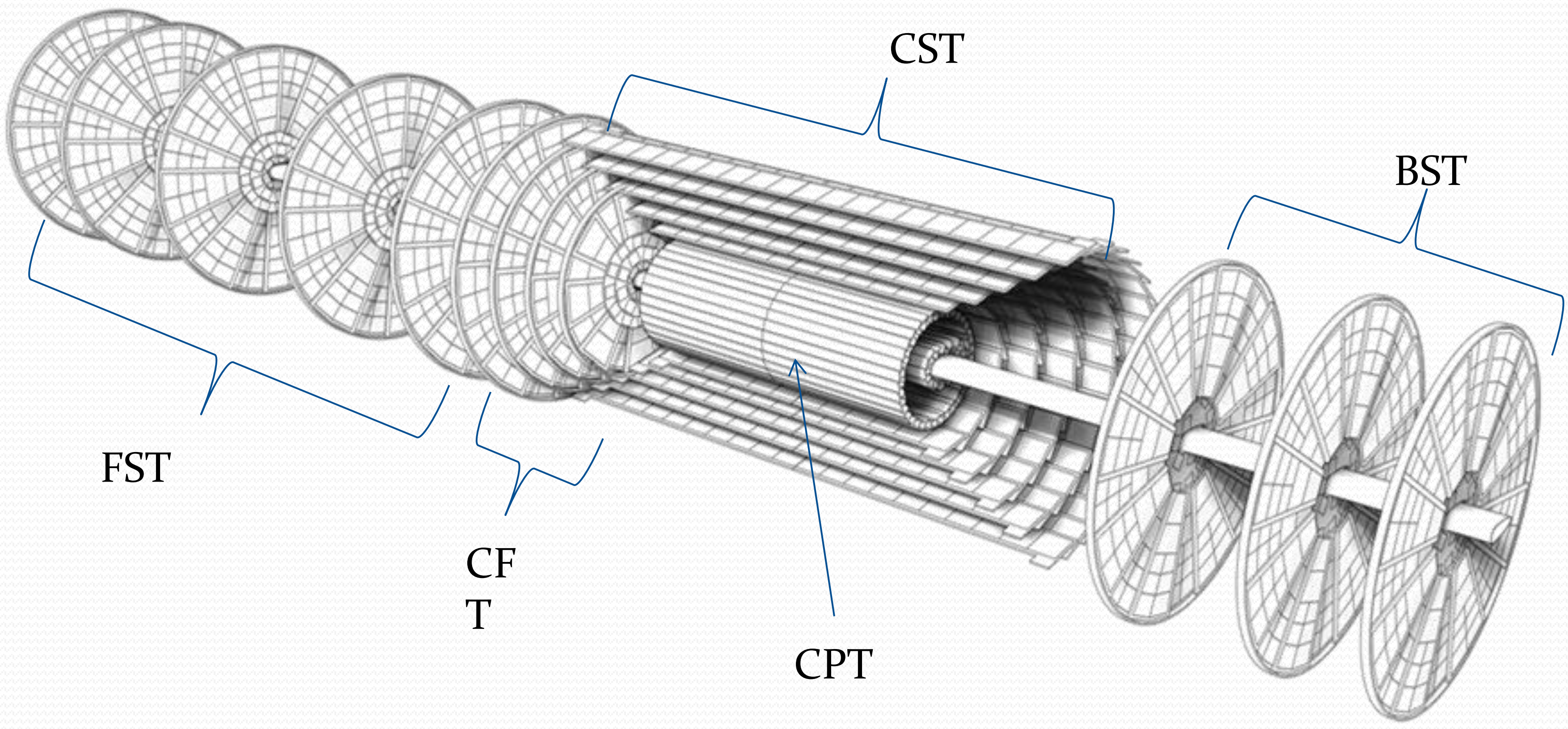


Forward (Backward) Silicon Trackers (FST/BST)



- Modelled as being identical to largest CFT/CBT disks
  - 3 pixel rings (r<149mm)
  - 5 strip rings (r>132mm)
  - Outer radius 457mm (should be 462)
- FST (5 disks):
  - Pixel area = $0.35m^2$
  - Strip area = $7.2m^2$
- BST (3 disks): Treated as being the same here (is it worth inventing something new?)
  - Pixel area = $0.21m^2$
  - Strip area = $4.3m^2$

General View



NOTE: CBT not shown for clarity

Summary Table

Central Barrel	CPT1	CPT2	CPT3	CPT4	CST1	CST2	CST3	CST4	CST5
Min. Radius R $[cm]$	3.1	5.6	8.1	10.6	21.2	25.6	31.2	36.7	42.7
Min. Polar Angle $\theta[^0]$	3.6	6.4	9.2	12.0	20.0	21.8	22.8	22.4	24.4
Max. $\|\eta\|$	3.5	2.9	2.5	2.2	1.6	1.4	1.2	1.0	0.8
ΔR $[cm]$	2	2	2	2	3.5	3.5	3.5	3.5	3.5
$\pm z$-length $[cm]$	50	50	50	50	58	64	74	84	94
Project Ar									

Central En	CBT3	CBT4
Min. Radi	3.1	3.1
Min. Polar	178	178.2
at z	-90	-101
Max./Min.	-4.0	-4.2
Δz	7	7
Project Ar	8	

Fwd/Bwd	BST2	BST3
Min. Radi	3.1	3.1
Min. Polar	178.9	179.1
at z	-170	-200
Max./Min.	-4.7	-4.8
Outer Rad	46.2	46.2
Δz	8	8
Project Area $[m^2]$	3.3	2.0

Sub-detector	Area (m^2)		Modules		
	Pixels	Strips	Pixels(Q)	Pixels(D)	Strips
CPT	2.53	0.00	1400	700	0
CST	0.00	33.86	0	0	3832
CFT	0.28	3.75	192	0	720
CBT	0.28	3.75	192	0	720
FST	0.35	7.20	240	0	1440
BST	0.21	4.30	144	0	864
Total	**3.65**	**52.86**	**2168**	**700**	**7576**

Global Design Issues

- Global supports and services
  - Staggered barrel looks challenging
    - Most barrel systems end up 'square ended'!
    - One could imagine extending ATLAS stave co-curing technology to fabricating support cones with integrated services
  - ATLAS uses concept of 'services modules' – tightly integrated package (cooling, electrical & optical services)
    - Rapid installation (reduces on-surface assembly time)
    - Compact unit (optimises space)
- Environment (Temperature, humidity & gas, G&S)
  - Active thermal enclosures – space ?
  - Humidity barriers & seals around services
  - Grounding & shielding scheme often comes late & requires 'on the fly' implementations – need to address early in design phase
- Access & maintenance requirements
  - eg. ATLAS allows removal of pixel sub-system without interfering with strips (segmentation in R not Z)
    - Multiple 'tubes' & associated material in far forward direction

Conclusions & Outlook

- A first-go geometrical implementation of the CDR layout made using ATLAS Phase-2 upgrade prototype designs as motivation
  - Looks feasible and a reasonable basis for further work
  - Not a unique solution – developments of CMS/ALICE tracking system upgrades would be equally valid

- Allows calculation of module numbers & silicon area based on realistic assumptions
  - Active areas of some sub-components disagree with table from CDR
  - Implementation of CPT is quite far from CDR design

- Global supports & Services
  - Not addressed here but would have a major impact on any design