A tile calorimeter for the LHeC

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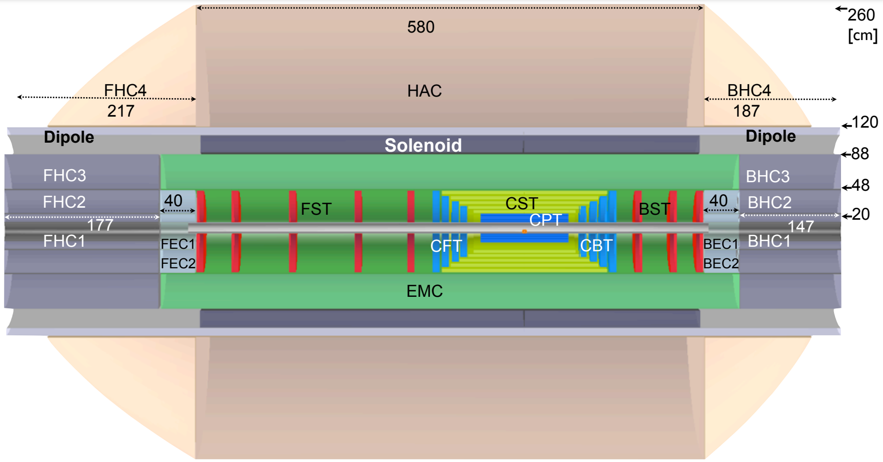
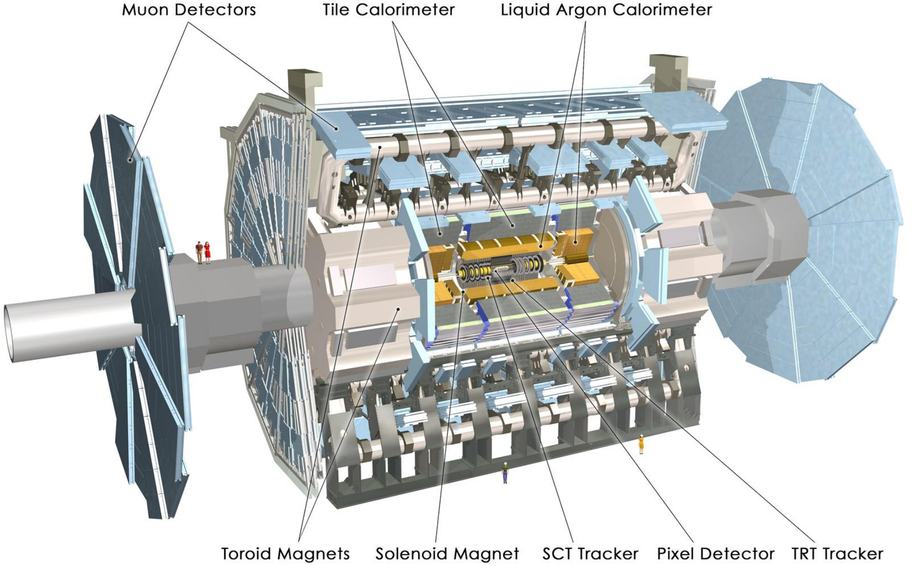
Introduction

- The CDR of the LHeC considers a tile calorimeter for the hadronic barrel calorimeter in the baseline detector option
  - Inner silicon tracker with extended forward and backward parts
  - EM calo surrounded by 3.5T field
  - Tile hadronic calorimeter enclosed in a muon tracking system
- We compare the preliminary simulations of the HAC with the performance of the ATLAS Tile calorimeter
- Since LHeC is planned for LS3 we can profit from the lessons learnt from ATLAS



LHeC baseline detector option (without muon system) for the Linac-Ring machine option

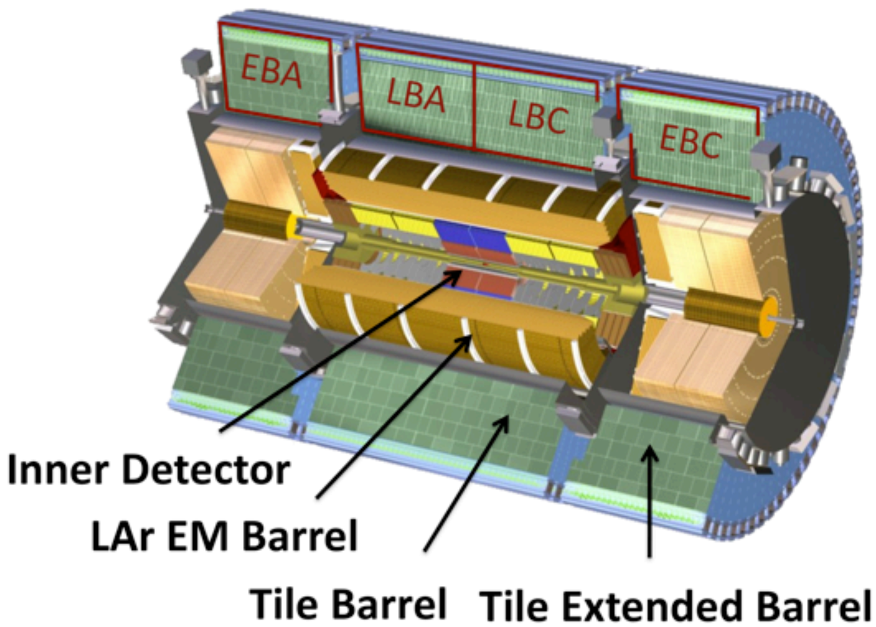


ATLAS Experiment

The ATLAS Tile calorimeter

- The ATLAS hadronic Tile calorimeter is a hollow cylinder that covers the range $|\eta| < 1.7$
  - Note $\eta = -\log(\tan(\theta/2))$
- Mechanically divided into three barrels one long barrel instrumented on both sides, and two extended barrels, and staggered in ϕ
- Based on a sampling technique where plastic scintillating tiles are embedded in a steel absorber plates
  - Number of nuclear interaction lengths at $\eta=0$ ($\theta=90^{\circ}$) is 7.4
- Design performance jet resolution for combined calorimeters

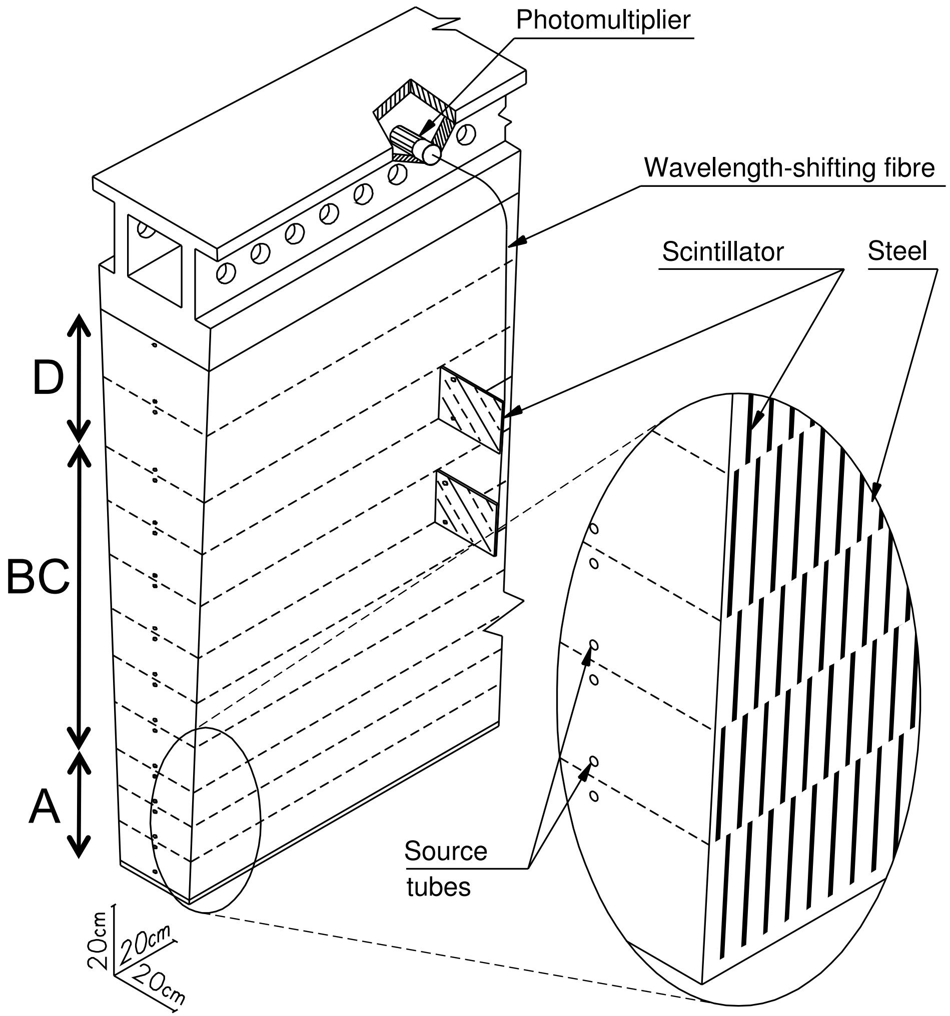
$$\frac{\sigma}{E} = \frac{50\%}{\sqrt{E(GeV)}} \oplus 3\%$$



	ATLAS	LHeC
Inner radius	2.28 m	1.20 m
Outer radius	4.25 m	2.60 m
Length in Z	12 m	9.78 m
Weight	2900 tons	~900 tons

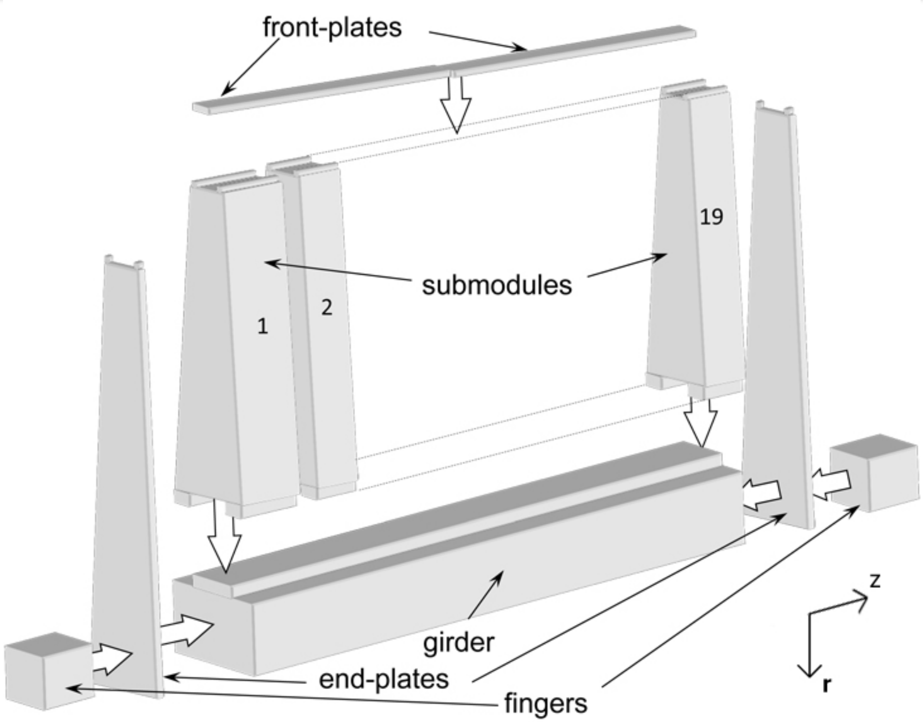
Detector facts

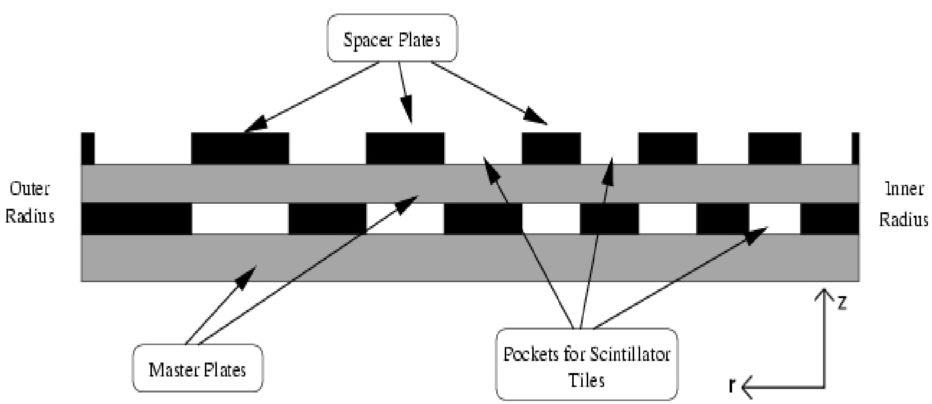
Tile modules



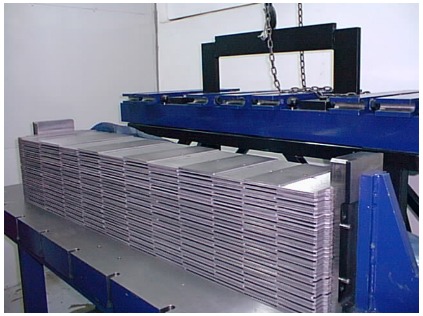
- Each barrel is divided into 64 modules providing a ϕ granularity of 0.1 rad
- Tiles are trapezoidal shaped scintillators which are placed in the gaps of the module, perpendicular to the beam direction
  - Eleven rows of tiles are used for each module
  - Two calibration source tubes cross each row
- Each tile is read-out on both sides by wavelength shifting fibers WLS that are coupled to the tiles along the external faces of the module
  - Read-out electronics are located in the outermost region of the module

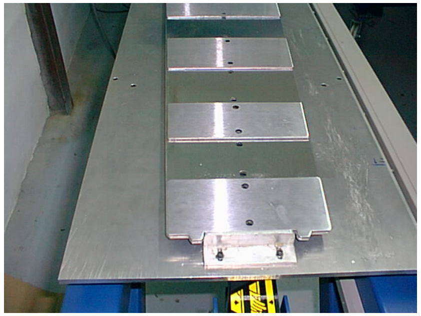
Tile module construction



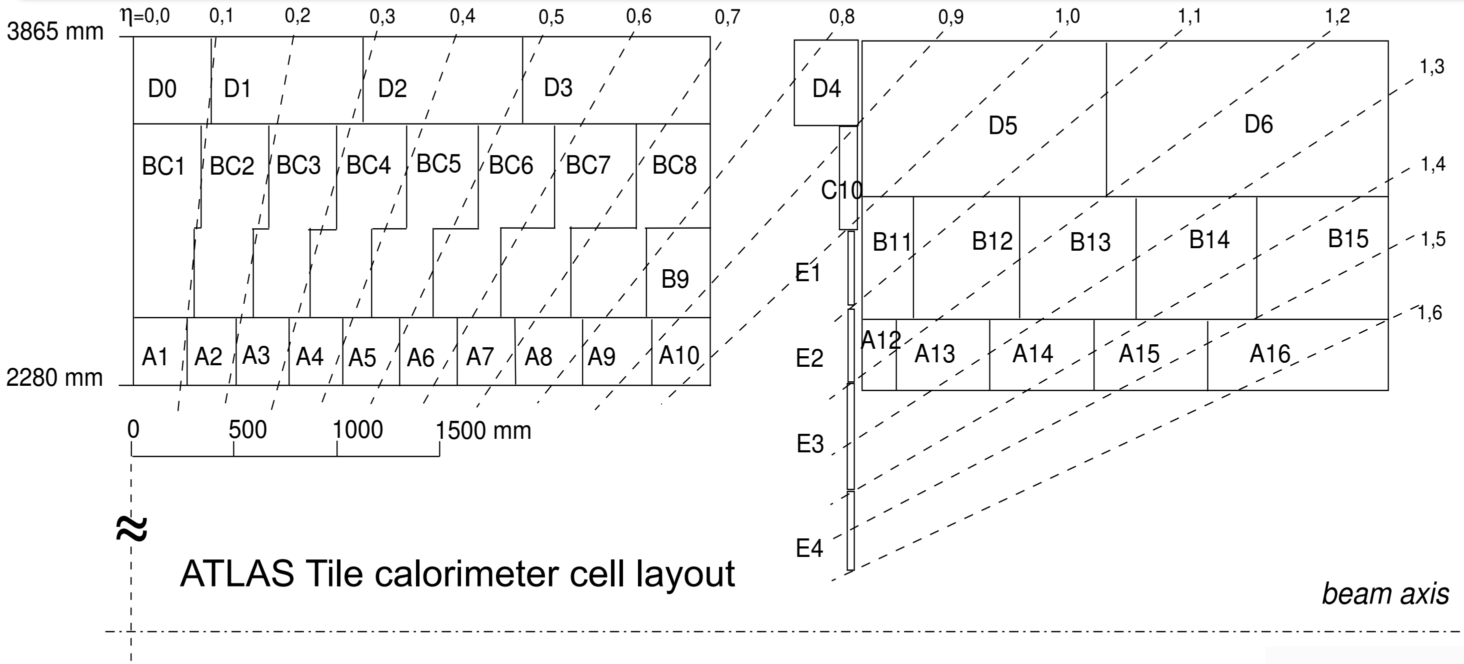


- Each module is built out of 19 sub-modules (~29 cm) which are attached to the girder
  - Constructed independently and before the optics instrumentation
- Spacer plates (4 mm) are placed in between two master plates (5 mm) leaving the space for the tiles (3 mm)
  - Periodicity of 18 mm
  - More details in 2013 JINST 8 T11001
- WLS fibers are placed along the spacer plates between two master plates without any compromise for extra space
- Similar assembly procedure can be followed for the LHeC detector





Cell layout



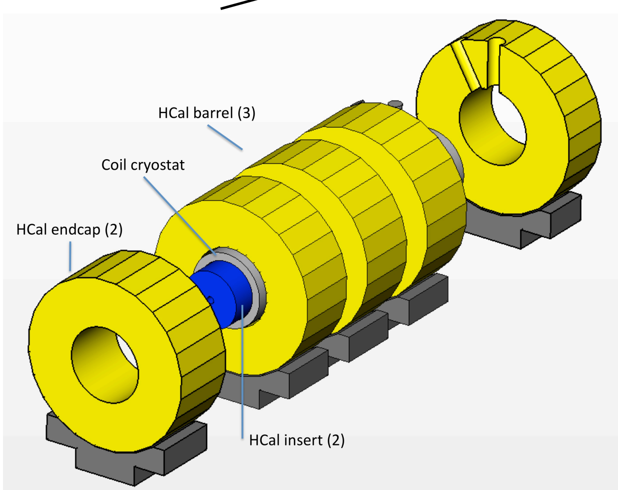
ATLAS Tile calorimeter cell layout

Size [mm]	ATLAS	LHeC
97	1-3	1-3
127	4-6	4-6
147	7-9	7-11
187	10-11	

Radial size of tile rows

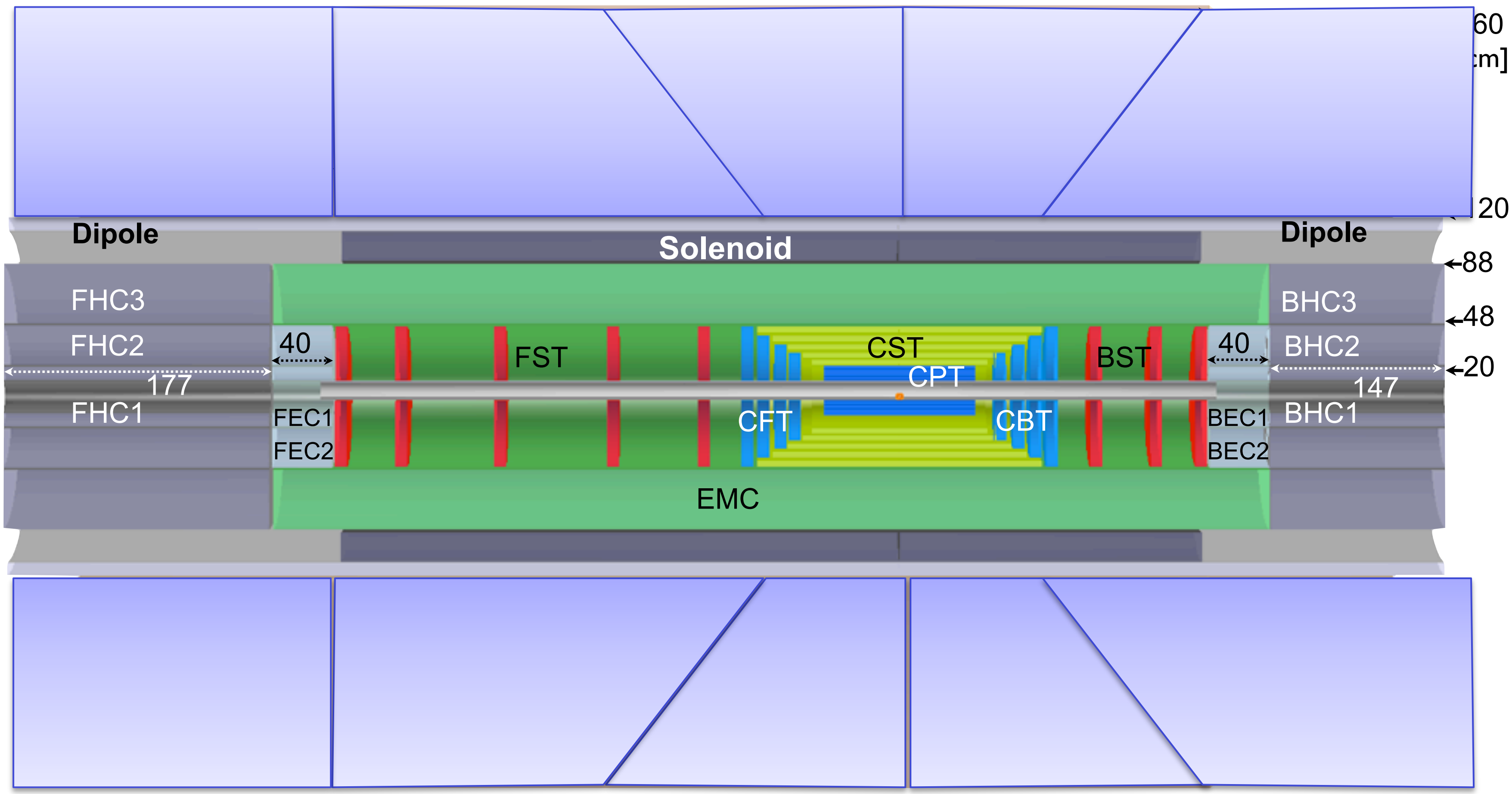
2013 *JINST* **8** P01005

- Groups of tiles are bundled together into cells and read out by photo-multipliers tubes (PMTs)
- Cells are laid out in order to have a projective geometry around the interaction point in steps of $\Delta\eta = 0.1$
- Tile is made out of 5182 cells of three types A (1.5λ), BC (4.1λ) and D (1.8λ)
- A projective cell segmentation is mandatory for LHeC
  - Might need an asymmetric granularity



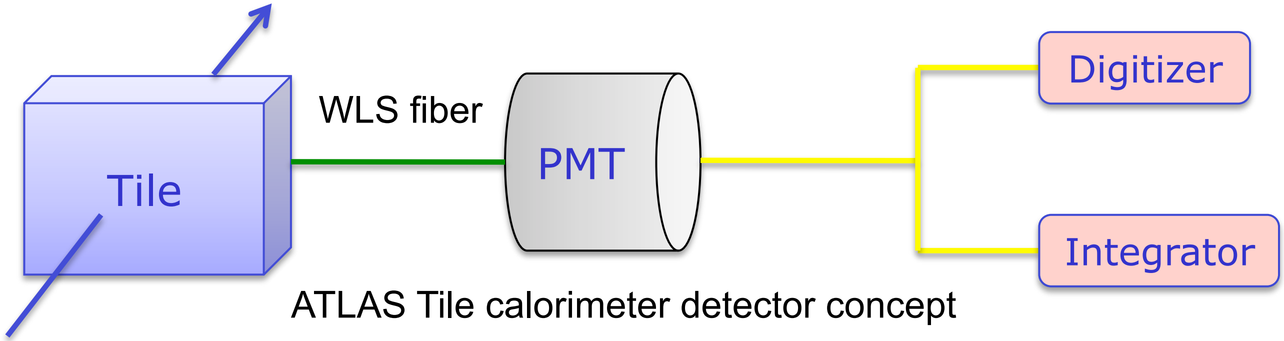
LHeC hadronic calorimeter concept

Projective barrel segmentation?



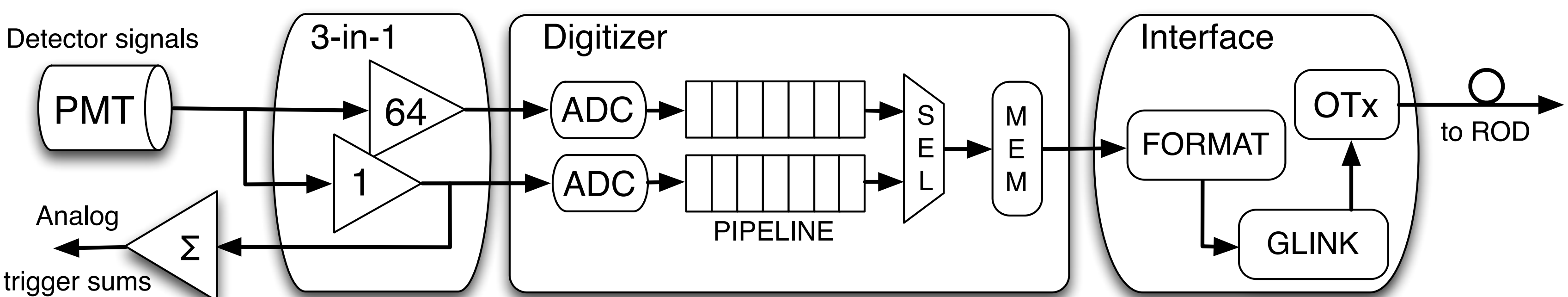
- Avoid splitting the barrel where more resolution is needed
- Minimize gap in the forward region to maximize coverage

Detector concept



ATLAS Tile calorimeter detector concept

- A Tile calorimeter is based on a simple detector concept
  1. Scintillation light is produced in the tile
  2. Light is collected by 2 WLS fibers (1 cell is read out by 2 PMTs)
  3. Electrical pulse produced by the photo-multiplier (9852 in ATLAS)
  4. Signal is sampled (and also integrated in ATLAS)
- Samples are stored in pipeline memories located in the front-end electronics
  - See upgrade plans to be considered for LHeC in following slides

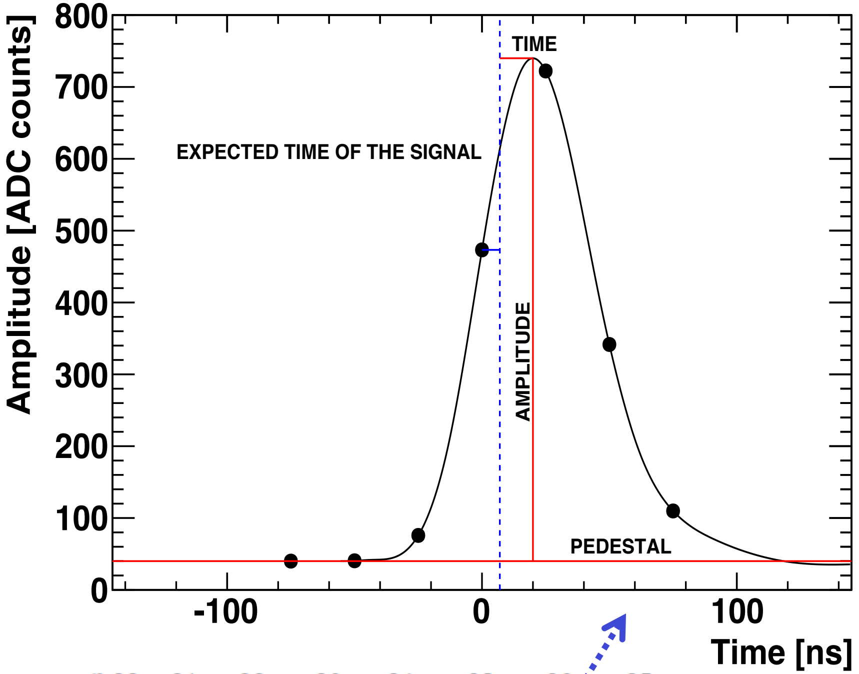


ATLAS Tile calorimeter read-out

Signal reconstruction

- The signal reconstruction in Tile is based on the Optimal Filtering
  - Amplitude and time are obtained through a linear combination of the digital samples
  - Weights are obtained from the signal pulse shape and the correlation matrix between the samples for an expected time of the pulse

$$A = \sum_{i=1}^{7} a_i S_i \quad \tau = \frac{1}{A}\sum_{i=1}^{7} b_i S_i$$

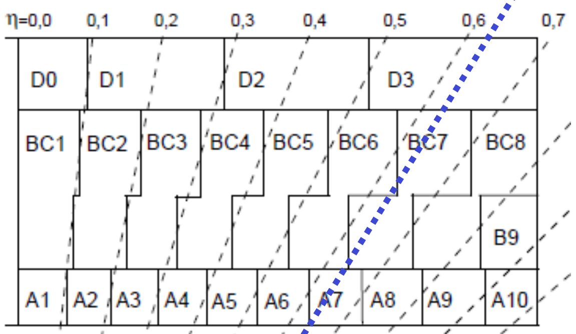


- Energy is proportional to the amplitude

$$E_{PMT} \propto A$$

- Cell energy is the sum of the two PMTs

$$E_{cell} = E_{PMT1} + E_{PMT2}$$



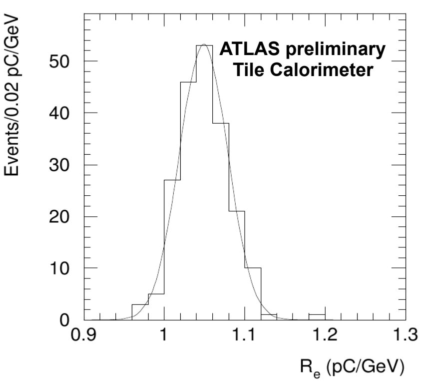
Signal deposits from particles originated in the IP should have reconstructed time equal to zero

- Fast and reliable for deterministic pulses.
  - Alternative reconstruction methods are under evaluation

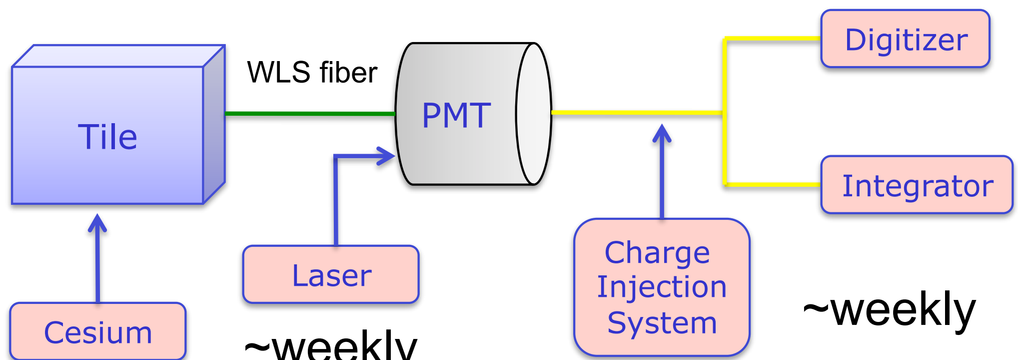
Energy calibration in Tile

$$E_{PMT} = C_{pC\rightarrow MeV} \cdot \varepsilon_{Cs} \cdot \varepsilon_{Laser} \cdot C_{ADC\rightarrow pC} \cdot A$$

Half cell energy | EM constant | Cesium equalization | Laser equalization | Charge Injection System | Reconstructed amplitude



Tile EM calibration is preserved in ATLAS by the Cs calibration system



~monthly

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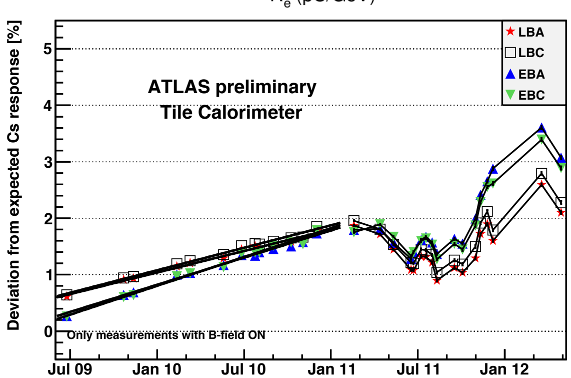
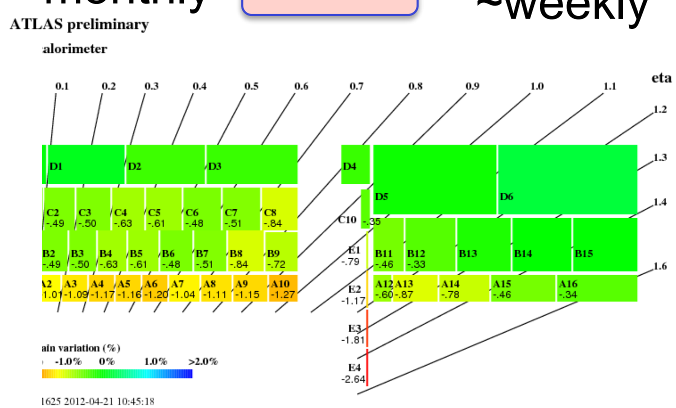
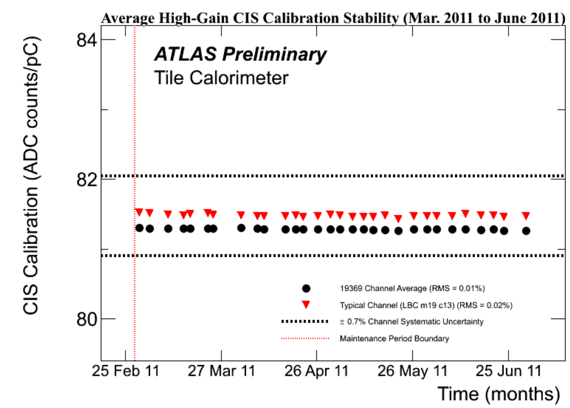
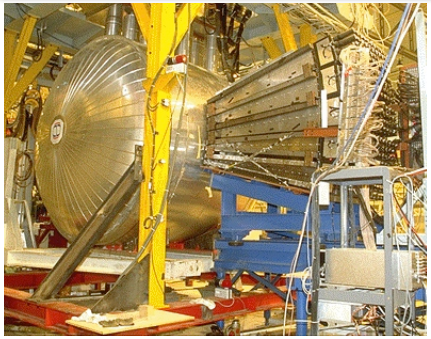


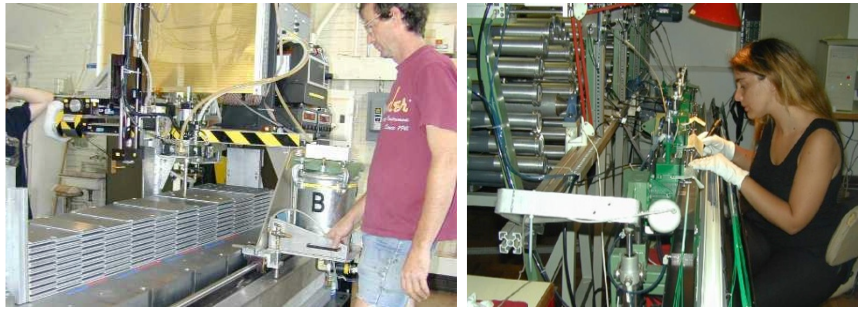




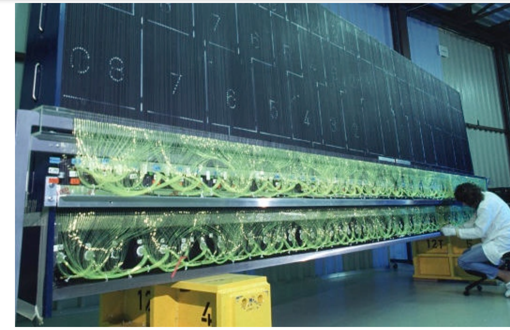
A bit of ATLAS history



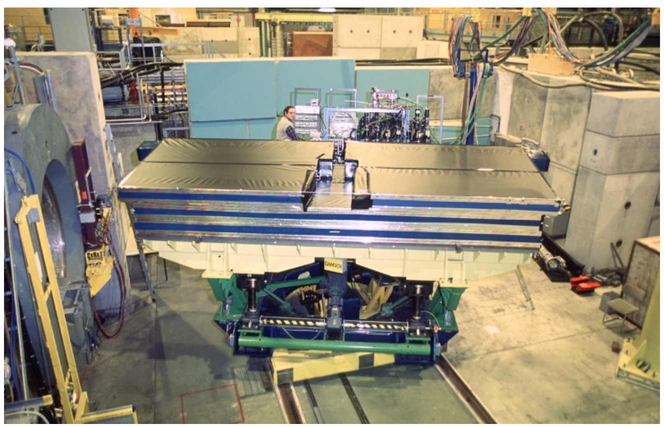
1993 – 1995: R&D



1996 – 2002: Construction



1999 – 2002: Instrumentation



2000 – 2004: Test-beam

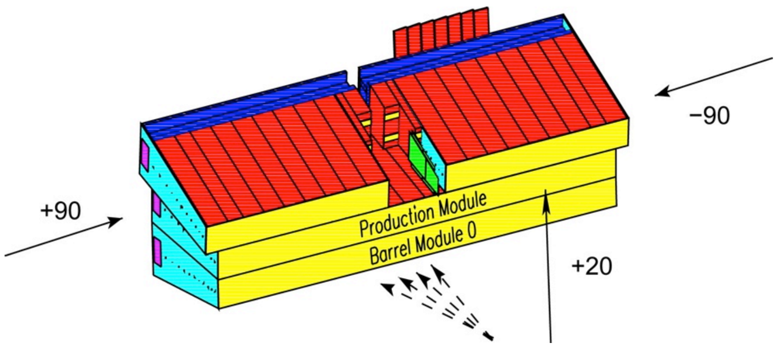
2004 – 2006: Installation

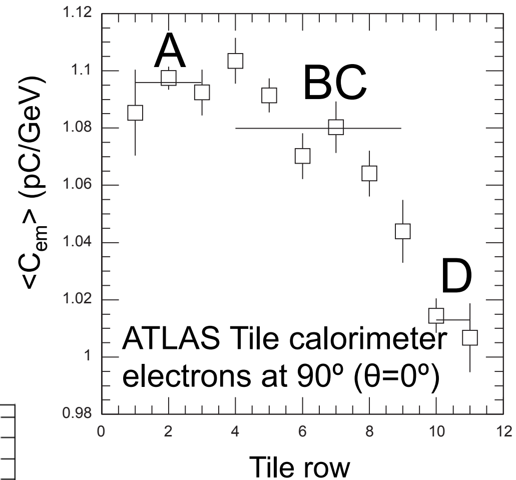
2005 – 2009: Commissioning with particles and calibration systems

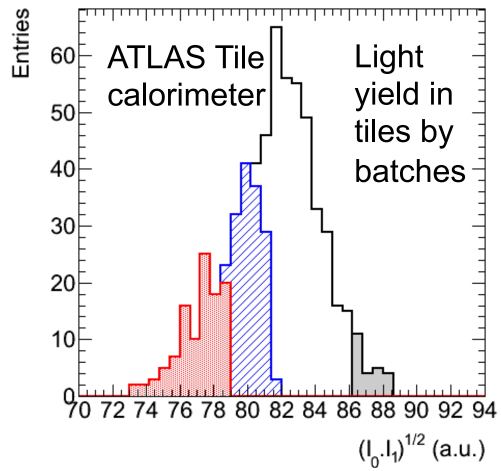
2010 – 2013: Operation in LHC run 1

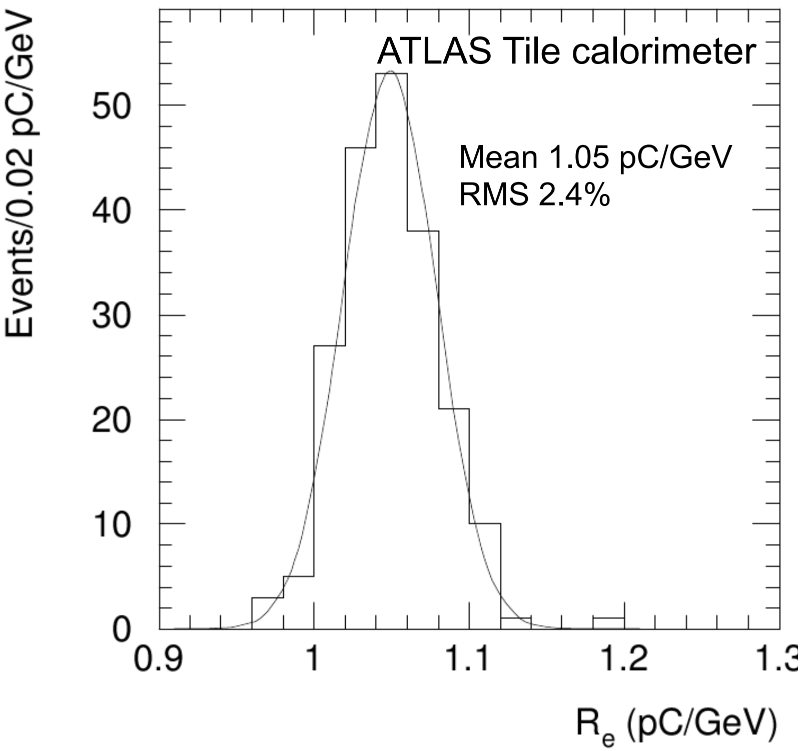
2013 – 2015: Electronics consolidation during Long Shutdown 1

Electromagnetic scale constant





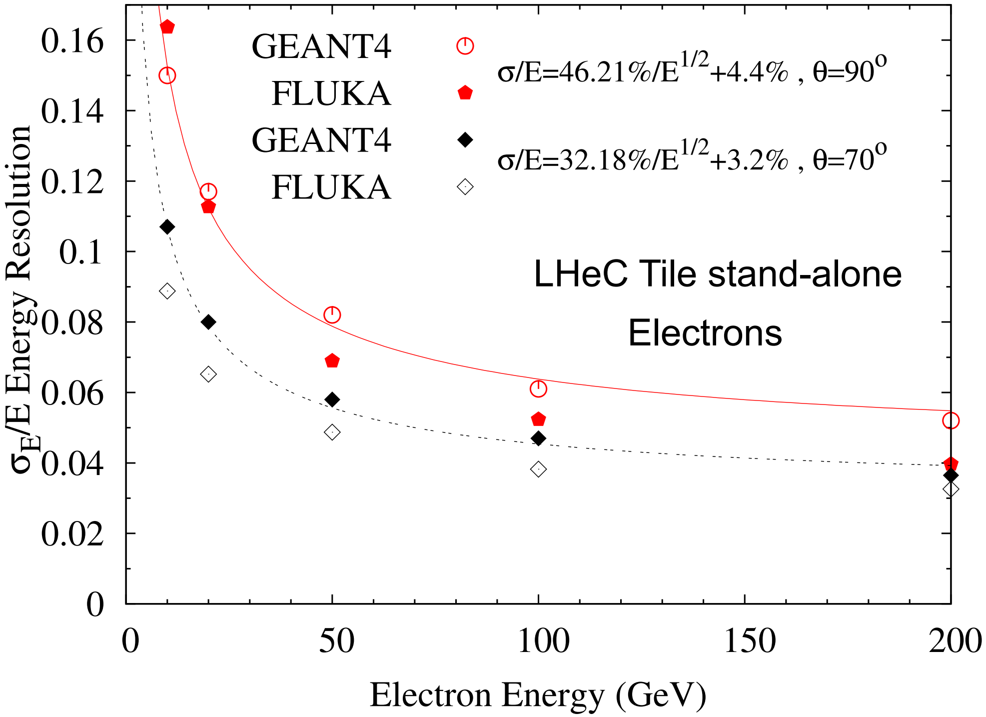


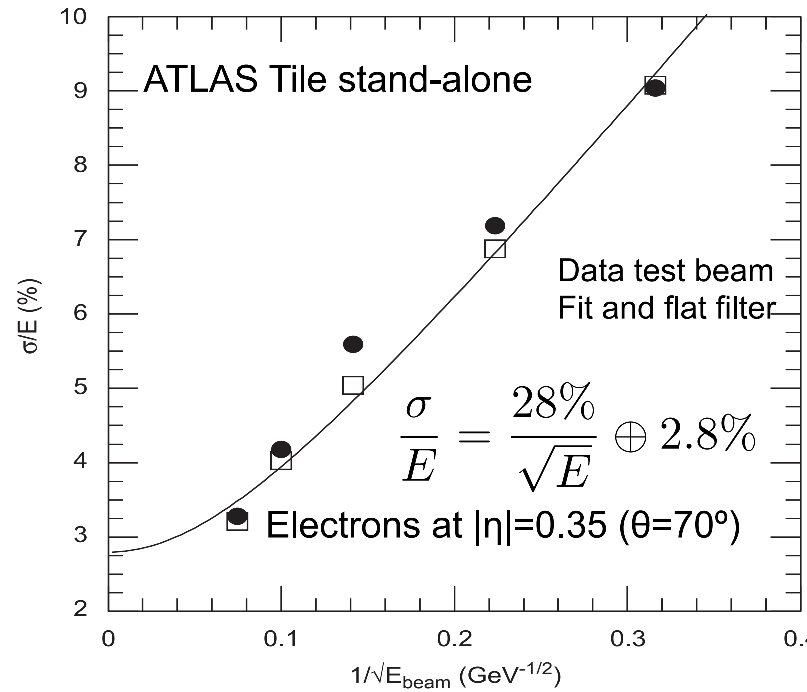


LHeC should aim for better uniformity in the tiles

- EM scale (Response/E_{beam}) was set at the test beam on the innermost radial layer (A) using using 20 to 180 GeV electrons with an incidence angle of 20º (θ=70º)
  - 11% of the Tile modules were brought to the H8 beam of the CERN SPS
  - EM scale constant : 1.05 pC/GeV with an RMS 2.4% (dominated by optics fluctuations)
- Scale is transferred to the other two radial samplings with electrons at 90º (θ=0º)
  - NIM A 606 (2009) 362–394
- Tile EM calibration is preserved in ATLAS by the Cs calibration system

Energy resolution for electrons

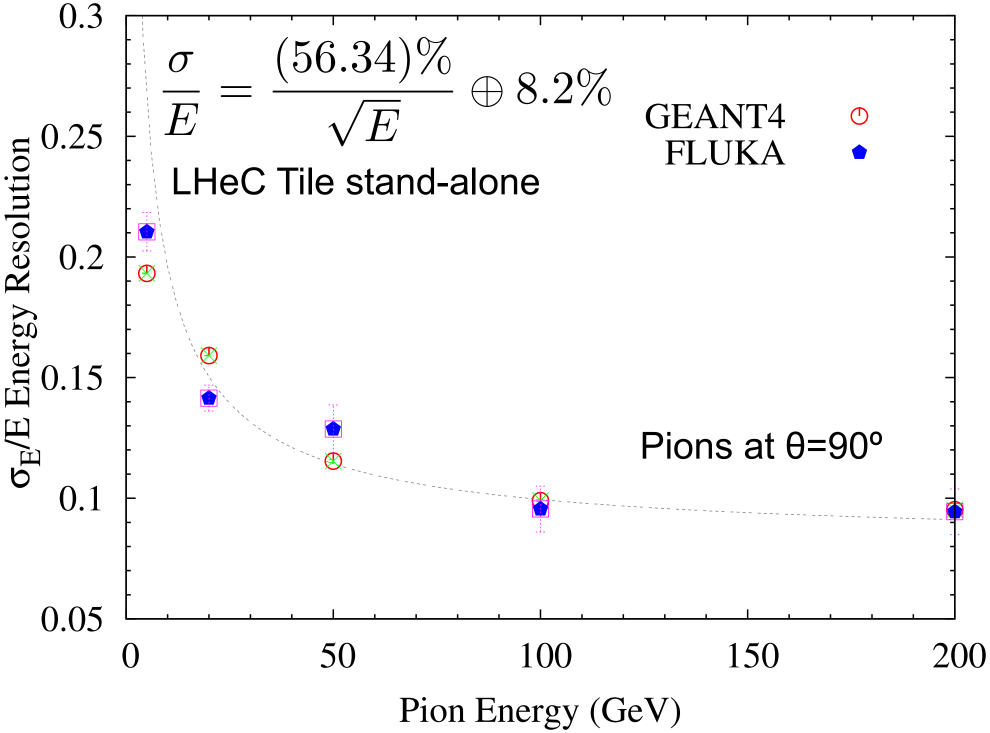


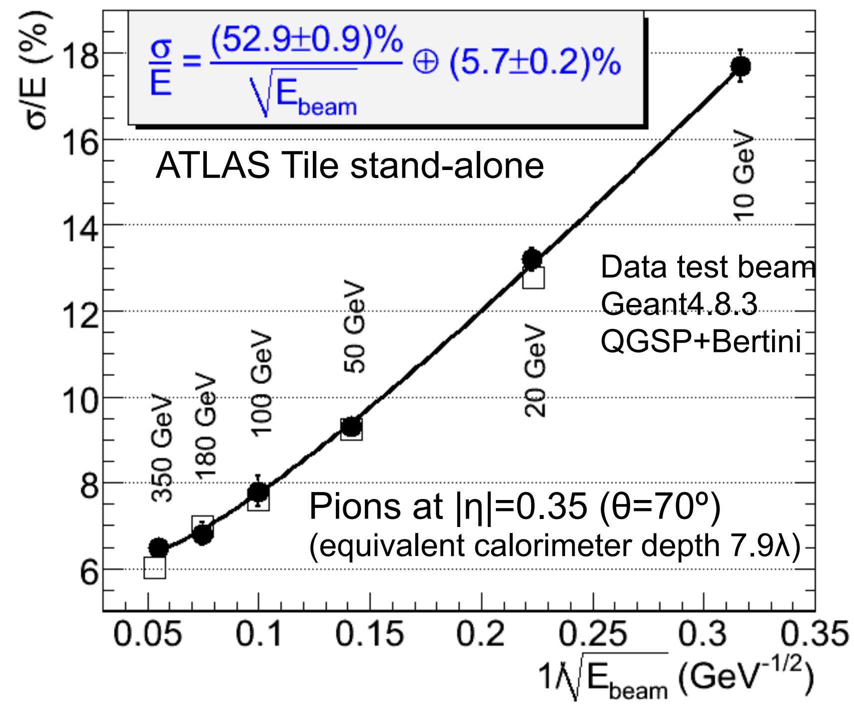


- Simulation of the energy resolution with electrons have been conducted for the stand-alone Tile calorimeter for the LHeC
  - Preliminary results are compatible with test-beam measurements for ATLAS Tile calorimeter
- Constant term comparable with local variation of response

NIM A 606 (2009) 362–394

Energy resolution for Pions





- Simulation of the energy resolution with Pions have been conducted for the stand-alone Tile calorimeter for the LHeC
  - Preliminary results are compatible with test-beam measurements for ATLAS Tile calorimeter
- Constant term affected by longitudinal containment
  - The expected constant term for jet energy resolution in ATLAS is typically 2.6%

Reconstruction Algorithm	$0 < \eta < 0.5$		
	a (%)	b (%)	c (GeV)
Cone $R_{cone} = 0.7$ Tower	64 ± 4	2.6 ± 0.1	4.9 ± 0.5
$k_T R = 0.6$ Tower	68 ± 5	2.5 ± 0.2	6.3 ± 0.5
Cone $R_{cone} = 0.7$ Topo	63 ± 4	2.7 ± 0.1	4.2 ± 0.5
$k_T R = 0.6$ Topo	64 ± 5	2.7 ± 0.2	5.4 ± 0.5

CERN-OPEN-2008-020, page 306, Table 3

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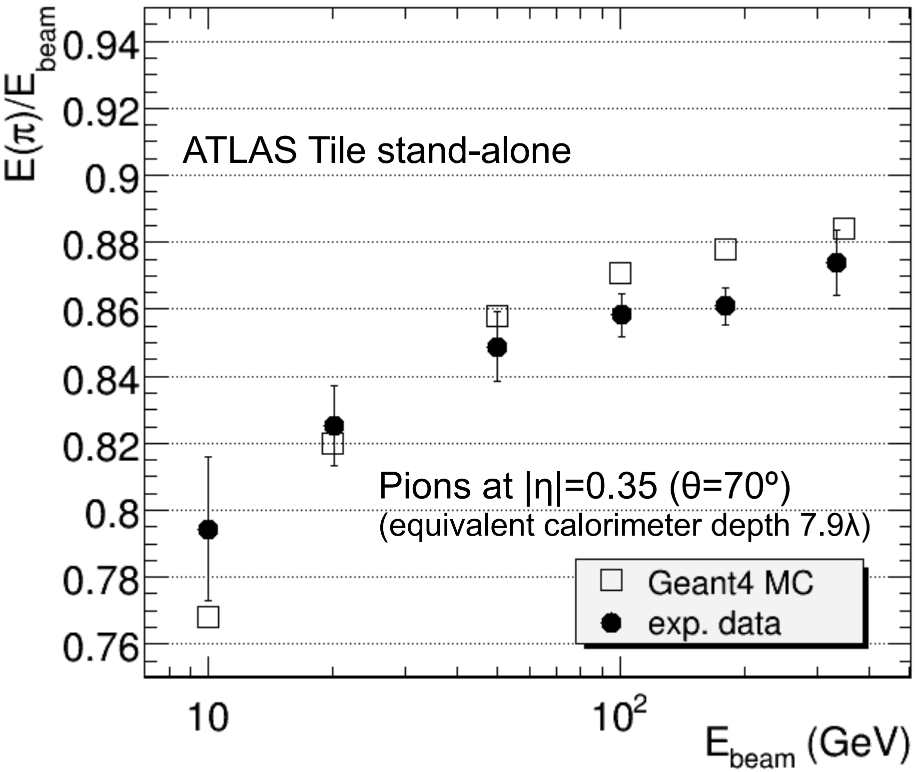
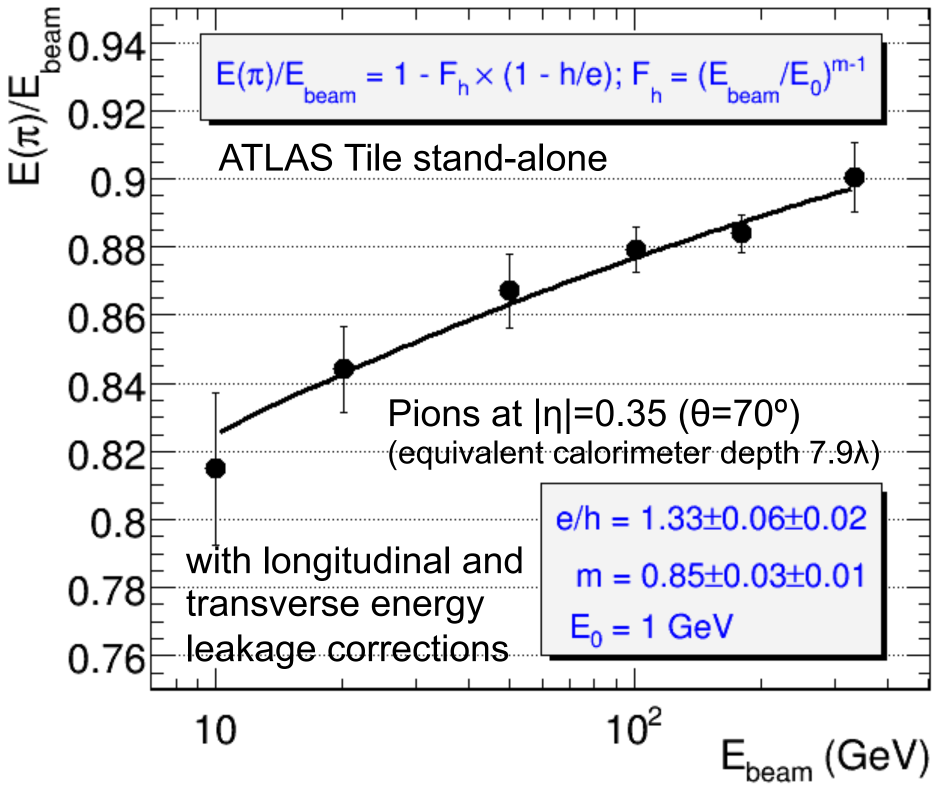
Pion response linearity

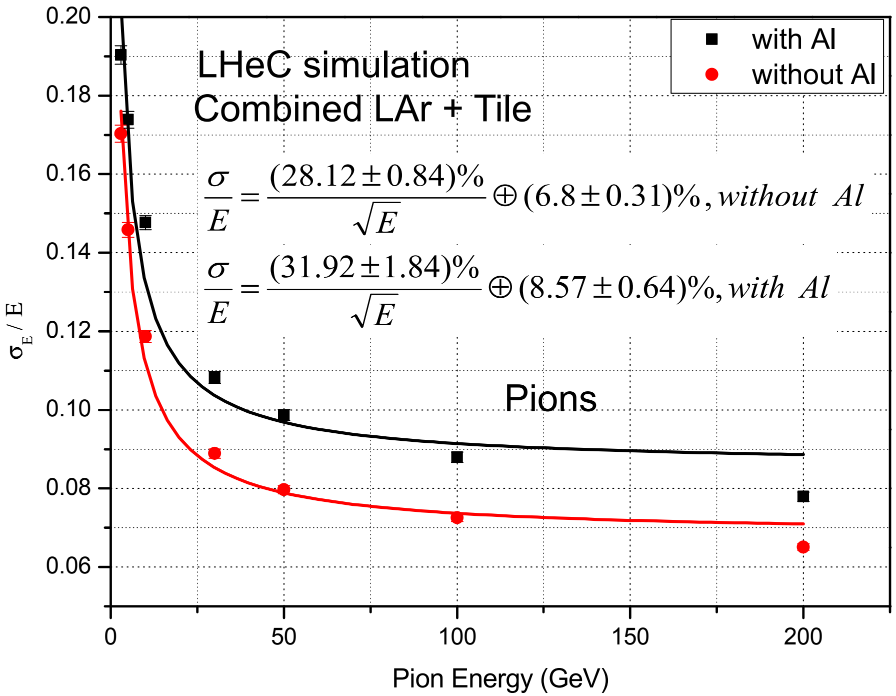


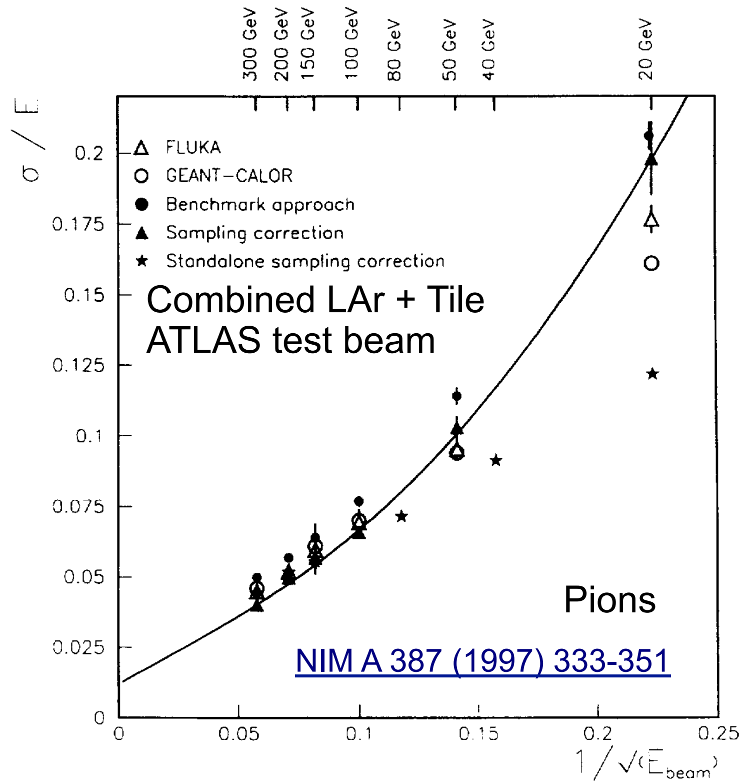


- The pion non linear energy dependence is due to calorimeter non-compensation
- Using Groom's parameterization of the non-EM component of hadronic showers we obtained e/h and m from the test beam measurements
- Sampling fraction should be calculated for LHeC

NIM A 606 (2009) 362–394

Combined calorimeter resolution





- Simulation of the energy resolution with electrons have been conducted for the combined LAr + Tile calorimeters for the LHeC
  - Preliminary results are better than test-beam measurements for ATLAS calorimeters
- The LHeC simulation is being compared in the CDR to
  - TILECAL 98 141 (which adds a noise term) and ultimately to NIM A 387 (1997) 333-351

$$\frac{\sigma}{E}=\left(\frac{(38.3\pm4.6)\%}{\sqrt{E}}+(1.6\pm0.1)\%\right)+\frac{(3.0\pm0.2)\%}{E}$$

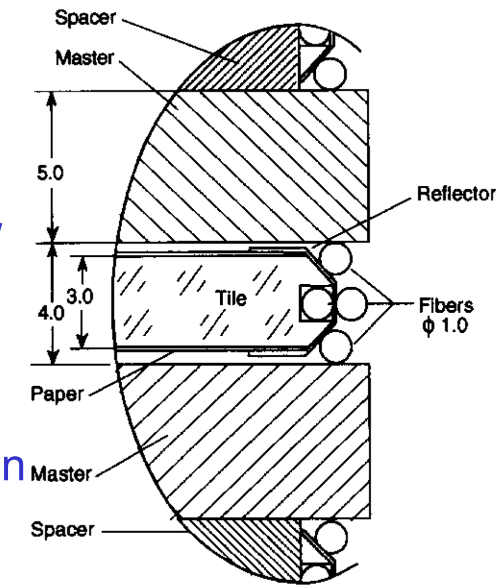
TILECAL 98 141

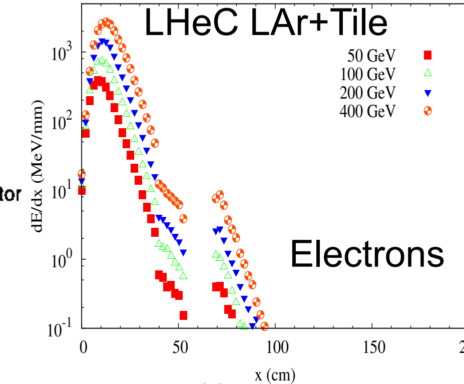
$$\frac{\sigma}{E}=\left(\frac{(46.5\pm6.0)\%}{\sqrt{E}}+(1.2\pm0.3)\%\right)\oplus\frac{(3.2\pm0.4)\%}{E}$$

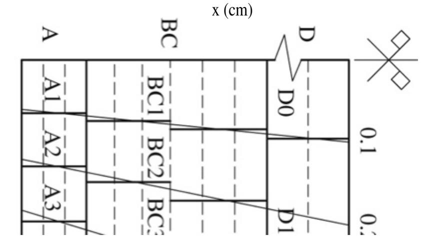
NIM A 387 (1997) 333-351

Can we improve the resolution?

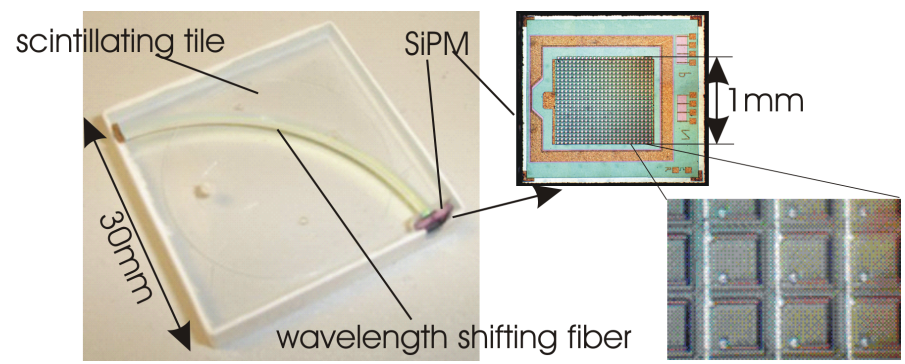
- We know there is an attenuation effect in the tile, edges yield more light
  - Should study ways of increasing the light yield by evaluating alternative tile/ WLS couplings
- We should aim to identify EM from hadronic showers
  - Increasing the cell granularity at least in the first radial sampling but need to increase the light yield
  - Or use an alternative SiPM with reduced size to increase the number of channels by a factor 2 – 11 (all the tiles)
- Reduction of the stochastic term of the resolution still remains an issue
  - Not feasible to change the thickness of the absorber
  - More efficient photomultipliers, increase lateral and longitudinal information?







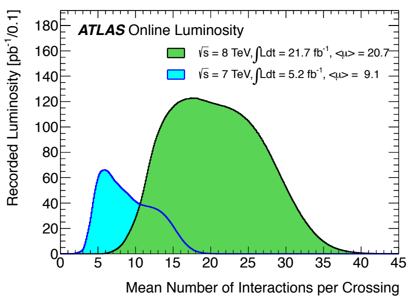
ATLAS Tile rows

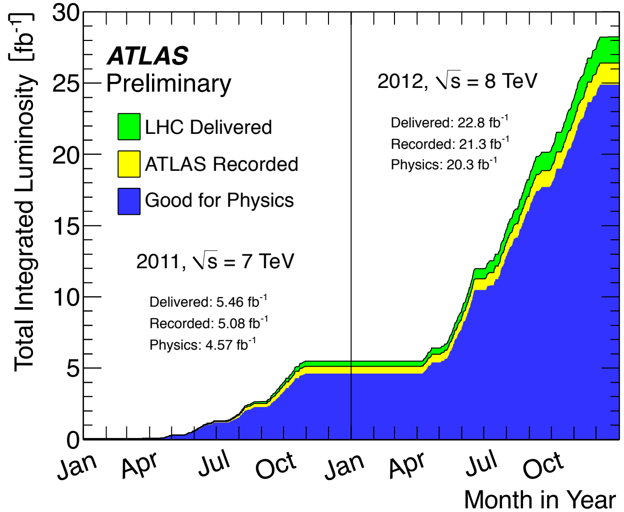


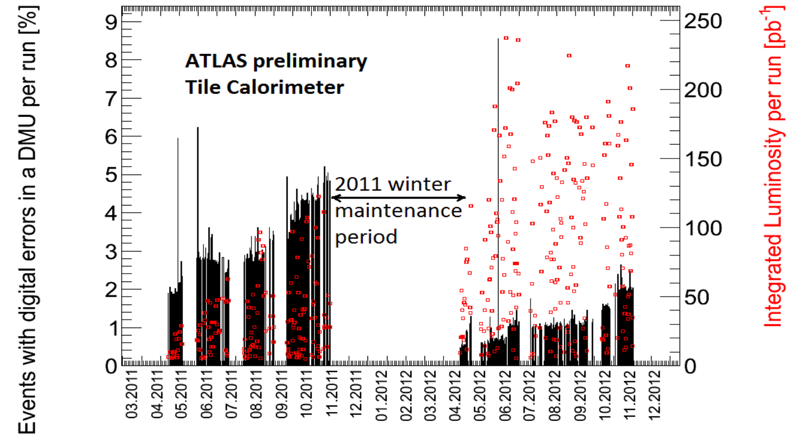
CALICE read-out for HCAL

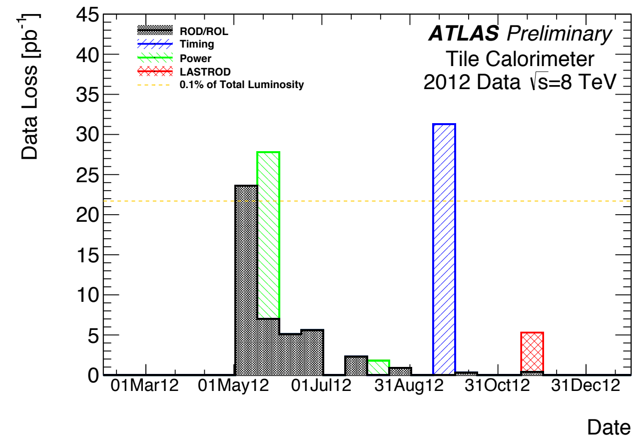
Tile operation summary in Run 1

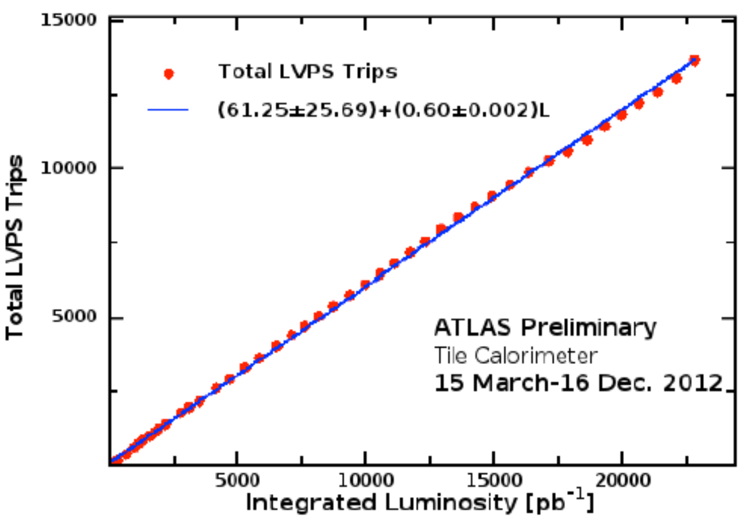
ATLAS Tile has been easy to operate in Run 1, despite...

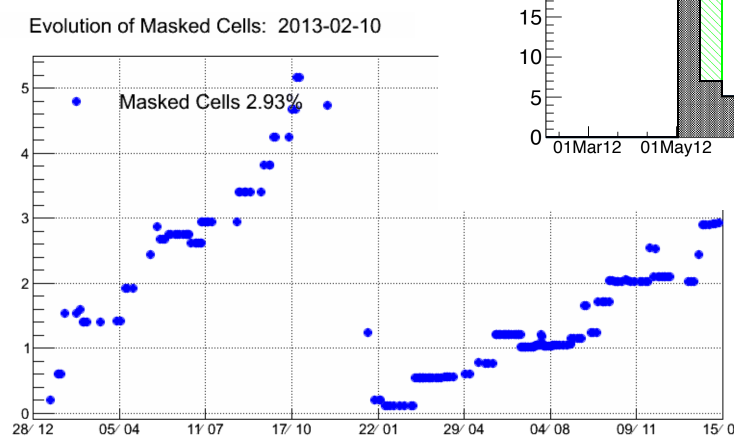








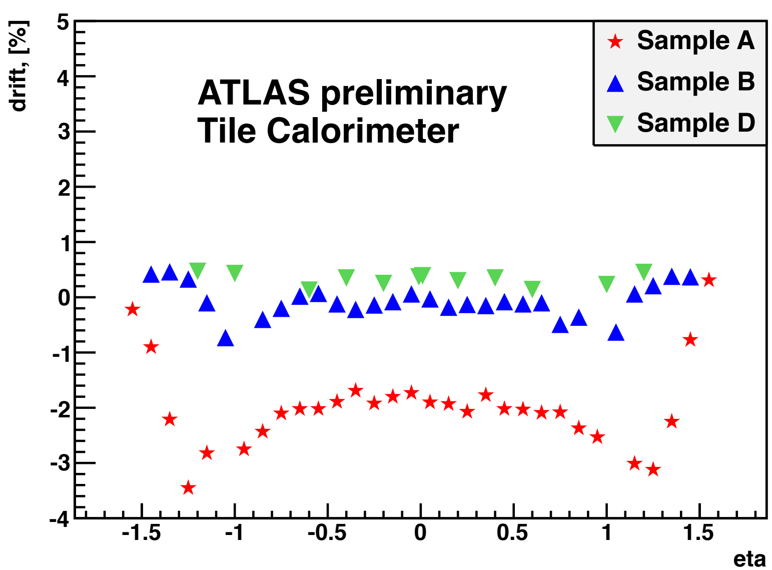


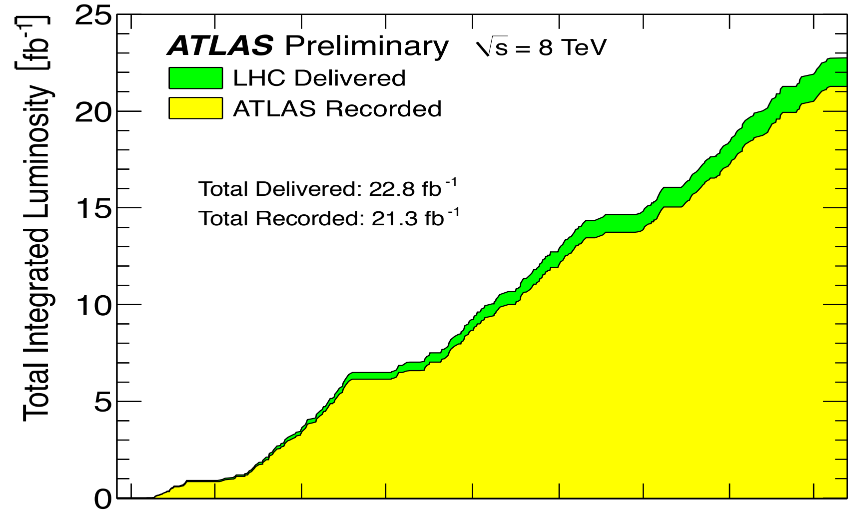


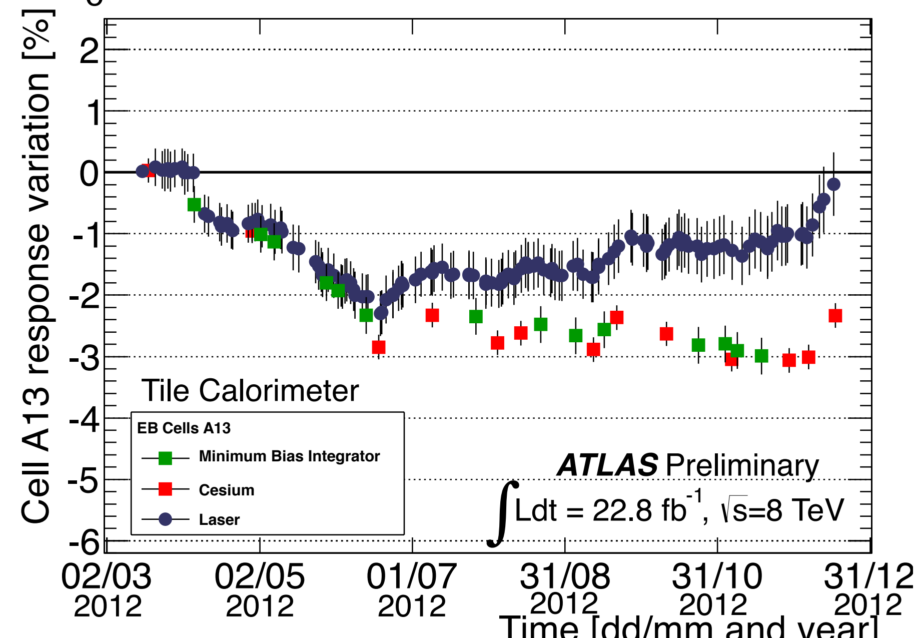
Response calibration in 2012

- Tile response was very stable, maximum drift was ~3.5% for A13 cell, inner most layer at |η|~1.3 in 2012 proton-proton run
  - Estimated ~50% PMT gain down-drift ~50% scintillator damage
- Up and down drifts follow data-taking and machine development periods
  - Recovery started after proton period ended
- Observed 2/3 of the total damage in 4 months after run start
  - Applied weekly calibration to PMT response

Drift in March-November 2012

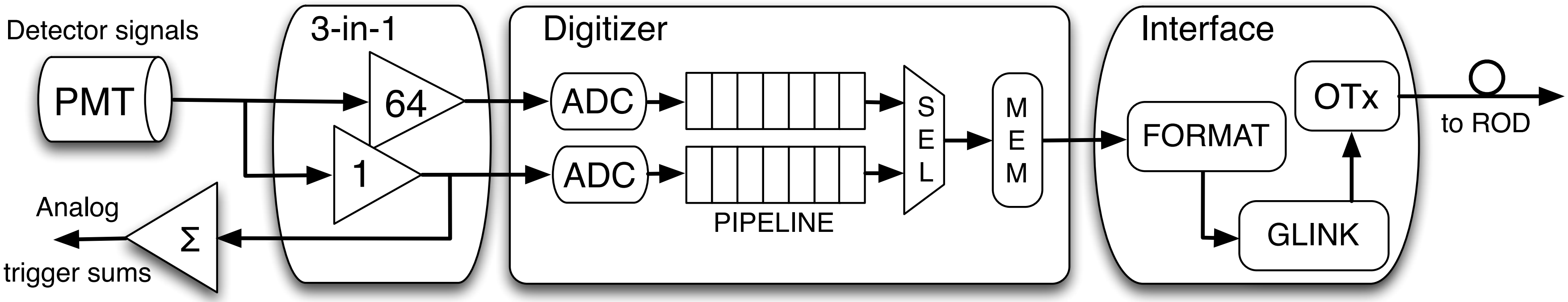




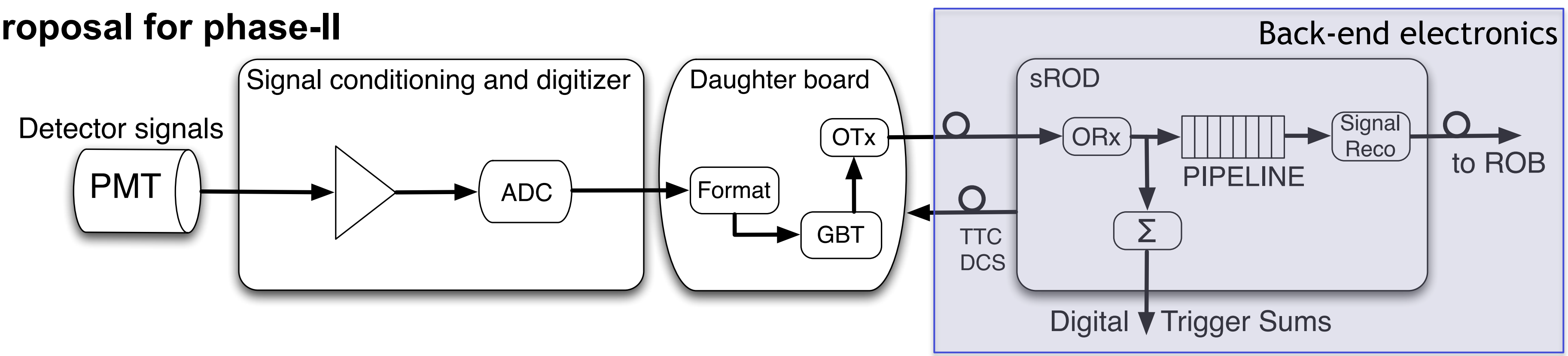


Strategy for phase-II upgrade

Present

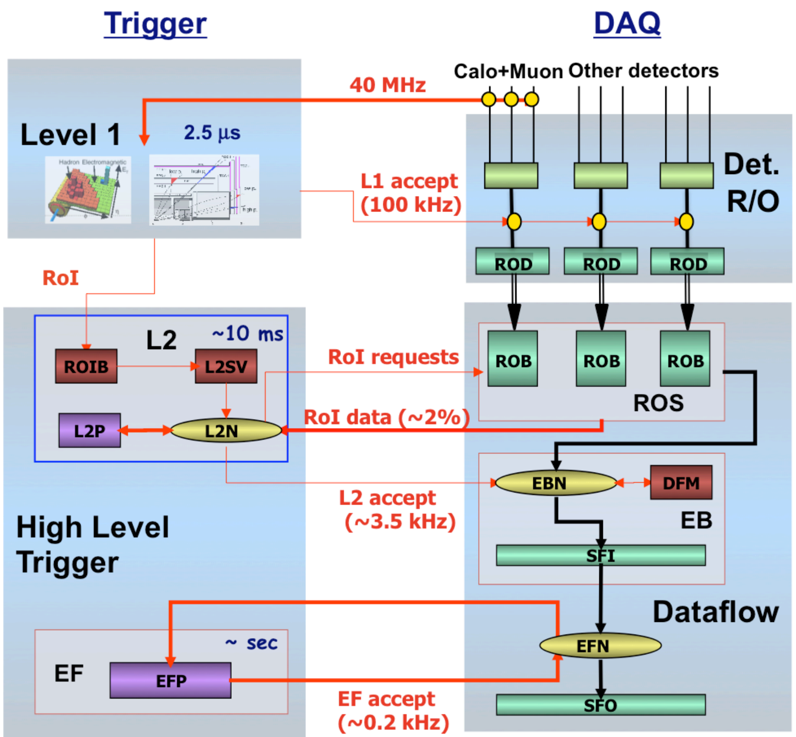


Proposal for phase-II

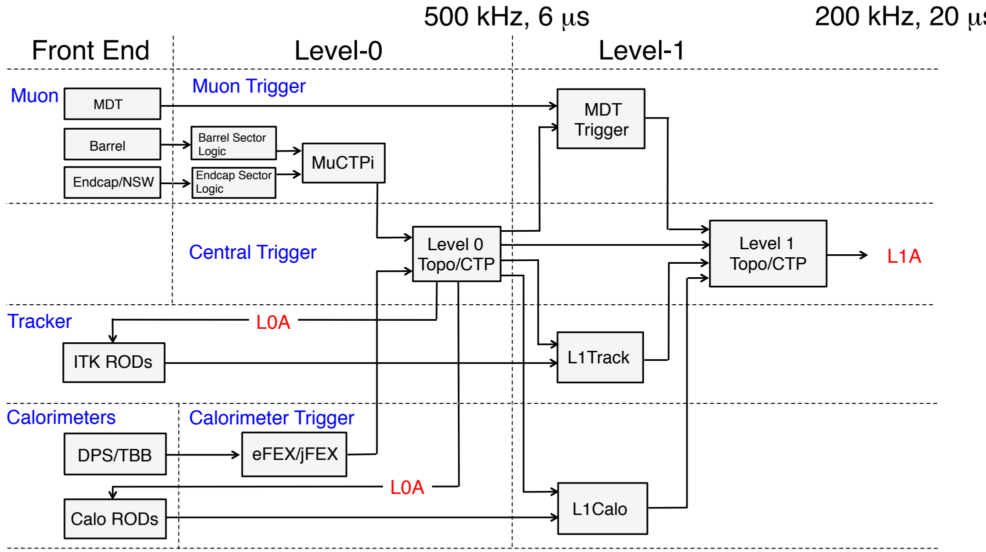


- Tile's plans for the upgrade phase-II of the LHC are to completely replace the front-end and back-end electronics introducing a new read-out strategy
  - Full digitization of signals at BC rate and transmission to off-detector electronics
  - Move pipelines to back-end electronics
  - Digital input to trigger Levels 0 and 1

Trigger upgrade for the HL-LHC

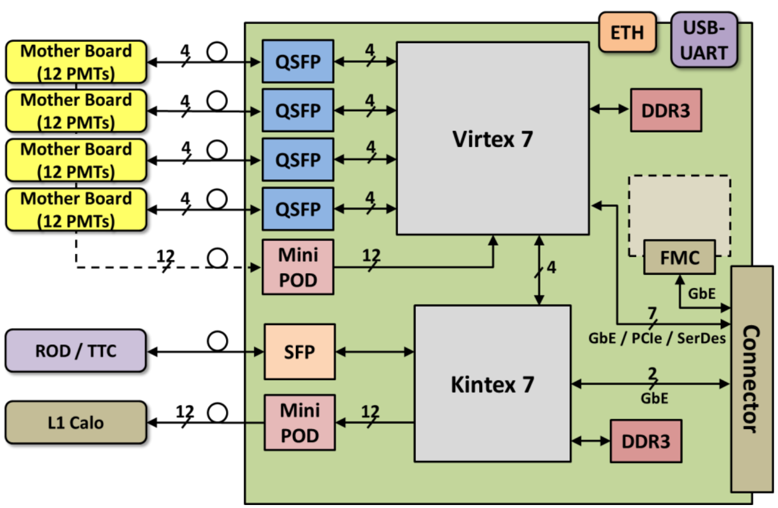


Block diagram of ATLAS TDAQ



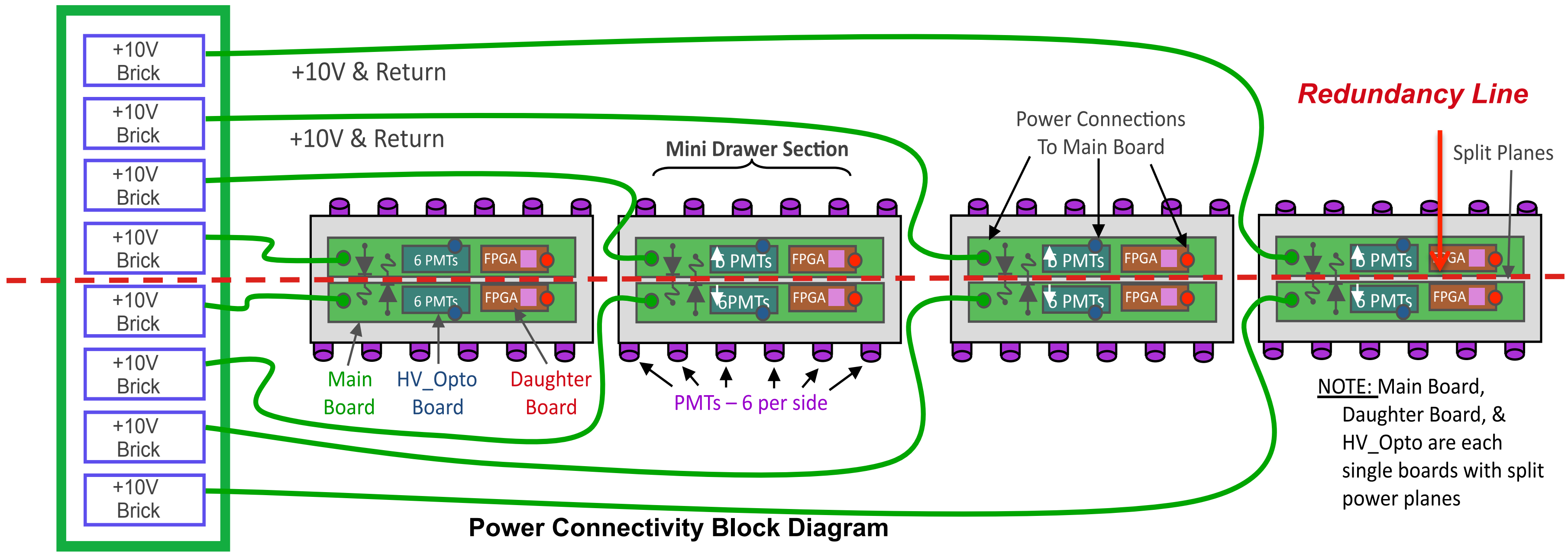
Block diagram of the Level-0/Level-1 hardware trigger

- LHeC should follow current tendency for phase-II upgrade of ATLAS
- Level 0 trigger with fully calibrated cell energies
  - As opposed to average calibration of analog trigger towers
- Development of high throughput read-out drivers to implement Level 0 and 1 pipelines
  - Implementing QSFP optical modulators



Conceptual design of ROD for the HL-LHC

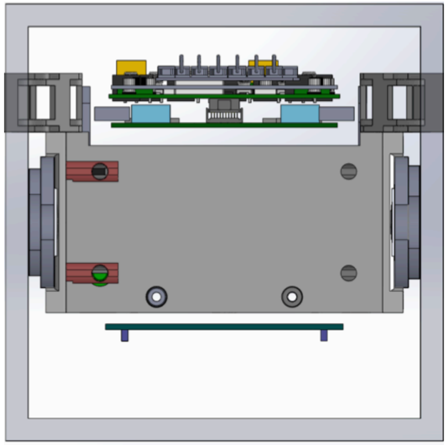
Redundancy in the electronics



Power Connectivity Block Diagram

- One of the lessons we have learnt from the electronics consolidation process in ATLAS during the LS1 is that we need to think the electronics to maximize the redundancy in case of failure, minimize the coverage damage in case of failure
- A double read-out for the cell should be accompanied by a redundant data path from the PMT up to the back-end electronics
  - Split the super-drawers into four independent mini-drawers
  - Split each mini-drawer into two independent halves (one cell read-out by one side)
  - Use redundant powering scheme

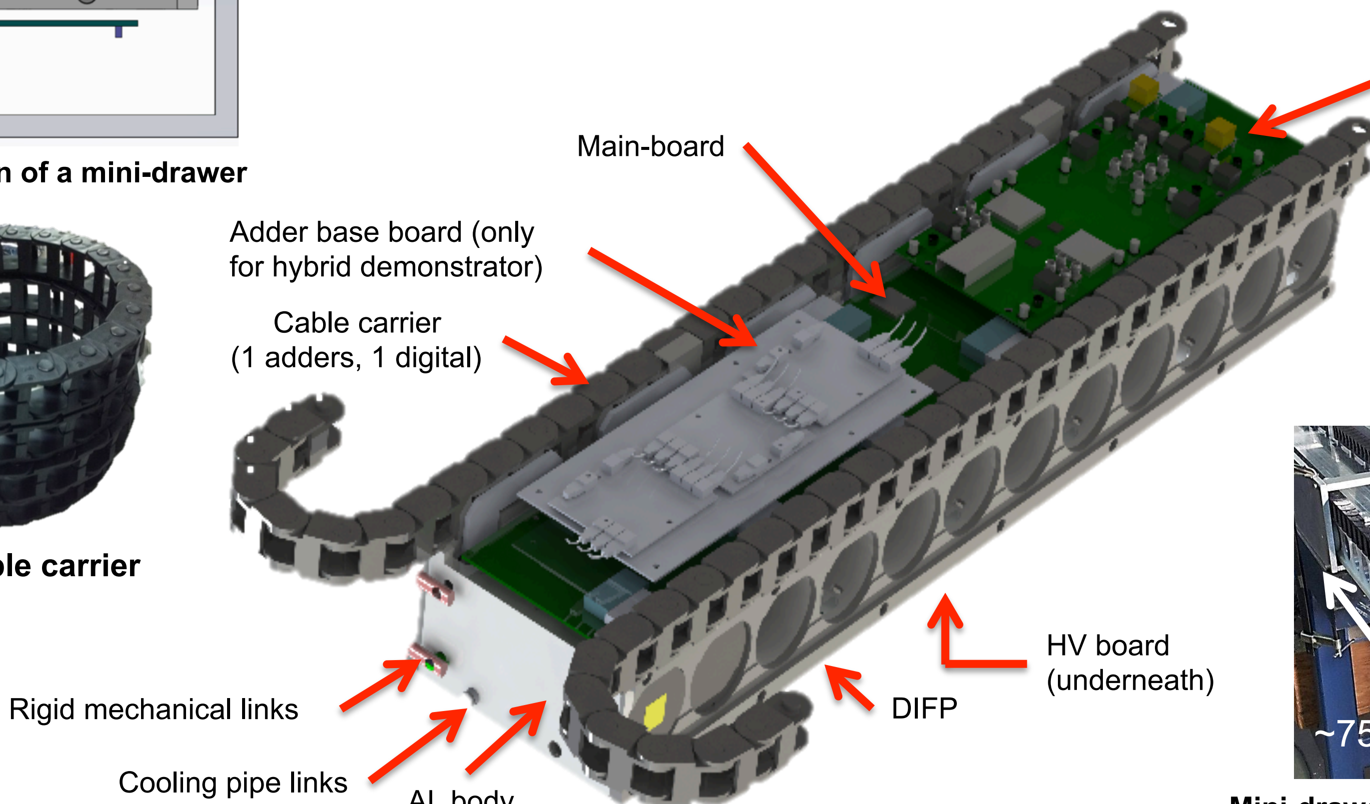
Mini-drawers in ATLAS

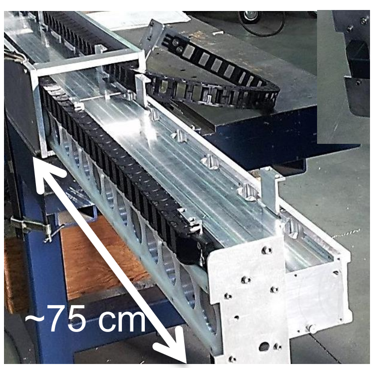


Cross section of a mini-drawer

Empty cable carrier

- Super-drawer demonstrator will be composed of 4 mini-drawers, each one containing
  - 12 front-end boards: 1 out of 3 different options
  - 1 main-board: for the corresponding FEB option
  - 1 daughter-board: single design
  - 1 HV regulation board: 1 out of 2 different options
  - 1 adder base board + 3 adder cards: for hybrid demonstrator





Mini-drawer with cable carriers

Conclusions

- A tile calorimeter has been proposed for the LHeC detector
- It's good performance in ATLAS during Run 1 makes it a good candidate for the baseline option

- Preliminary resolution studies show compatibility with ATLAS
- Studies need to continue to evaluate ways of increasing the resolution

- We should pursue and increase in the granularity in cell segmentation, redundancy in read-out electronics and modularity in overall design

Backup

A project 20 years old

P. Jenni – Expression of interest – EAGLE collaboration
General Meeting on LHC Physics and Detectors
Evian-les-Bains, France, 5 - 8 Mar ***1992***

Scintillator tile hadron calorimeter conceptual design

Novel concept for a simple and economic hadronic scintillator calorimeter with Fe absorber and possibly integrated magnetic field return

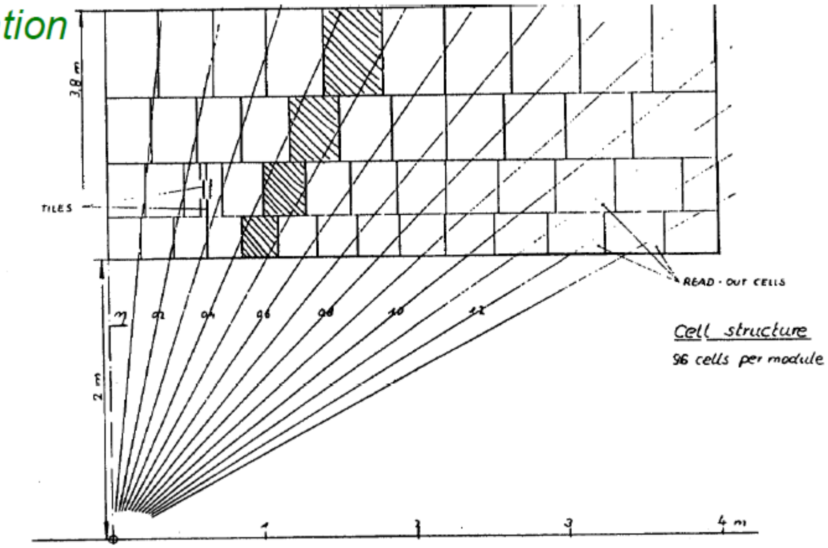
Vertical scintillator plates (w.r.t. barrel axis) read out with straight wave length shifting fibers at two edges (light collection experimentally checked)

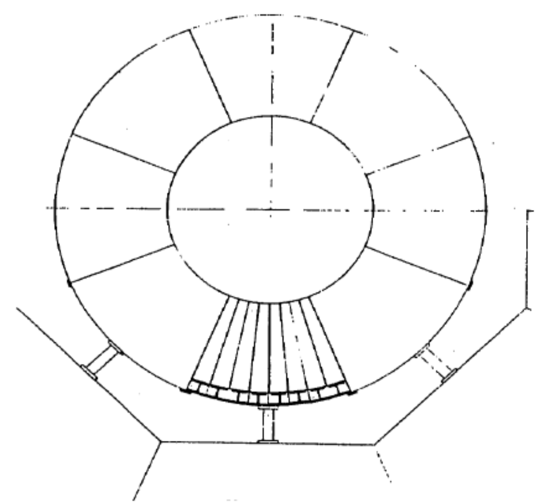
Granularity $\Delta\eta \times \Delta\phi \sim 0.1 \times 0.1$ with 4 longitudinal samples, 15000 channels total

η-projectivity by grouping WLS readout fibers of the longitudinal samples to form approximatively pointing towers

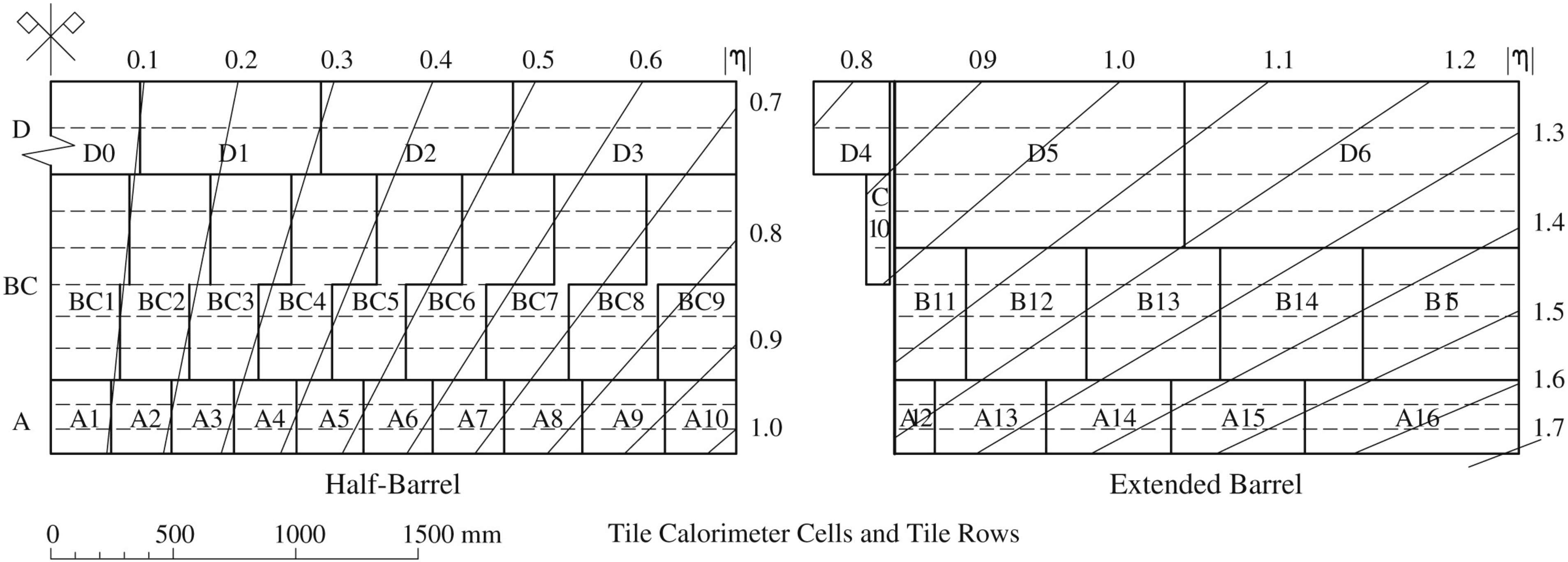
Expected jet resolution (MC simulation assuming a 25 X_0 Pb - LAr EM calorimeter in front)

$$\sigma(E)/E = 41\%/E + 2\%$$



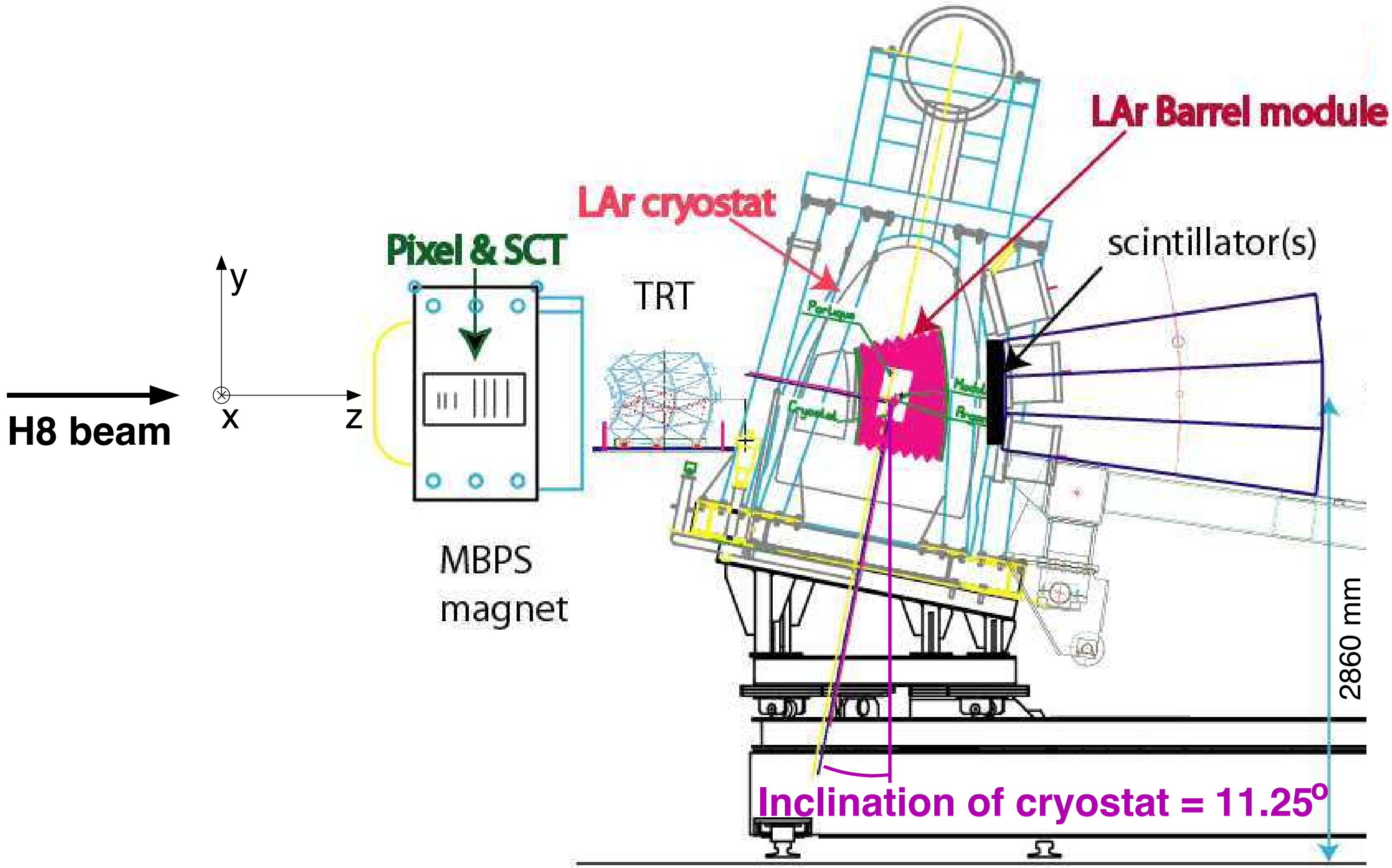


Tile cells and scintillator rows

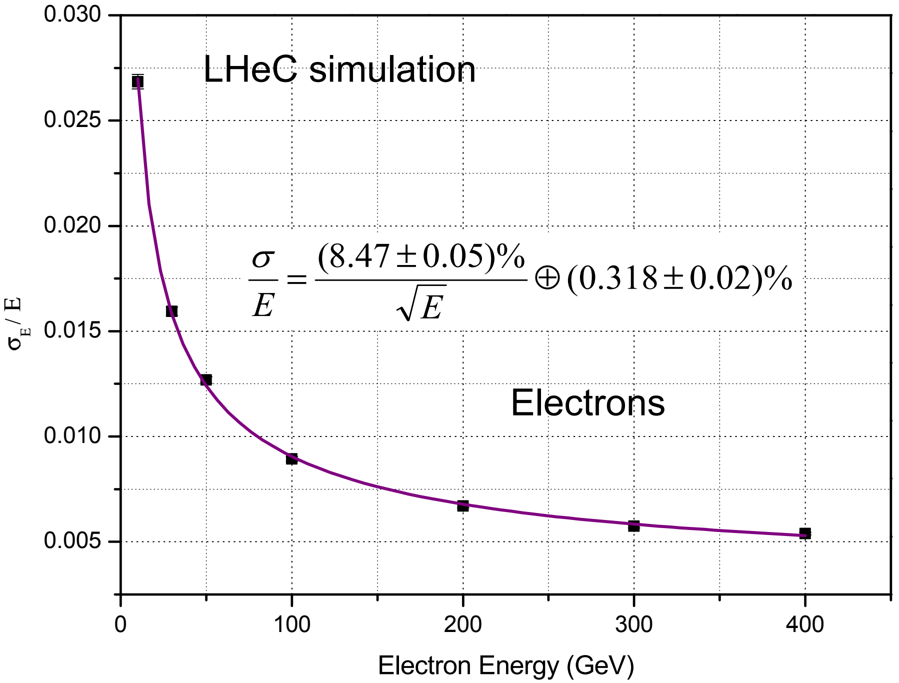


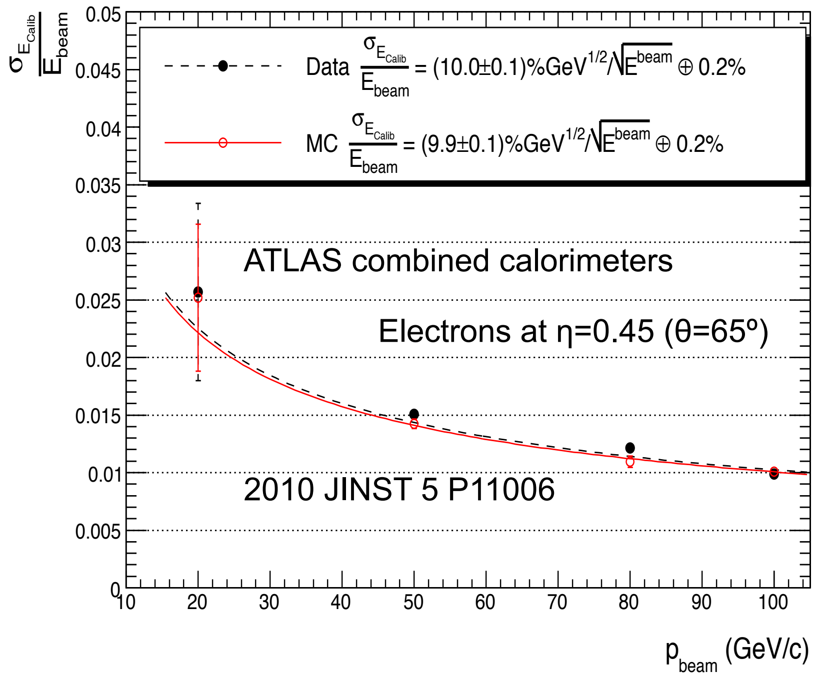
Tile Calorimeter Cells and Tile Rows

Combined test beam setup

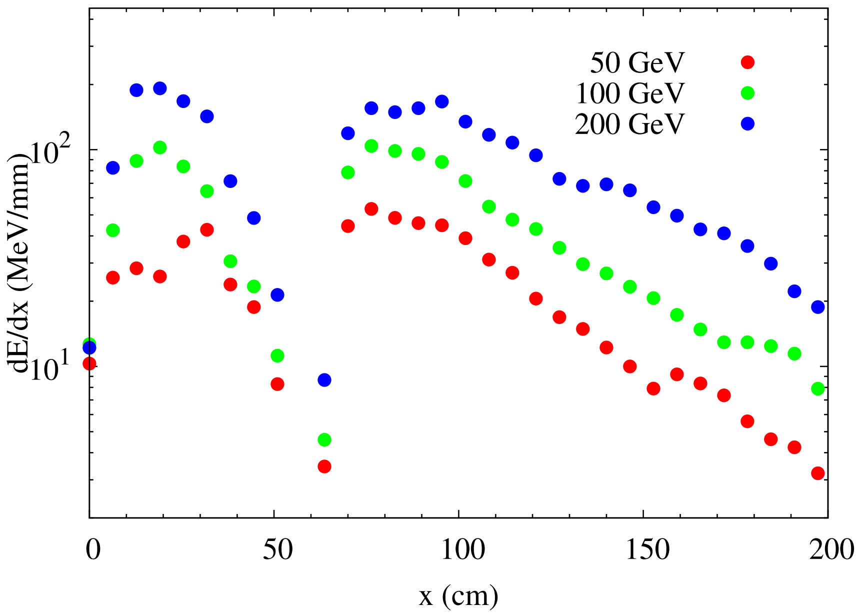


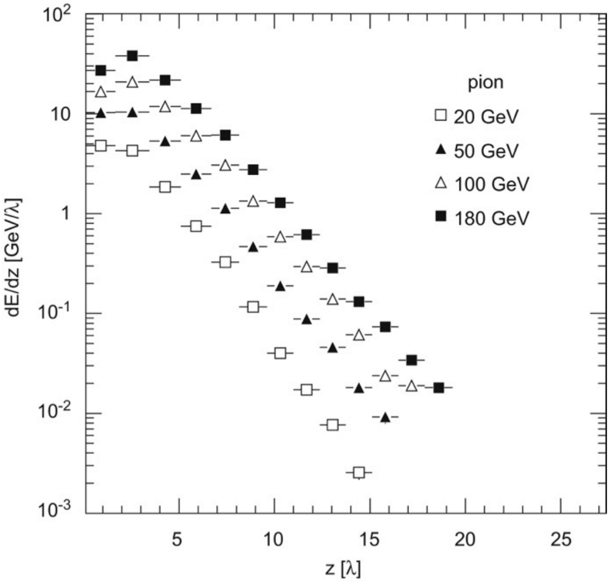
Combined calorimeter resolution

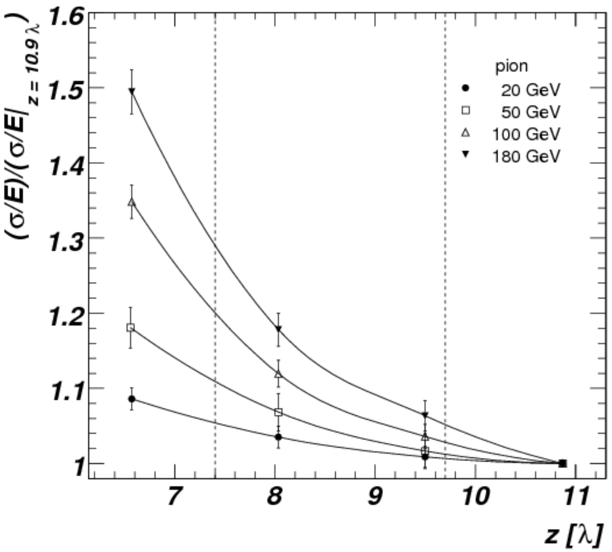




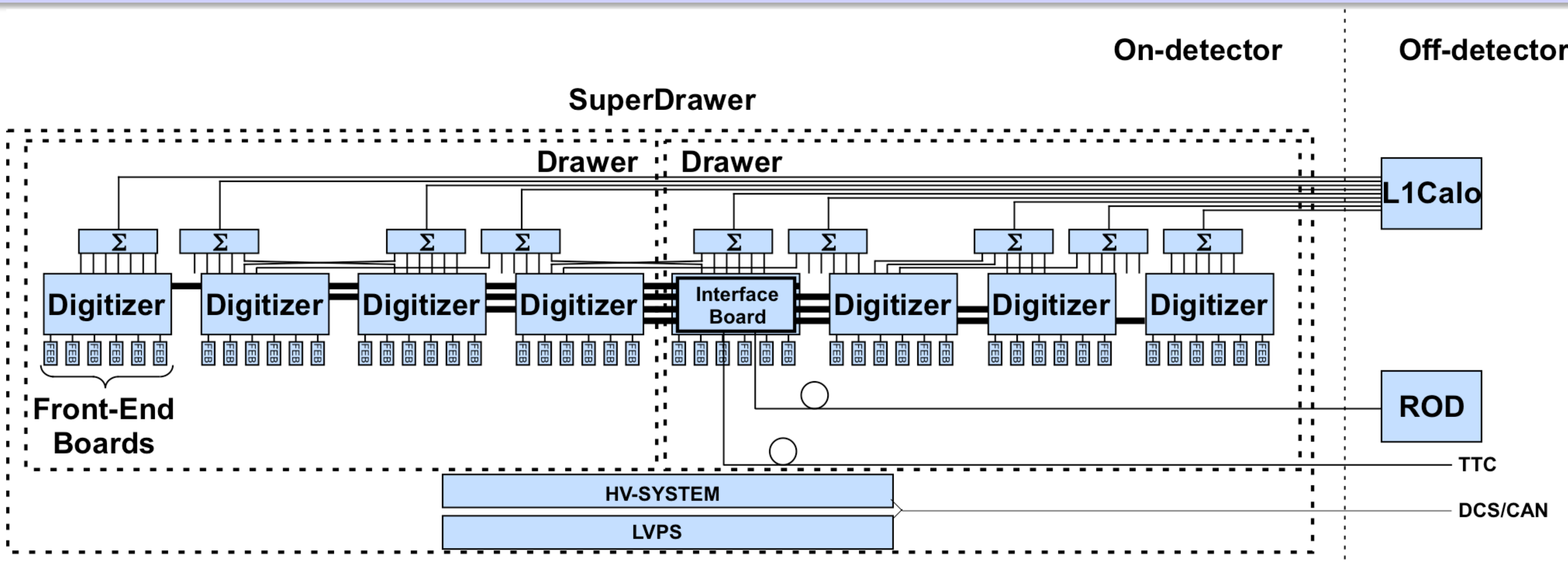
Longitudinal shower profile





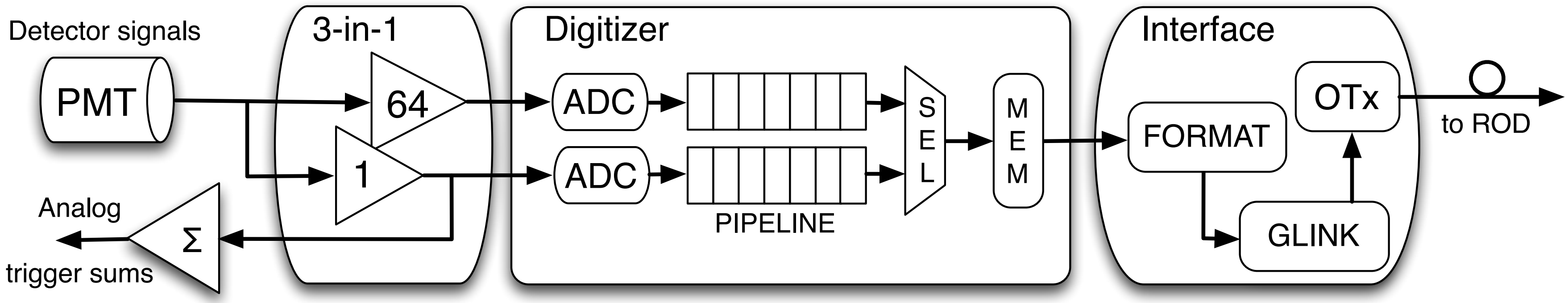


Tile front-end electronics



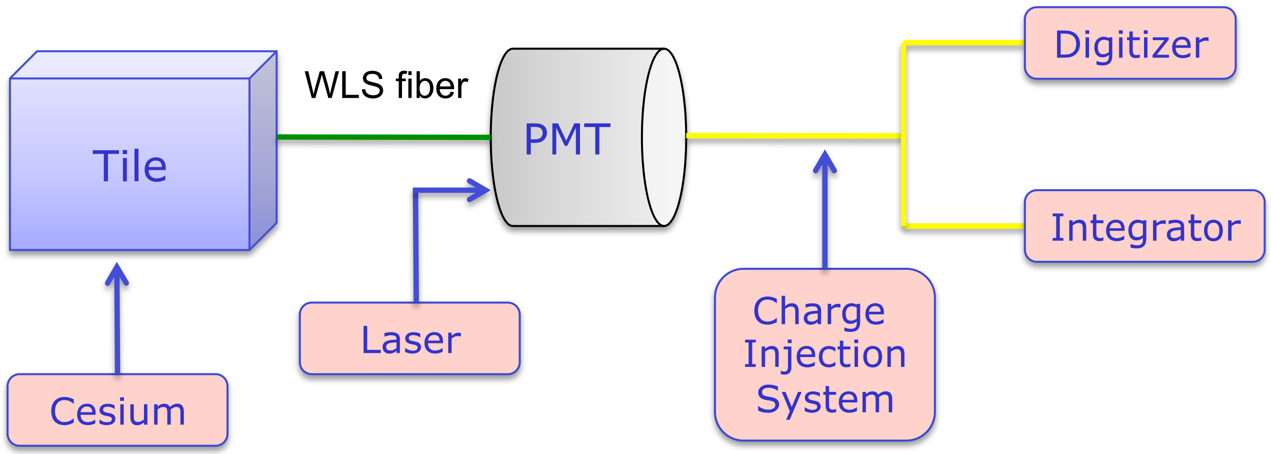
- Each PMT is connected to a 3-in-1 card
- Six PMT blocks are connected to one digitizer board
- Eight digitizers read-out a complete super-drawer
- One interface card is needed to read-out one super-drawer

Tile read-out



- The analog pulses from the PMTs undergo shaping and amplification in the 3-in-1 cards in two gains (low and high) with a ratio of 1:64. Low gain signals which are summed in groups by adder boards are provided to the Level 1 Calorimeter Trigger. The analog pulses are received by digitizer boards where the signal is converted into digital samples every 25 ns, which are stored in the front-end pipeline memories, the so called Data Management Units (DMU). Upon Level 1 accept, an event-frame-selector selects high gain samples unless the highest sample is saturated in which case the low gain samples are used and stores them in a buffer. Event frames are pulled from the DMUs by the Interface card which formats the data and transfers the frames to the off-detector Read-Out Drivers (RODs).

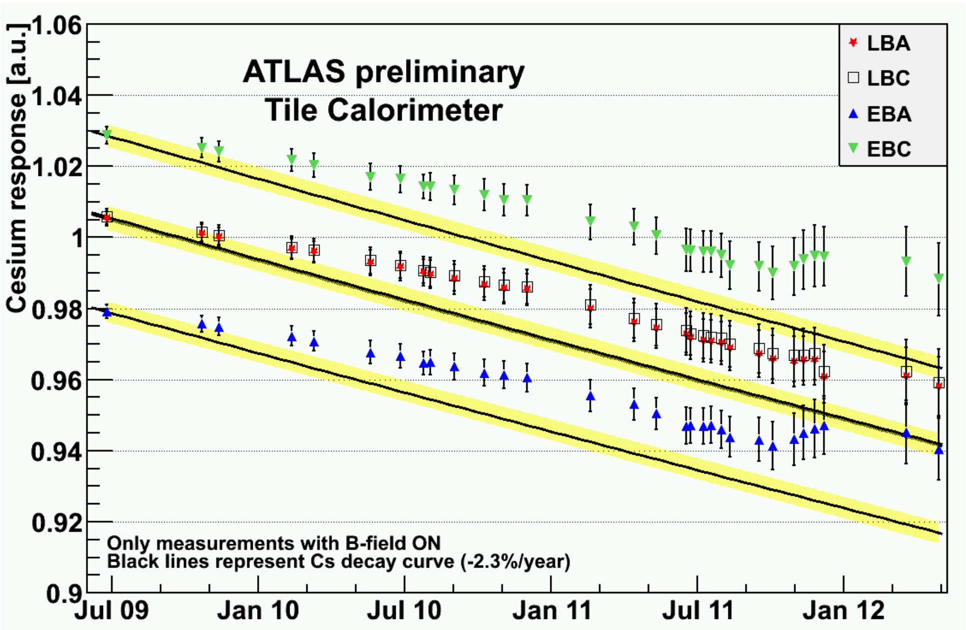
Calibration systems

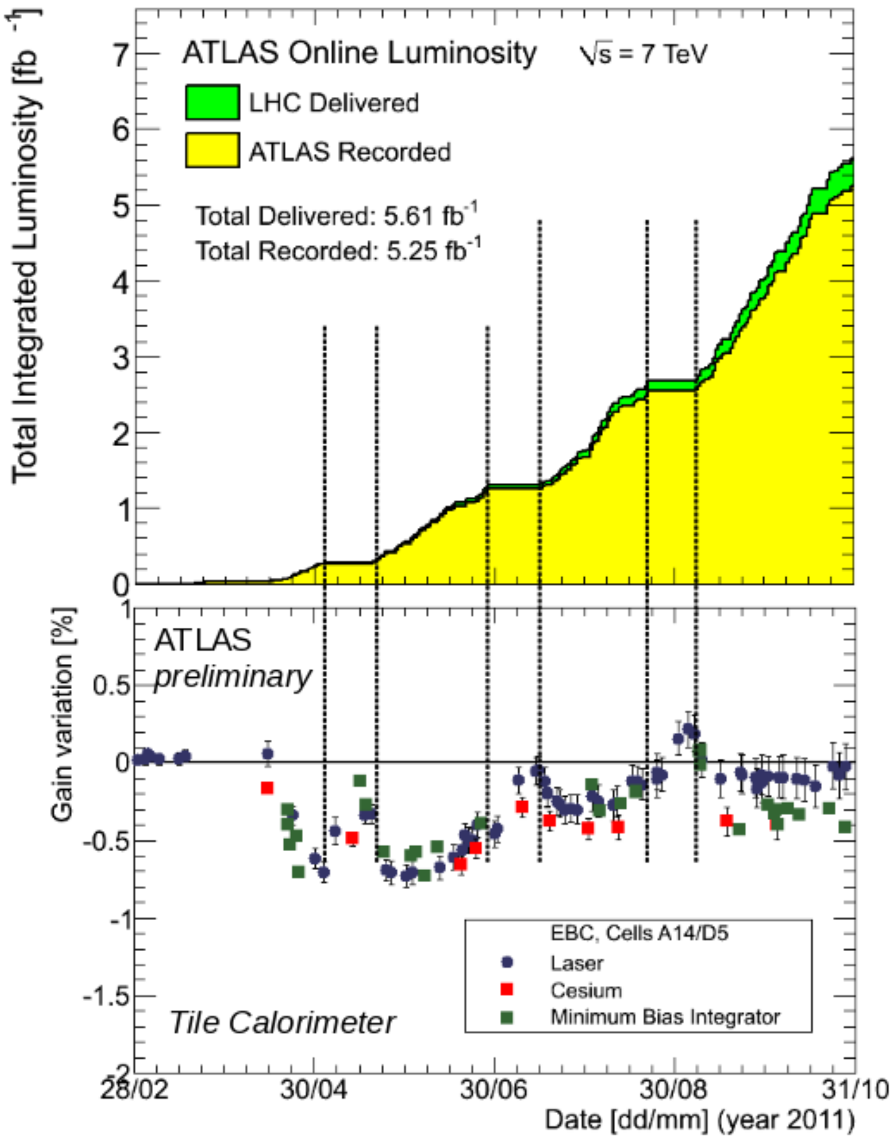


- Cesium system: scan with a ^{137}Cs source ~1-2/month
- Laser system: correction relative to last Cs scan ~2/week
- CIS: Measurement of the ADC to pC constant ~2/week

Response calibration in 2011

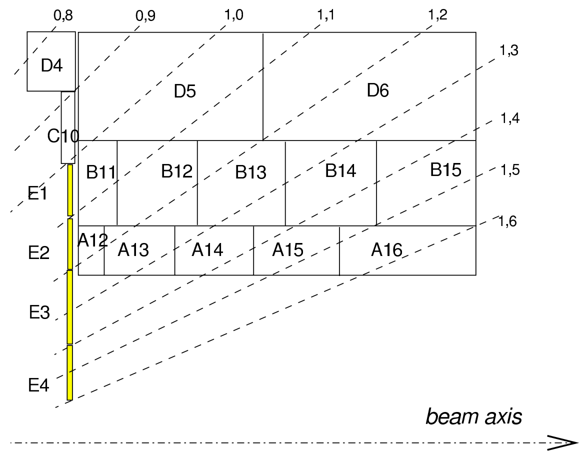
- 2010: up drift of Cs response (~1%)
- 2011: Up/Down drift oscillation (<1%) during beam/no beam periods
  - Consistent behaviour seen by all three calibration systems
  - Drift dominated by PMT gain effects
  - Corrections applied to the PMT response to compensate this effect

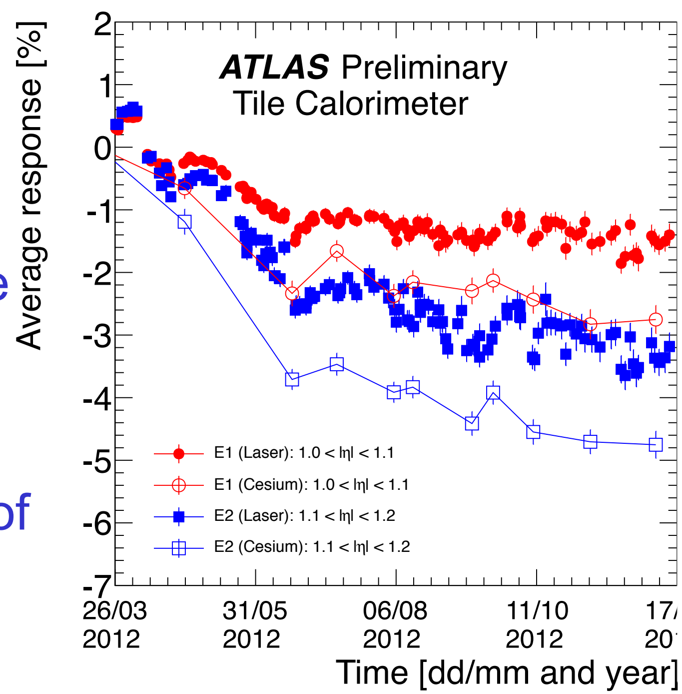


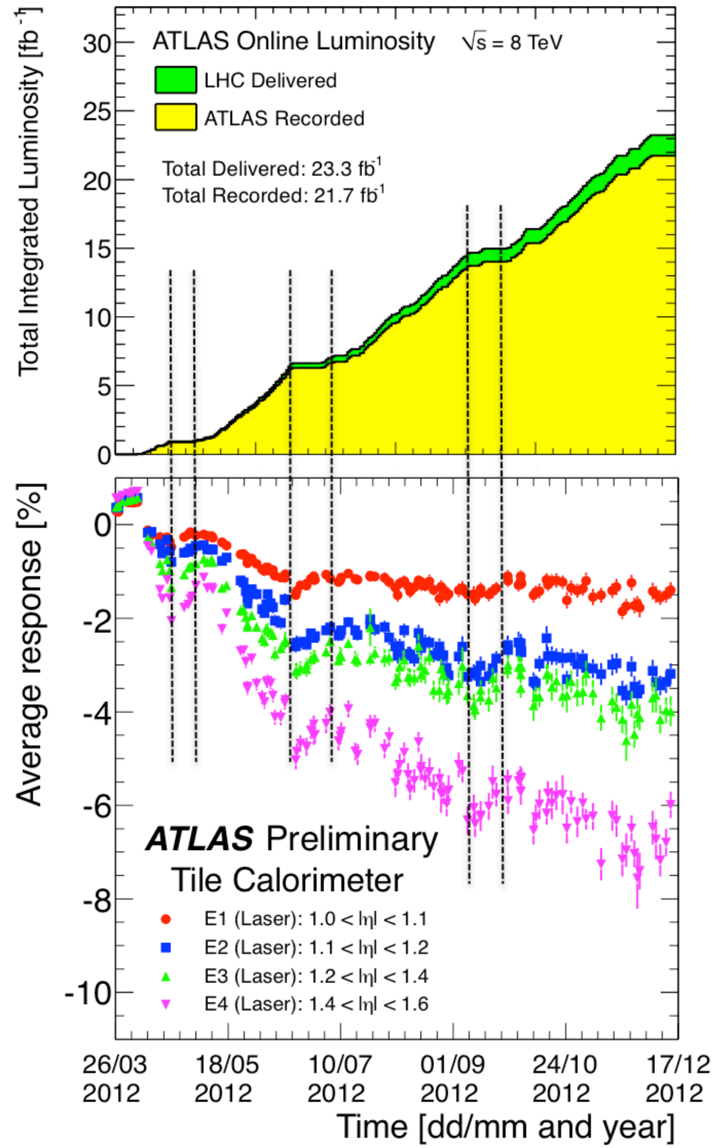


Most irradiated cells

- Crack scintillators (E cells), located in 1.0 < eta < 1.6 are the most irradiated cells in Tile
- Up to 6% down-drift was observed for E4 cell with Laser calibration
  - E3 and E4 cells don't have Cs calibration
- In E1 cells, ~50% down-drift was due to PMT drift
- In E2 cells, PMT drift was responsible for ¾ of the gain variation

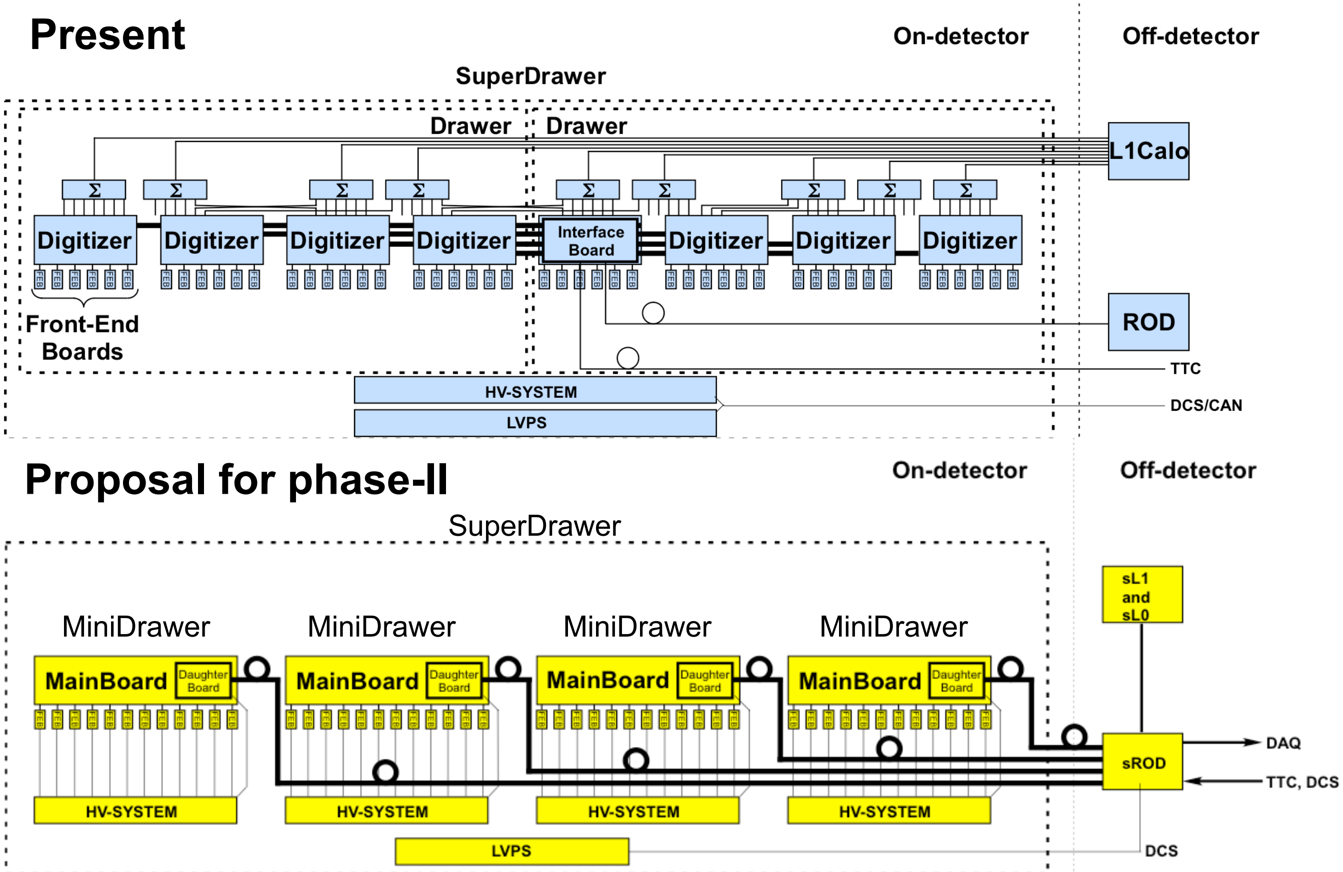




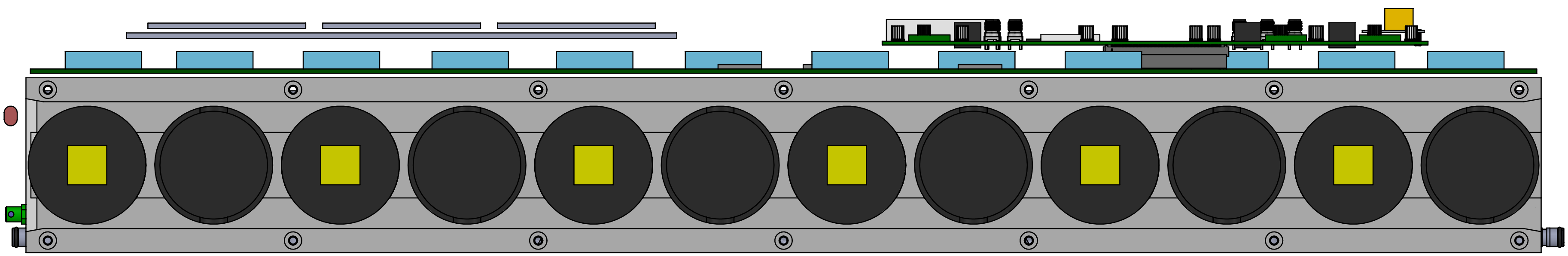


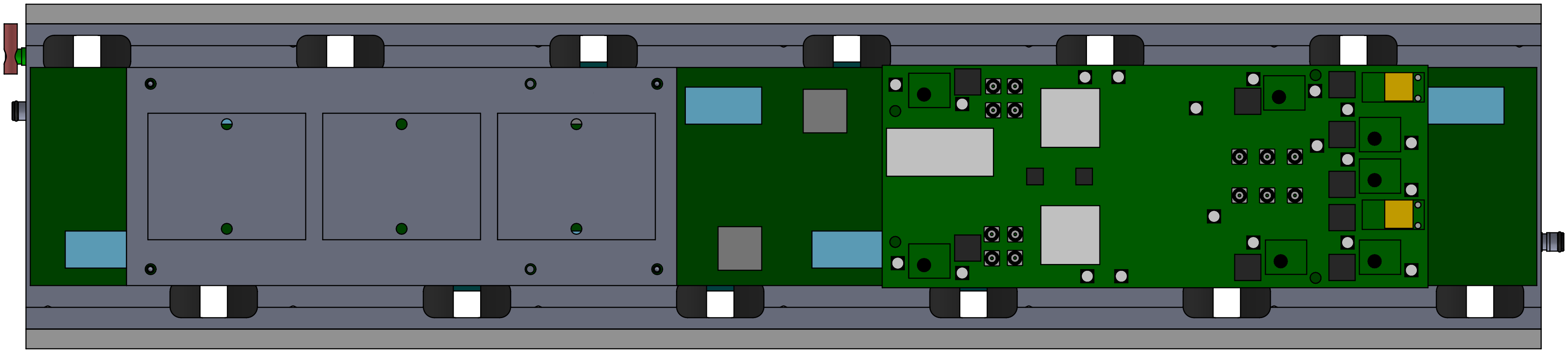
Changes in the front-end

- Aim to cope with luminosity increase and reduce single point failures (improve reliability)
  - **Fewer failure-prone connectors** in the new system, but also the challenge of routing **more fiber optic and LV cables**. Moving from dependent drawers to independent mini-drawers
  - **Increase the redundancy in the read-out path** from the cell to the backend
  - Similar **redundancy in the power distribution** and introduction of Point-Of-Load regulators



Mini-drawer drawing



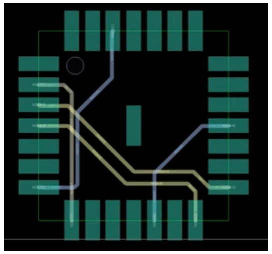


Choice of optical links

- Directly modulated lasers (including VCSELs)
  - Have been qualified at ~10 Gb/s per link with a Bit Error Rate (BER) ~10^{-12}
  - Increasing bandwidth increases problems
  - Commercial VCSEL arrays (SNAP12) have shown Single Event Upset (SEU) at ~10^{10} p/cm^2
  - Also these use Multi Mode fibers which are more expensive
- A commercial off-the-shelf solution exists that uses single mode fibers at high transfer rates from Molex using Silicon Photonics technology developed by Luxtera (QSFP Active Optical Cable)
  - Can operate above 40 Gb/s (4x10) with BER < 10^{-18}
  - Made out of 130 nm Silicon On Insulator CMOS which should be very radiation hard
  - Radiation tests showed no SEU at TID of 165 kRad and fluence of 8x10^{11} p/cm^2
  - Problem is the PIC microcontroller used for configuration and monitoring survives ~20 kRad
  - A PIC replacement board has been designed, and control done from FPGA
  - Firmware to initialize the electro-optical chip has been developed
  - Several anti-fuse FPGAs are being evaluated and will be tested for radiation tolerance
- QSFPs are the preferred option for the demonstrator
  - Having less fibers vs lower clock frequency

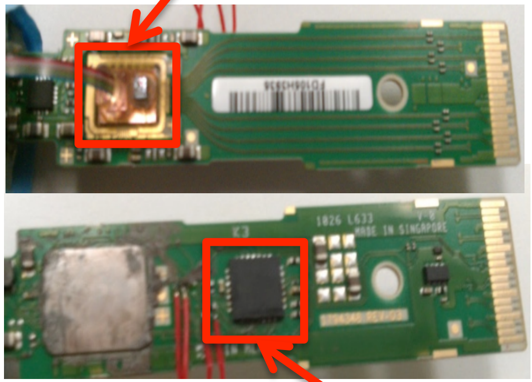
10^{-12} BER = ~900 errors per day

10^{-18} BER = 1 error in ~1000 days



PIC Replacement Board

Modulator



PIC Microcontroller

Per Super-Drawer: