TRIUMF

Hyper-K Electronics; Overview and Canadian Plans

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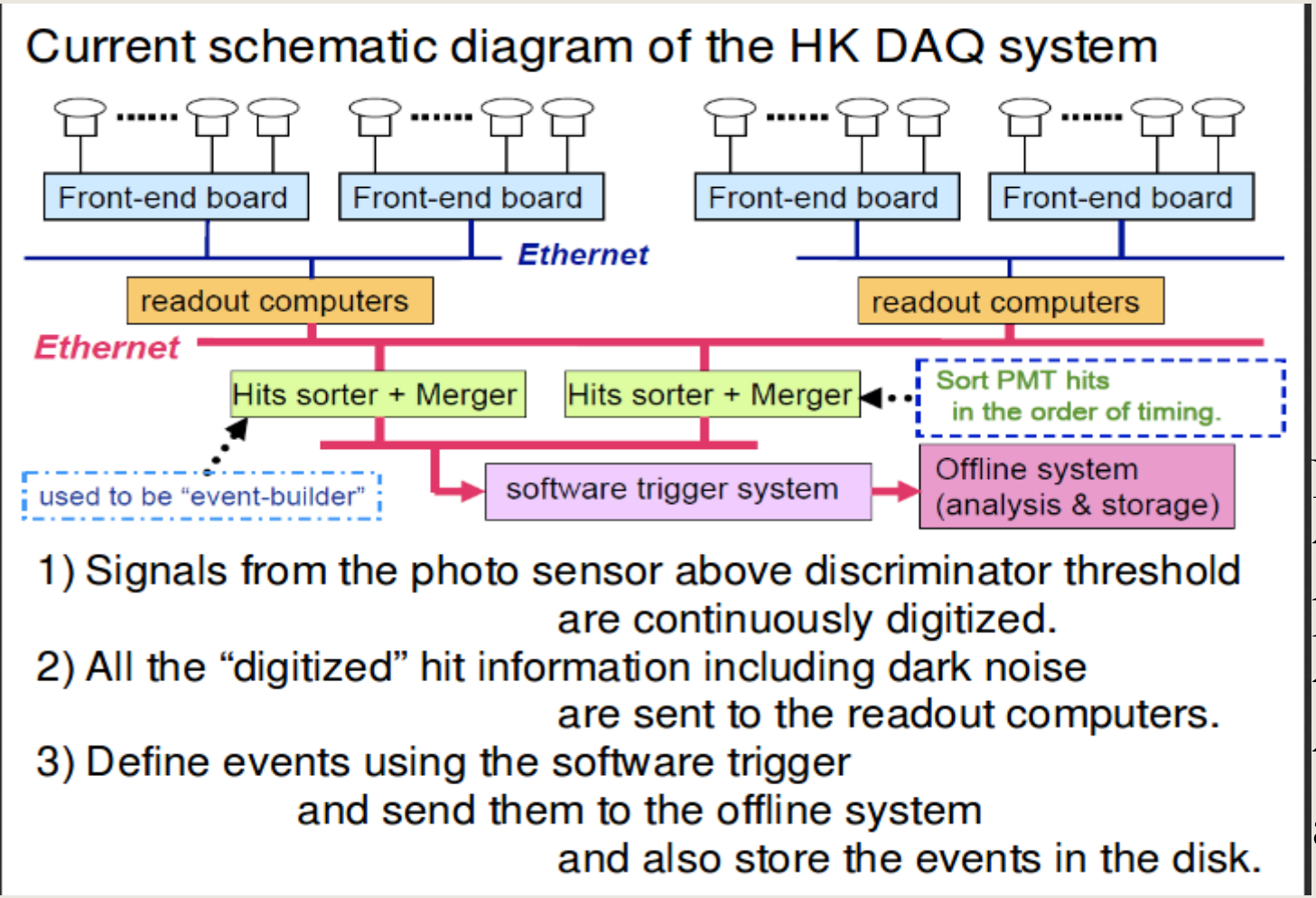
HK-EU Meeting, Dec 2013

Overview

- Reminder of baseline HK electronics/DAQ plan
- Canadian electronics/DAQ interests
  - FADC digitization
  - Communcation
- Current work
- Plans for 1kton

Much of the content is just stolen slides from Hayato-san and Fabrice (not an official summary)

Hyper-K Electronics/DAQ

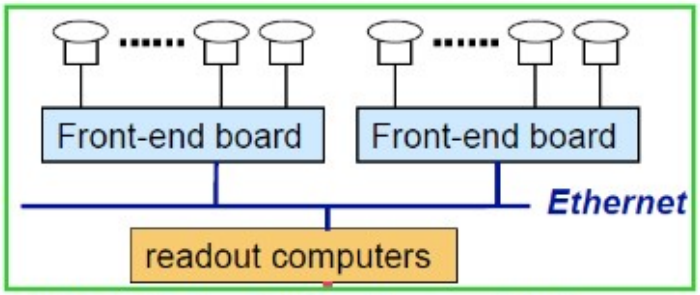


No global hardwar
triggers; all PMT
hits stream up
to PCs where
trigger decisions
are made.

Hayato-san

Hyper-K Communication Scheme

Possible front-end electronics module connections

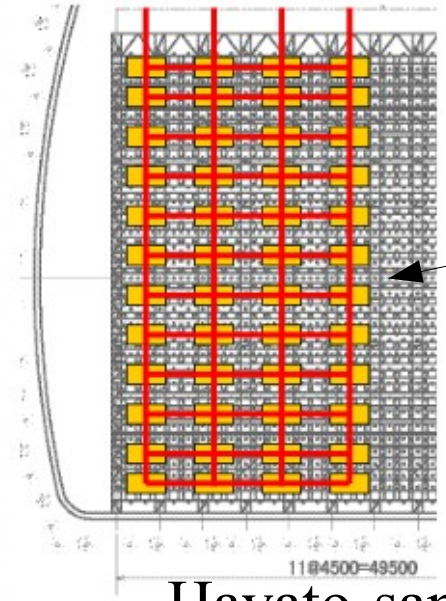


~ Design of the data flow

1) Assuming to use 1GbE

- Robustness
- Power consumption

HK detector Side view



2) Connect neighboring Front-end boards each other

- Reduce total length of the cables
- Avoid single point failure

Usually, data collected by a module are transferred to the upper module (vertically)

If a module failed, transfer data to the other module instead of the failed module (horizontally).

Data rate at the top modules has to be enough smaller than 1Gb/sec.

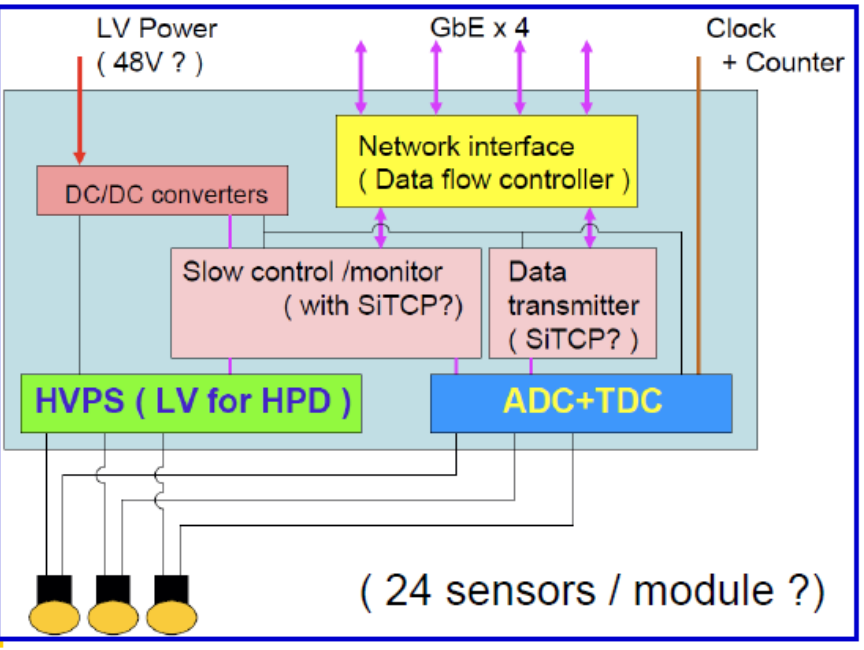
Hayato-san

Electronics sit in water! Redundant communication needed.

HyperK: Baseline Front-end Digitization

- Baseline signal digitization: TDC + ADC (like SK).
- One potential concern: the TDCs used for SK electronics are no longer available; need to find new ones.
  - A possible Fermilab chip being investigated.

Schematic diagram of the front-end board



QTC/ADC specification (performance)
(current performance = minimum requirements)

• **Built-in Discriminator**	¼ p.e. (~ 0.3 mV)
• **Processing Speed**	~ 1usec/HIT
• **Charge Resolution**	~ 0.05 p.e. RMS (< 5 p.e.)
• **Charge Dynamic Range**	0.2~2500pC (0.1 ~ 1250 p.e.)
• **Timing Respons**	0.3ns RMS (@ 1p.e.) 0.2ns RMS (> 5p.e.)

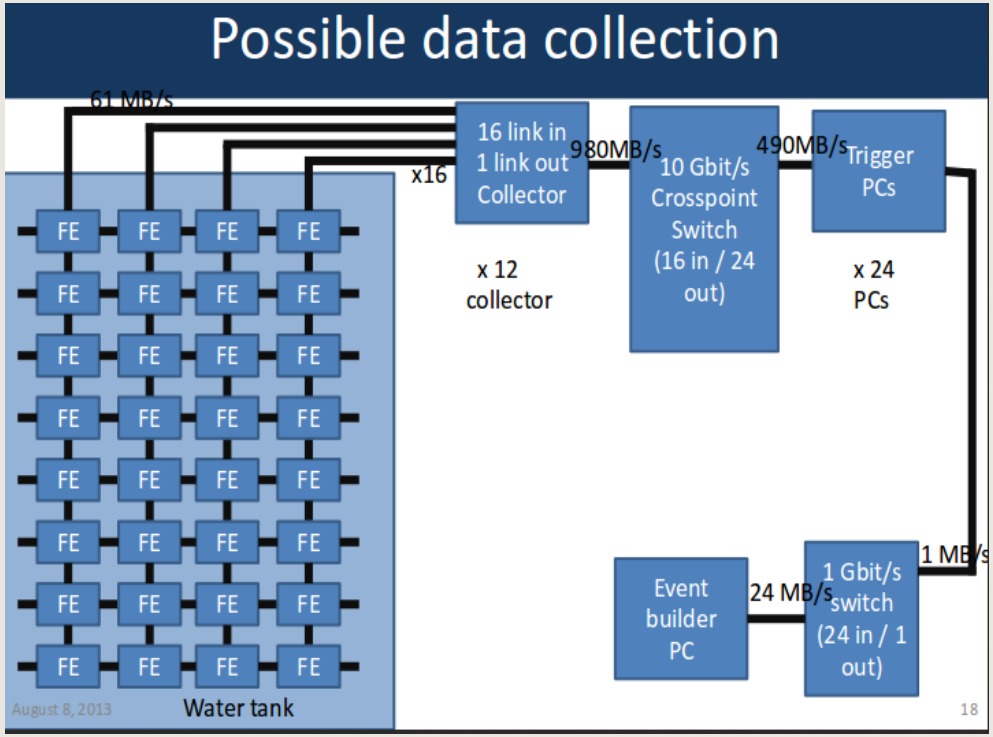
TDC specification (performance)

• **Least Time Count**	0.52 ns
• **Time resolution**	250ps
• **Dynamic range**	≥15bits
• **Continuous running mode**	

Baseline specifications

Back-end Architecture

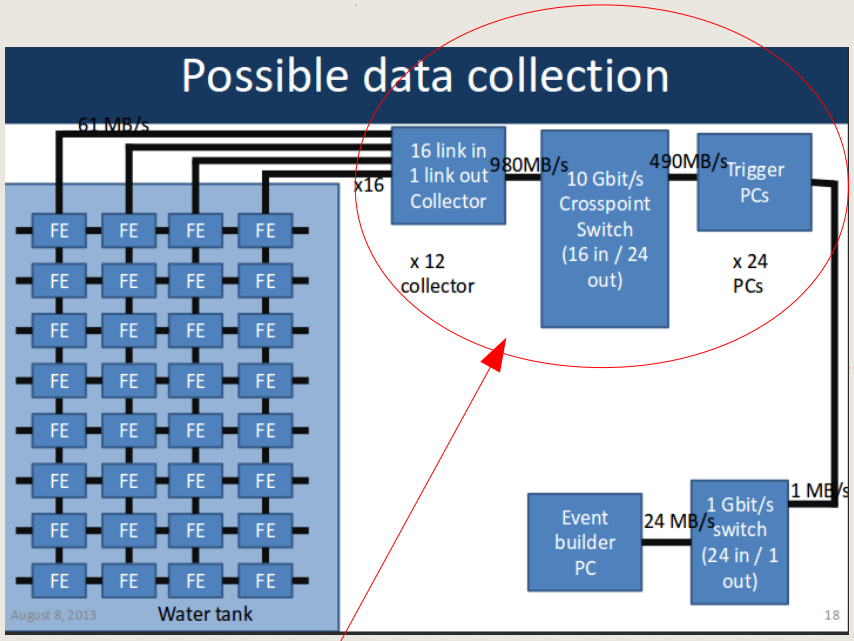
- Fabrice picture for possible back-end architecture.
- Data from front-end electronics get time-sliced and sent to different PCs.
- PCs make trigger decisions and decide if event(s) get logged to disk.



Back-end Data rates

- Maximum 12GB/s for rate.
  - This dominated by the rate for the dark noise:

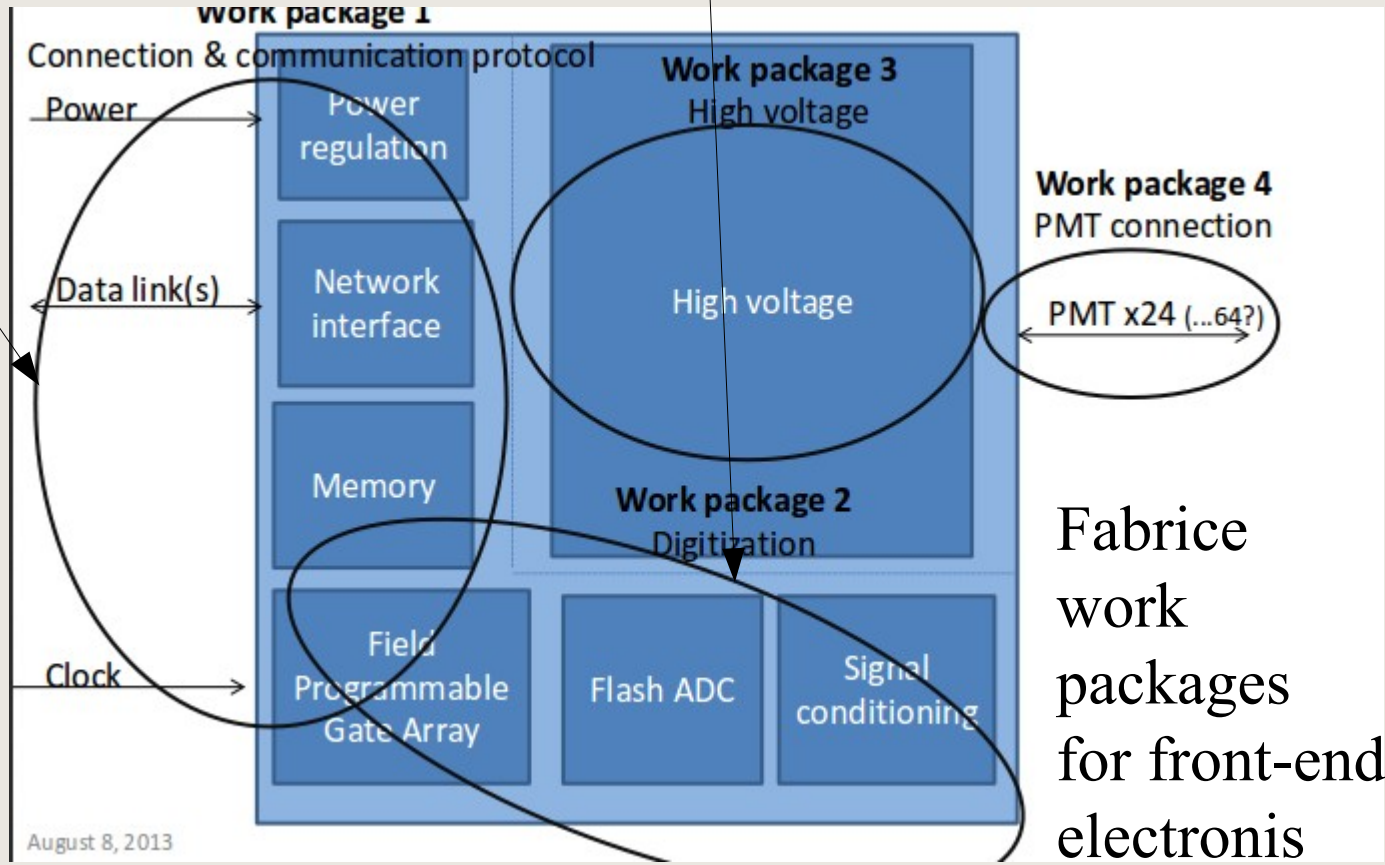
    10 kHz dark rate * 100k channel * 12 bytes per hit
  - But that is without compartmentilization; rate could be lower, near 1GB/s from a compartment.



- Details of backend architecture depend on these details quite strongly.

Canadian Front-end Electronics Interests

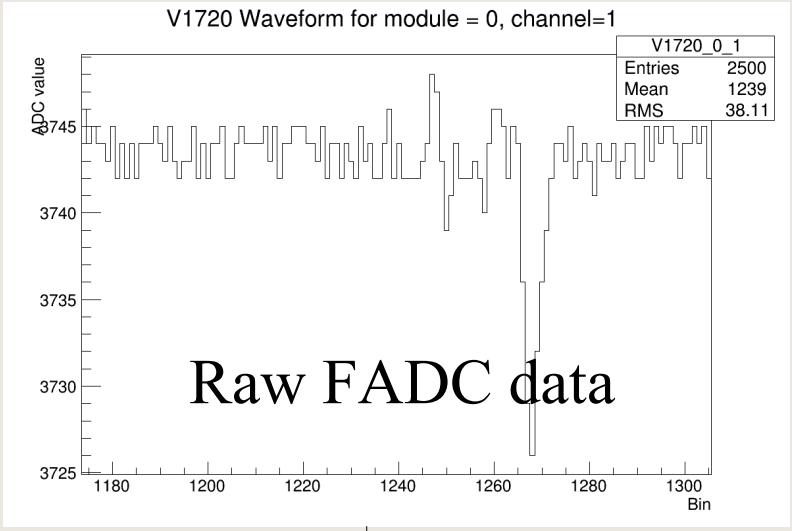
- FADCs instead of TDC/ADC for digitization
- Redundant communication protocol



Fabrice work packages for front-end electronis

FADC Option - Overview

- Proposal is to use FADC (Flash ADC).
  - Something like 125-500 MHz sampling, 12-16 bit resolution.
- FADC data is continuously processed using FPGA on front-end board; only send pulse summary to backend.
  - Pulse summary is either just Q/T (for small pulses) or a set of ADC samples (for large pulses).



Process with onboard FPGA

Pulse charge/time -> backend

FADC Option – Overview II

- Have experience with this digitization from DEAP (dark matter) and GRIFFIN (nuclear physics).
  - Also with FPGA processing for T2K-FGD.

Pros

- Deadtime-less
- More information on multiple pulses in 1us after first pulse.
  - Ie, distinguish direct/reflected light.

Cons:

- Higher power (?) and cost
- More complex: pulse processing in firmware.
- Can we meet timing resolution + dynamic range requirements?

FADC Option - Overview

Current work is focused on these two questions:
1) Can we quantify gains of FADC? What physics does this help?
-> decay electron tagging?
-> neutron tagging?
2) Can we meet timing resolution, dynamic range requirements?

Pros

- Dead-time less
- More information on multiple pulses in 1us after first pulse.
  - Ie, distinguish direct/reflected light.

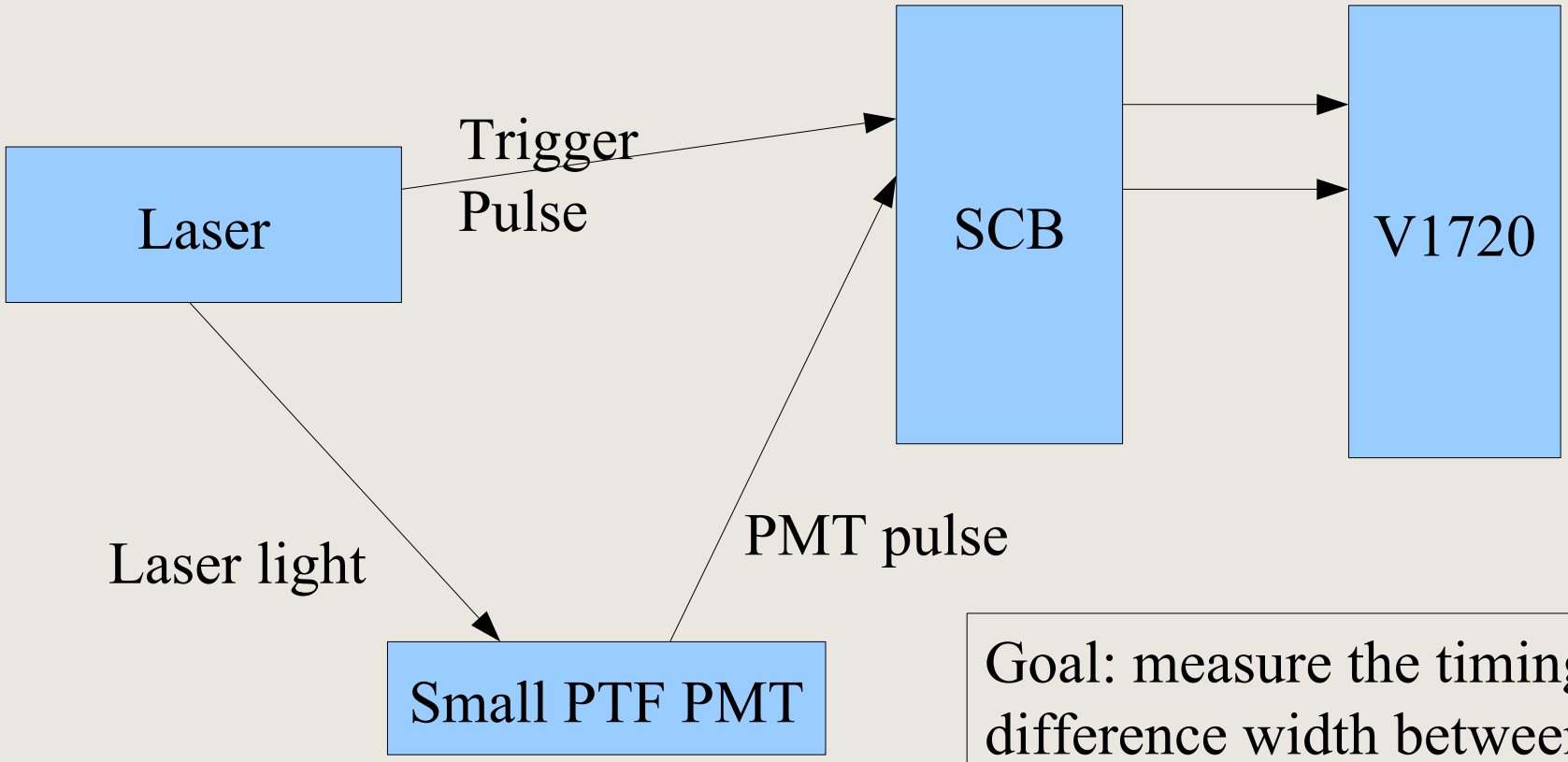
Cons:

- Higher power (?) and cost
- More complex: pulse processing in firmware.
- Can we meet timing resolution + dynamic range requirements?

FADC Test with DEAP Electronics

- Did quick test of FADC timing resolution using DEAP electronics setup at TRIUMF.
- DEAP using CAEN V1720 to digitize PMT signals.
- V1720 is a 12-bit, 250 MHz FADC.
- DEAP PMT signals are put through a custom Signal Conditioning Board (SCB) to shape the pulse V1720.
- Not proposing using this CAEN module for HK, but the technology would be similar..

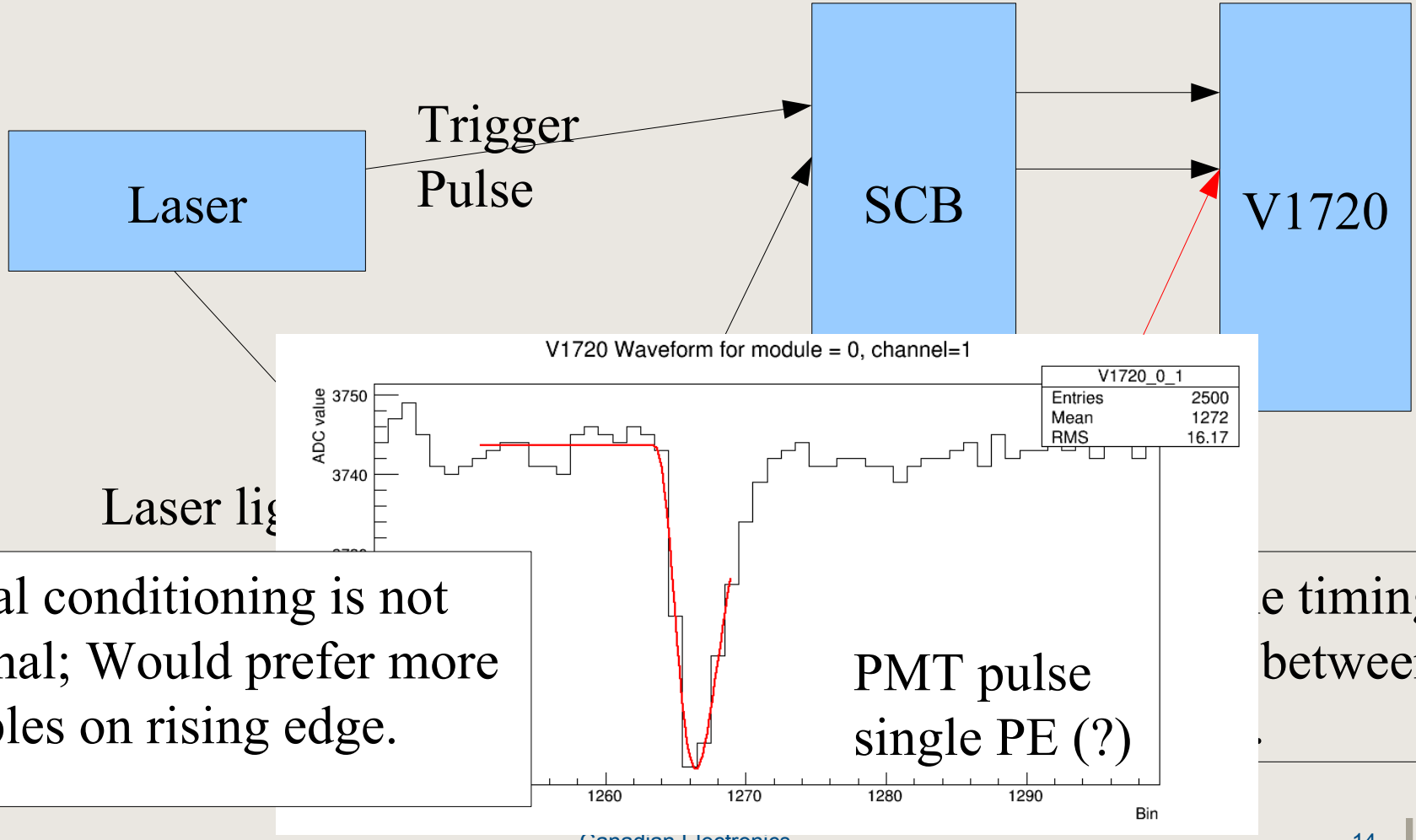
Timing Test Setup



Goal: measure the timing difference width between trigger and PMT pulses.

Hamatsu R9980U 16mm PMT;
should have a small intrinsic timing jitter.

Timing Test Setup



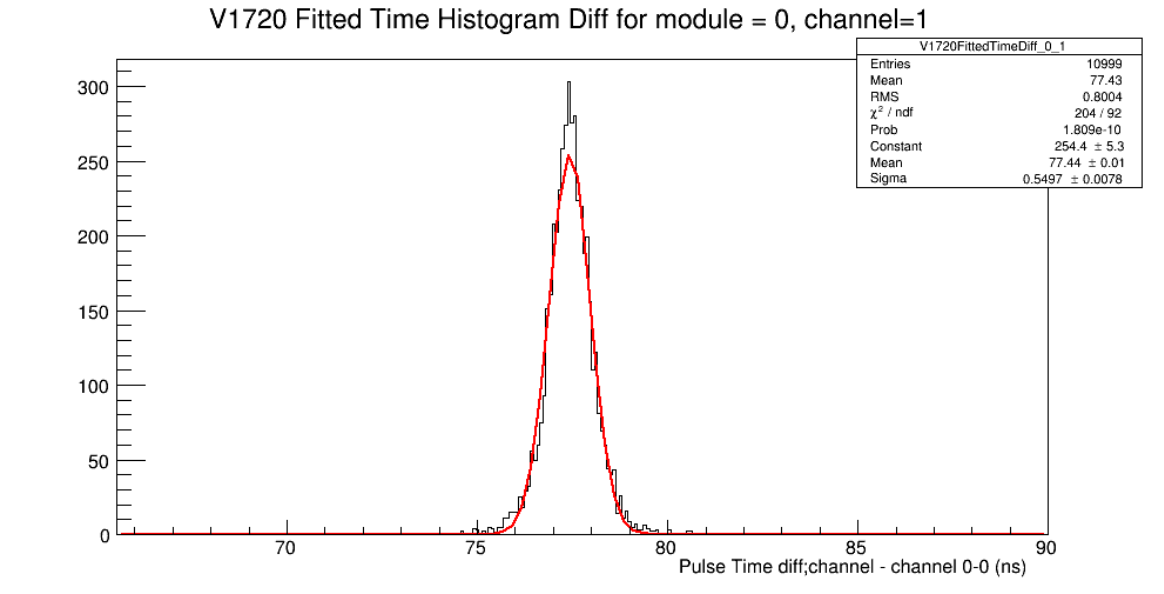
Laser lig

Signal conditioning is not optimal; Would prefer more samples on rising edge.

e timing between

Timing Resolution

- Plot shows the difference between the fitted PMT signal time and reference time.
  - Note: time fits done offline, not in firmware.
- The distribution width is ~0.5ns; even if width is totally from the PMT signal, this is still pretty good.

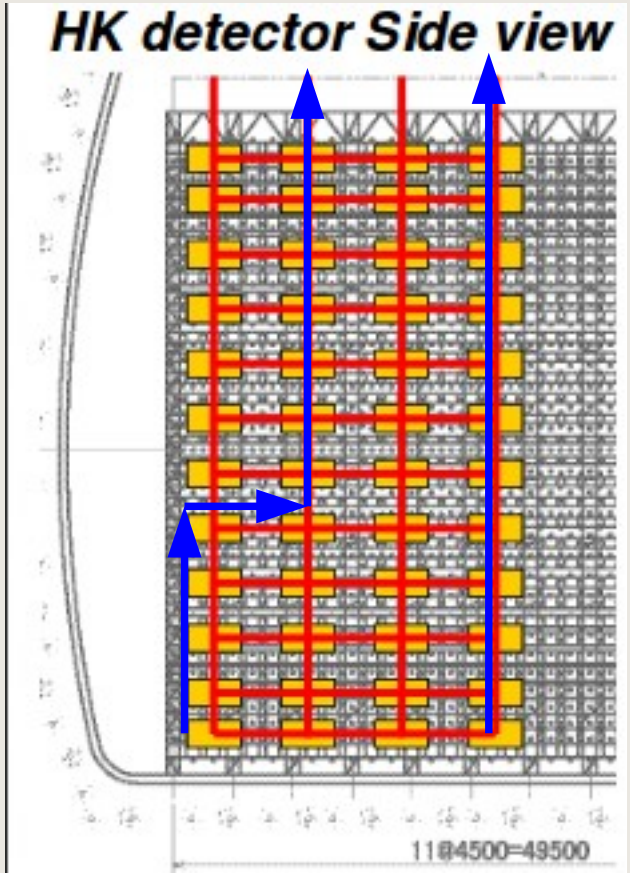


Timing Test Summary

- Initial results with test are promising; can get reasonable 0.5ns resolution for pulses that are ~1 PE.
- Further work:
  - Improve the signal conditioning; stretch the pulse more to get more samples on rising edge.
  - Make proper estimates of timing resolution vs pulse height.
  - Understand what dynamic range this solution provides; don't think that dynamic range is acceptable (only ~200PE). Consider further options:
    - Attenuate pulse more
    - Split into high and low gain channels (higher power/cost)
    - Non-linear amplifiers.
    - Faster (500 MHz) or more precise (14-bit) FADC

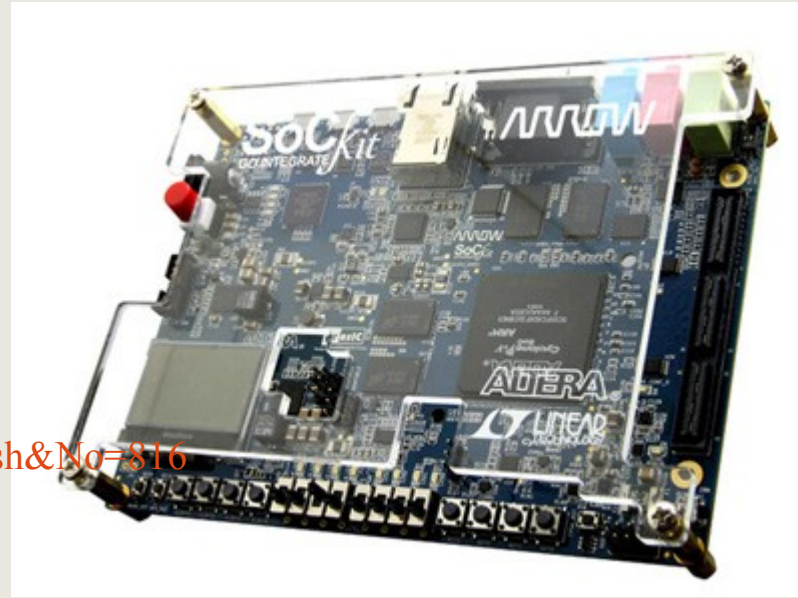
Communication Work

- Have a set of four UBC engineering students who are working on some tests of a possible communication scheme based on RapidIO protocol.
- RapidIO seems interesting because it allows ways of specifying routing of data packets.
- Could use this functionality to route packets for redundant mesh network.



Communication Work II

- Plan is to mock up a test of the RapidIO communication using a set of ~10 Altera FPGA evaluation boards.
- Specifically Terasic evaluation board with Altera FPGA (with NIOS CPU) and dual ARM processors.
- Students have made some progress in getting RapidIO core working and Konstantin has some gotten linux installed on the ARM processor.
- Hopefully students will also compare RapidIO to other possible protocols (ie ethernet).



http://www.terasic.com.tw/cgi-bin/page/archive.pl?Language=English&No=816

Plans for 1kton Prototype

- We hope to provide the FADC digitization and communication scheme for some/all of the 1kton electronics.
- Need to understand how the overall electronics will be provided; useless to provide digitization for PMTs that have no HV.
  - How to divide work?

Canadian Funding for 1kton Prototype

- We have made request to CFI (Canadian Fund for Innovation) for funds to help build part of the 1kton electronics.
  - The grant request also includes money for photosensor development and ND280 heavy water.
- We budget that the money will be spent mostly on TRIUMF engineering support; actual hardware purchases will not be large.
- Timeline:
  - Decision on grant in early 2015, money flows in mid-2015.
  - Difficult; will need to make some progress in 2014 without substantial engineering support.

Conclusions

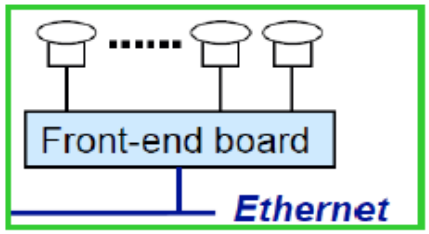
- We are interested in helping with solutions for digitization and communication for HK front-end electronics.
- We hope to integrate these elements in the 1kton electronics; we have requested funding to make this happen.
- We are looking forward to discussing ways of collaborating on this work.

Backups

Front-end Board Elements

- From Hayato-san's slides

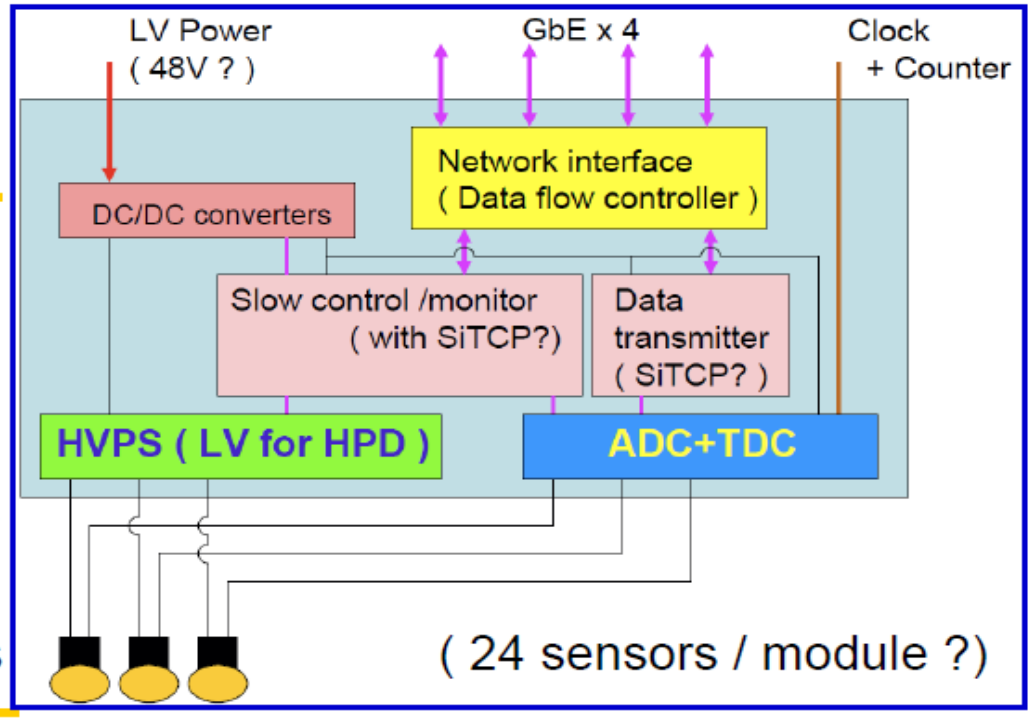
Possible front-end electronics module connections



Key components

- Self triggering & dead-time free ADC + TDC
- HV (LV) for photo-sensors
- Intelligent network interfaces

Schematic diagram of the front-end board



In the last meeting, experts strongly recommend to keep the module DRY (not to in the water).
Detector design group want to reduce the weight of the cables….

Triggering Scheme

- From Hayato-san's slides

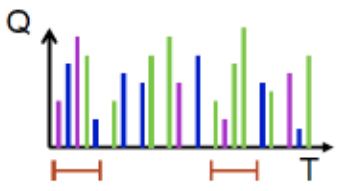
Triggering Scheme

Simple “majority” trigger is assumed.
Count # of hit photo-sensors
within a few ~ several hundreds of ns
If # of hits exceeds the threshold,
hit data are recorded as an event.

Collect all the hits in a detector (compartment)
and search for the timing cluster (peak)

1) sort hits in order of time

2) search for events
by software or hardware



For Hyper-Kamiokande, ~ 3 PMT hits / MeV
Threshold : 20 ~ 30 PMT hits in 400 ~ 600 ns.
(3 compartments)