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The ATLAS Insertable B-Layer

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The Insertable B-Layer

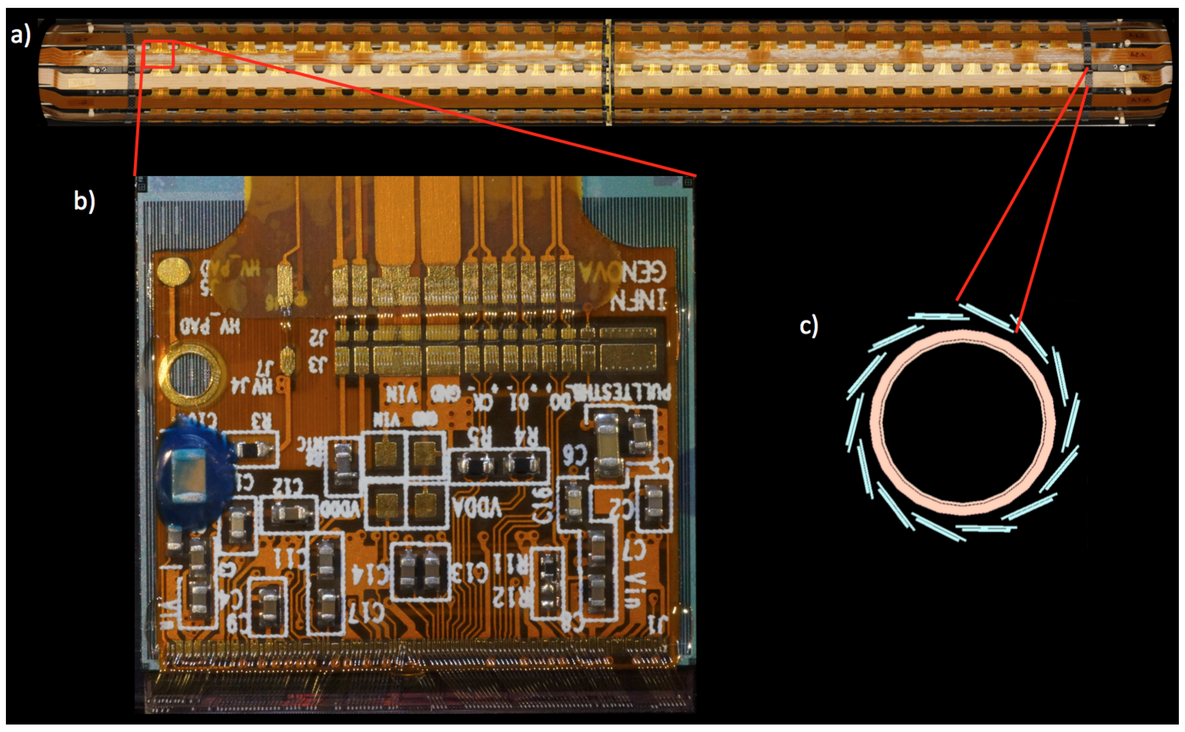

Figure 1: The Insertable B-Layer, a) side view, showing the assembly of fourteen staves, b) an integrated FEI4-B module (FEI4-B front end, silicon sensor, and flex) , and, c) the radial geometry of the 14 staves around the beam pipe.

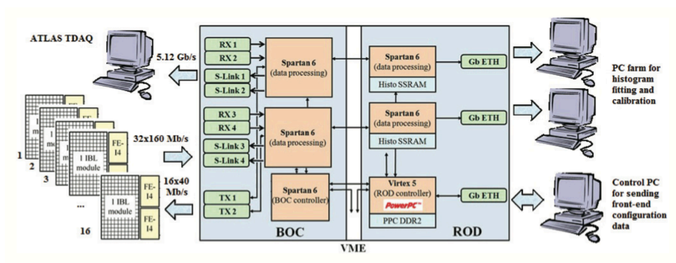

Figure 2: Overview of the IBL DAQ system

Introduction

Twelve million new channels at the heart of the ATLAS detector 3 cm from the IP, the Insertable B-Layer (IBL) is ATLAS's 4th and innermost silicon pixel layer. Built from the FEI4-B front end chip, one specially designed for the unprecedented occupancy that LHC run 2 brings, and bonded both to planar and to new 3D silicon substrate, the IBL will increase substantially the efficiency, quality, and precision of ID tracking at Point 1.
In 3.5 years the IBL has been built and integrated with over 99.9% working channels into the ATLAS experiment. This poster introduces the IBL detector and DAQ, as well as the process by which its quality has been measured and achieved.

Design

The ATLAS Insertable B-Layer was designed with the following physics goals in mind:

- Tracking performance: A 4th silicon measurement 3 cm from the IP enhances reconstructed track quality and increases impact parameter resolution resulting in better *b*-tagging efficiency.
- Tracking robustness: The fourth layer ensures the required three measurements for curved track reconstruction will remain in light of expected pixel degradation.
- Increased luminosity and pileup: the FEI4 accomodates the increased charged particle flux from reduced radius and eventual High Luminosity LHC beam conditions with decreased pixel size and improved readout design, Figure 5 below.
- Radiation dosage: the IBL was designed to be robust against large radiation doses, especially from unexpected events such as beam failures.

Characteristics

- 14 staves, 32 FEI4-Bs per stave, 26880 pixels per front end
- Radius: 33 mm
- Pixel size (ϕ, z): 50x250 μm
- Coverage: $\eta < 3.0$
- Data rate: 160 MB/s per front end
- Cooling: -40C by CO2 (expected sensor temperature is -25C)

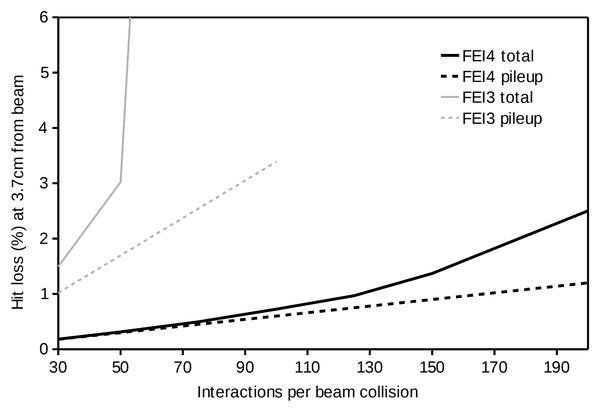

Figure 5: The FEI4 shows significantly reduced hit loss over the existing pixel FE in the IBL geometry accross the range of expected beam conditions expected from 2015 - 2021.

Data Acquisition

Housed in a single VME crate, 14 Read-out Driver (ROD)/Back of Crate Card (BOC) pairs receive data via optical link at a rate of 160 MB/s per FE-I4. Several Spartan6 slave FPGAs build events on the BOC and histogram the resulting hit data on the ROD. A Virtex5 master FPGA with an integrated PPC processor running C++ directs resources on the ROD/BOC pair during calibration and data-taking. An external fit farm is used for the processing of histograms produced by the ROD slave FPGAs.

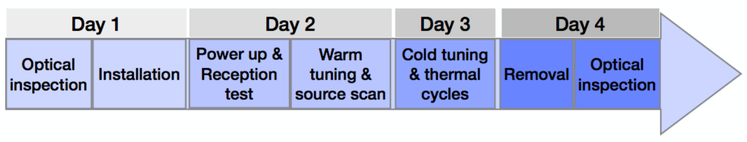

Figure 3: Point 1 quality assurance stave-by-stave testing schedule.

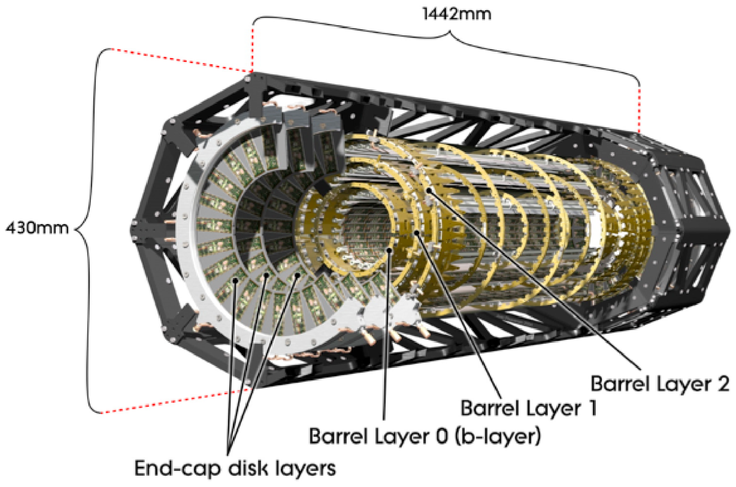

Figure 4: ATLAS Pixel Detector.

FEI4-B Front End

A 2cm x 2cm chip, the FEI4-B contains 26880 pixels, with end of chip logic for buffering, error correction, and I/O. Figure 1 b). Each pixel combines a tiny analog amplifier and discriminator with a digital hit processing and buffer circuit. The amplifier and discriminator levels of each pixel are calibrated to correct for differences in pixel manufacturing and degradation resulting from radiation.
The FEI4-B runs in two primary modes: data-taking and calibration. In data-taking mode, the FEI4-B operates independently to prepare hits into packages that are sent to the DAQ chain for readout via optical link. In calibration mode, the FEI4-B responds to commands to facilitate testing and chip configuration.

Construction and Testing

The IBL is assembled from fourteen staves, each bringing to 32 FEs the necessary structure and services, including: cooling, high and low voltage, and data input/output. Each stave has in turn been assembled from thoroughly-tested and ranked individual FEs. Each stave has undergone a 3 to 5-day series of tests, including digital and analog injection scans, triggering on external Americium and Cobalt sources, hot-cold thermal cycling, and individual pixel tuning, Figure 3 above.

Status and Stave Ranking

Twenty IBL staves were ranked by minimizing a metric, shown in Figure 6 right, designed to maximize the η - ϕ coverage of the detector: Staves are constructed with better FEI4 modules placed closer to $|\eta| = 0$, as this minimizes the chosen metric for each stave. The detector is built using the fourteen best-performing staves. A total of 20 staves were built with 18 of them full-filling all specifications, Figure 6 right. The selection results in a less than 0.1% bad pixel rate.

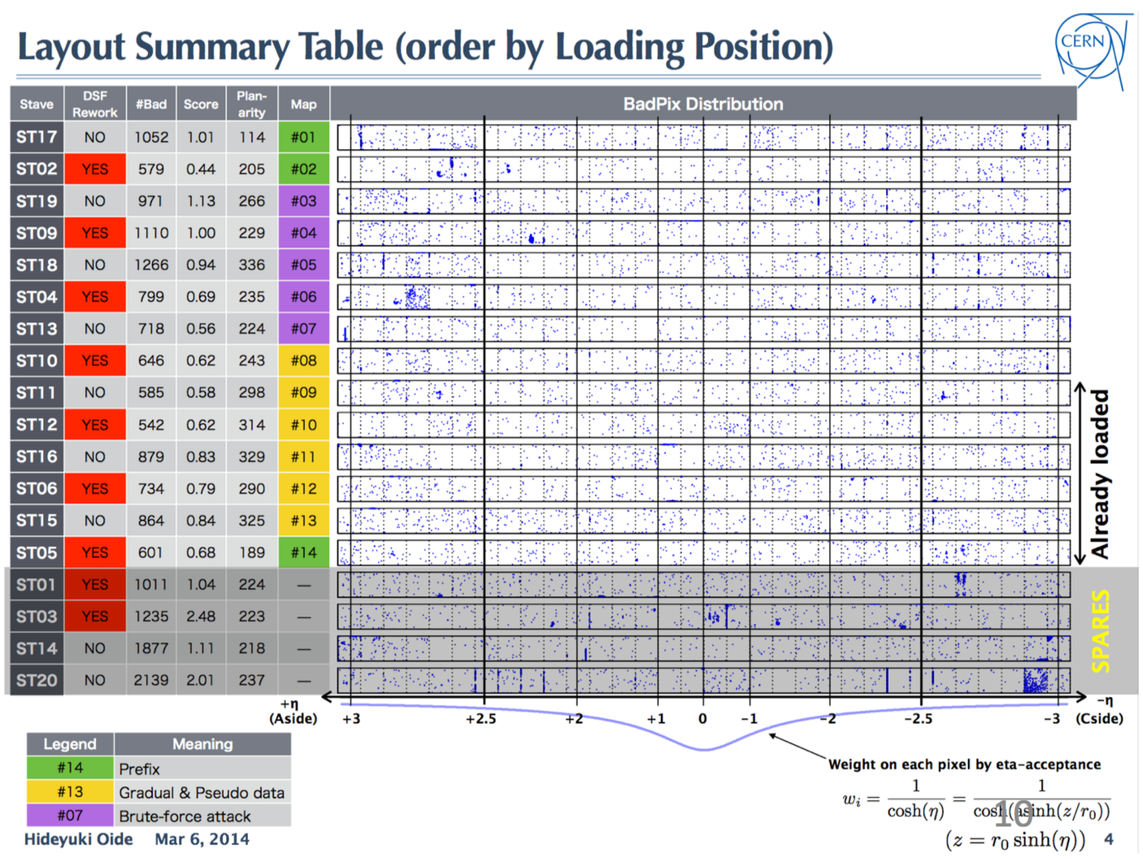

Figure 6: Bad pixel distribution, showing the intentional selection of higher-quality modules for low $|\eta|$. The IBL has < 0.1 % bad pixels.

References

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[4] The ATLAS Collaboration. ATLAS Pixel IBL: Stave Quality Assurance. *ATLAS Public Note in progess*, 2014.