The Phase 2 Upgrade of the ATLAS Hadronic Tile Calorimeter Readout Electronics

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ATLAS Tile Calorimeter System

TileCal in a Nutshell

- TileCal is the central hadronic calorimeter system in ATLAS
- Simplified view: Good hadronic calorimetry → Good jets → Exciting physics!
- The TileCal converts hadron energy to readout signals in four main stages
  - Iron/Scintillator Tiles: Convert hadrons to light
  - Photo-Multiplier Tubes: Convert light to charge
  - On Det. Electronics: Convert charge to ADC counts
  - RODs: Read out drivers for signal consolidation
- On detector electronics samples shaped pulse seven times with an active measure of the baseline
- TileCal was designed and operates with
  - 4 partitions × 64 azimuthal wedges with 9852 PMTs
  - 2 PMT's and readout per cell
  - Granularity : 0.1×0.1 in (η,φ) for η<1.7
  - Performance : $\sigma_{hadronic} \sim (50/\sqrt{E} + 3)\%$

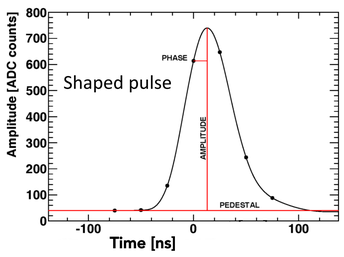


Figure 1 (left) – Typical signal shape, fit to seven pulse samples, used for extraction of signal strength.

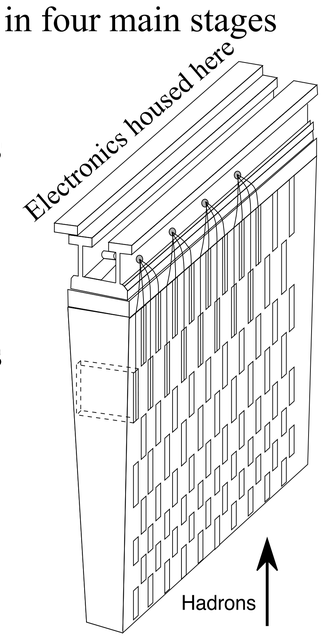


Figure 2 (above) – Physical layout of one of the 64 azimuthal wedges. The electronics being replaced are housed in removable "drawers", placed furthest from the beam line.

The Current System

- Single physical "superdrawer" housing
- Amplifier/shaper "3-in-1 Cards"
  - High/low gain channel for single PMT
  - Directs signal to adder board for analog tower sum for L1Calo trigger
- Digitizer Cards / Motherboard
  - Sixteen 3-in-1 cards per board
  - Signal and voltages daisy chained
- Interface Board
  - Single pathway for controls and signals
  - Output to buffer at 100 kHz
- How to improve with the new system
  - Replace COTS electronics with faster rad-hard components; fewer connectors
  - Redundancy (e.g. voltage) is key
  - Fully digitized signal will help physics → required 48 Gb/s output

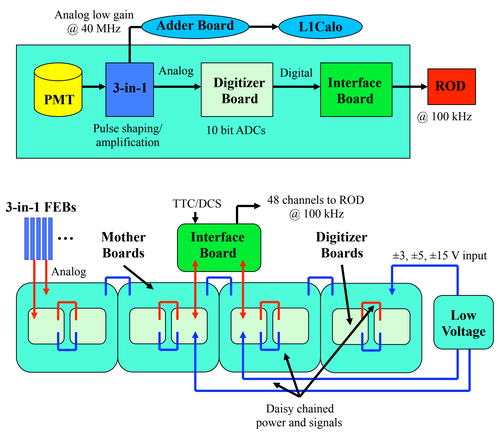
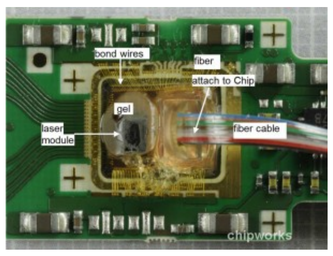


Figure 3 – Signal pathway (top) and physical layout of full system (bottom) for current design of the current tile calorimeter readout electronics.

Main Board / Daughter Board

- Main board feeds digitized signal to daughter board
  - Main board design dependent on FEB choice
  - Low voltage supplied to two diode-ORed halves (redundancy)
  - Digitized signals on traces up to 20 inches
- Daughter board transmits signal to sROD
  - Separate optical fibers readout independent halves of daughter board
- Data from all cells sent at 40 MHz to form trigger in sROD
- Low voltage distributed from +10V block and regulated with point of load regulators



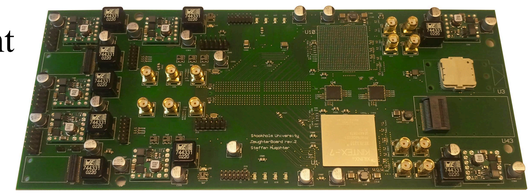


Figure 5 – (top) Fiber optic switch used to transmit signal at 10 Gb/s and (bottom) prototype of third generation daughter board

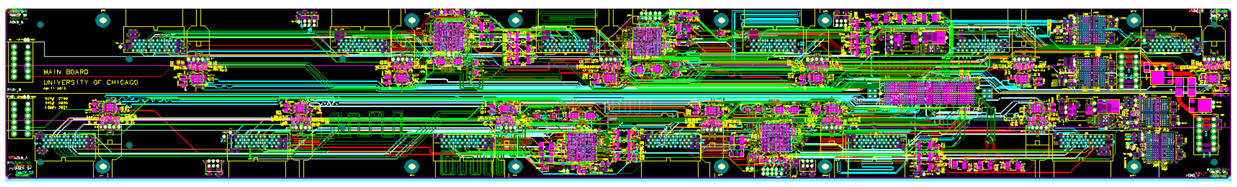


Figure 6– Trace layout for main board showing consolidation of signals frm FEBS on top and bottom and transport to daughter board readout on left end. The board is composed of 6 signal layers and 8 power planes.

The New System

- Main improvements
  - No daisy chaining of low voltage or data
  - Data pipeline in off-detector super-ROD
  - Fully digital trigger at 40 MHz
- "Mini-drawer" physical architecture
  - Standalone electronics per mini-drawer
- Front End Boards (FEBs)
  - Improved 3-in-1 cards or ASIC option
- Main Board
  - Combines digitizer and motherboard
  - Digitizes and serializes 12 FEBs
- Daughter Board
  - Replacing interface card with single high bandwidth unit per main board
- Super-ROD (sROD)
  - Off-detector electronics with tiered trigger

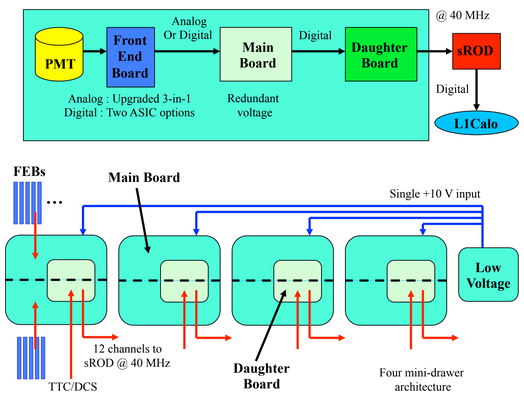


Figure 4 – Signal pathway (top) and physical layout of full system (bottom) for current design of the future upgraded tile calorimeter readout electronics.

The Off-Detector sROD

- sROD controls timing and trigger controls, routes data to DAQ, and forms trigger from cell energies
- Two GigaBit Transfer (GBT) chips used for off-board communication implemented in two FPGAs
- Tiered veto system for data pipeline implemented through FELIX
  - L0Calo : 40 MHz → 500 kHz
  - L1Calo : 500 kHz → 200 kHz

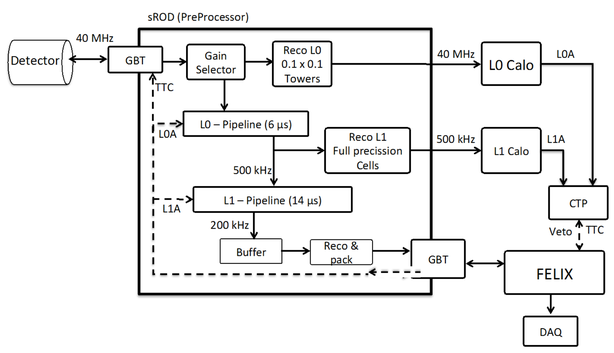
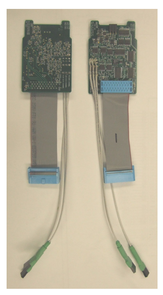


Figure 9 – Conceptual design layout for the upgraded super readout driver (sROD)

Front End Boards

- Functionality : Convert PMT signal to sampled or integrated pulse
- Two options being developed
  - Upgraded 3-in-1 Cards (left): Off the shelf components give improved linearity. Currently being implemented in "demonstrator" for Run 2
  - ASIC Implementation (right): Two options being studied for this application. Both require multiple gains for a single input. Time to digital converter allows for identification of out of time bunch crossings.

3-in-1 Cards



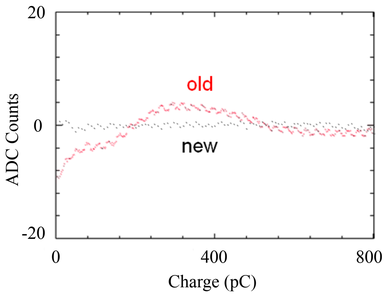
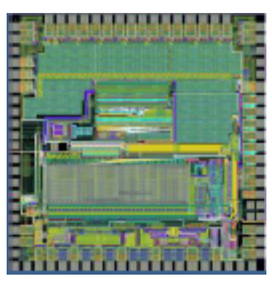


Figure 7 – Physical design (left) and response linearity (right) of the upgraded 3-in-1 front end boards

ASIC



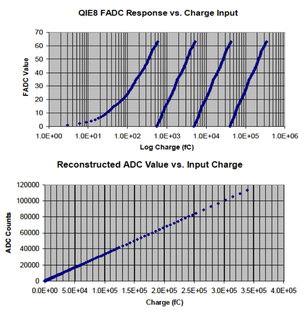


Figure 8 – Design layout (left) and response linearity (right) for the one implementation of the ASIC FEB