LHCP 2014 Poster Session - Columbia University, 6 June 2014

High-Speed Low-Latency Trigger Signal Packet Router for the ATLAS New Small Wheel Detector

Phase I ATLAS Upgrade

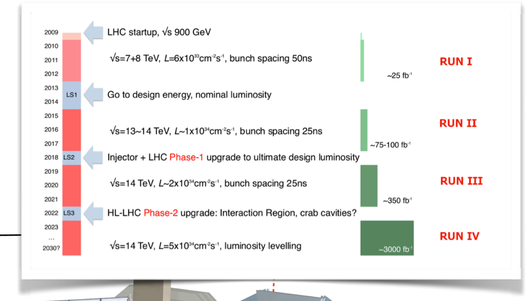
- Over the next decade, the LHC complex will be upgraded in three stages (Phases 0, I, and II), in order to maximize the machines capability for producing new physics.

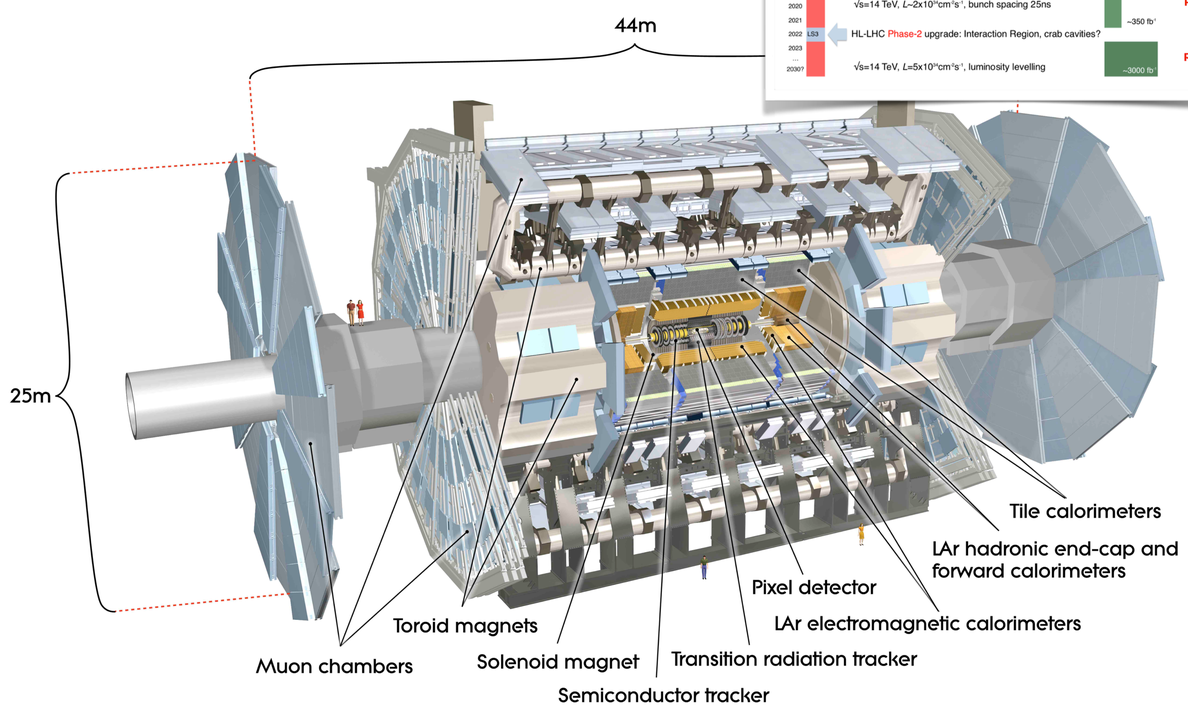
- After the Phase-I upgrade in 2018, the accelerator luminosity will be improved to the maximum design luminosity of the LHC to $2x10^{34}$ $cm^{-2}s^{-1}$. At this luminosity, ATLAS will collect an astonishing 100 fb^{-1} per year.

- To take advantage of the increased luminosity, the ATLAS detector will undergo corresponding improvements, focused primarily on enhancements to the trigger system to cope with luminosities beyond the nominal design.

  - ➡ The Phase-I upgrades will allow ATLAS to maintain low pT trigger thresholds for isolated leptons by increasing the granularity of the calorimeters involved in the Level-1 trigger and by introducing new muon trigger and tracking detectors in the forward direction.

  - ➡ Precision measurements of the couplings of the Higgs boson, if found in the low mass region, as well as searches for supersymmetric particles in a large region of the SUSY parameter space, rely on the capability of efficiently selecting low pT isolated leptons. Fast accurate tracking information provided near the start of the Level-2 trigger processing will lead to much more effective identification of events with isolated t and b-hadrons, improving the selection of Higgs boson decays and sensitivity to many other physics channels.

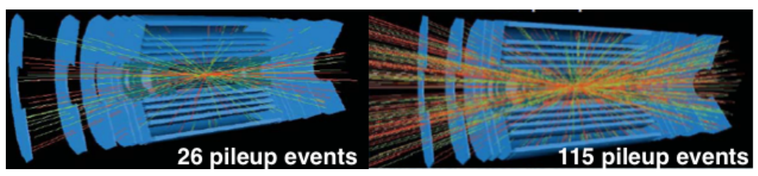




New Small Wheel Detector

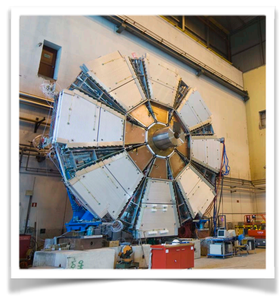
- The ATLAS forward muon spectrometer covers $1.0 < |\eta| < 2.4$ for triggering and $1.0 < |\eta| < 2.7$ tracking. It consists of three detectors: the small wheel, the big wheel, and the outer wheel.

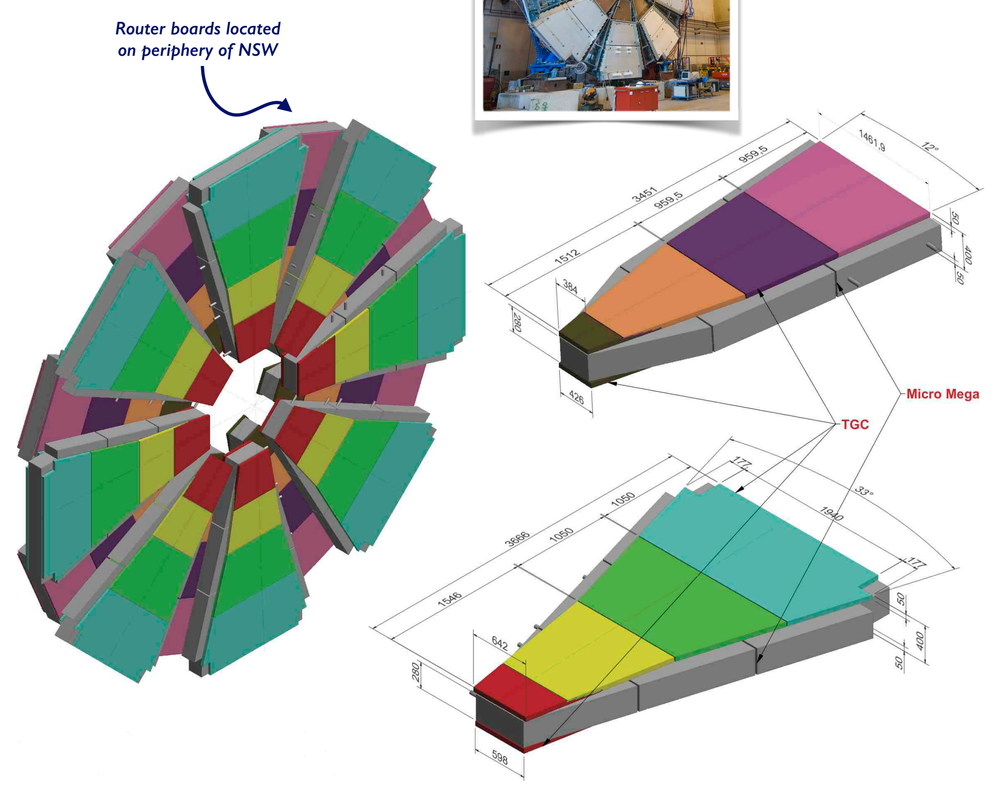
- High energy conditions expected after the Phase-I upgrade indicate a substantial degradation in the resolution and efficiency of the small wheel detector, where high resolution measurements of the momentum of forward tracks are dependent on accurate measured points. Further, at high luminosity roughly 90% of muon triggers in the end-cap are fakes.



- The new small wheel (NSW) will have improved spatial and timing resolution, allowing the trigger system to better verify if a track originates from the interaction point.

- The NSW consists of sixteen alternating large and small sections of detector systems arranged in a ring. Each section has eight layers of small-strip TGC (sTGC) detectors and eight layers of Micromega (MM) detectors. The sTGC will primarily be used for triggering and the MM for precision tracking.





High-speed, low latency Router for Trigger Signals

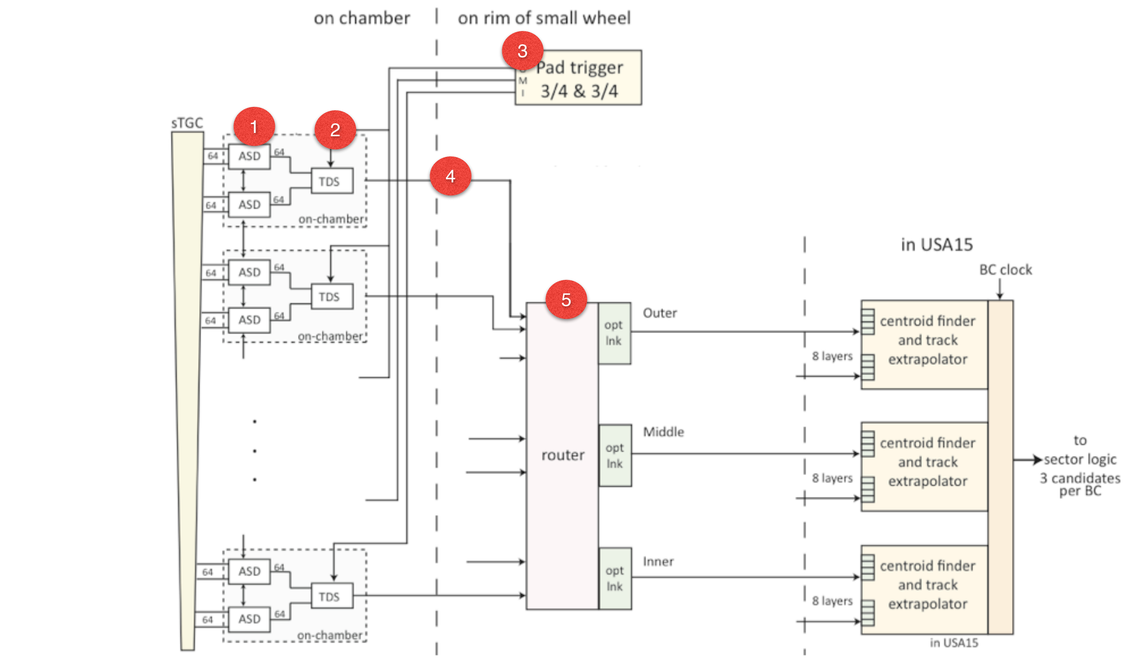
- A block diagram of the sTGC front-end trigger logic for one layer of a 1/16th sector is shown in the figure to the right. On detecting a signal peak..

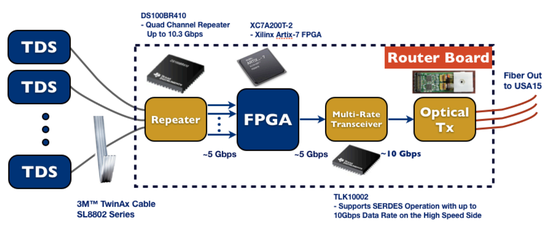
  (1) The front-end electronics, which consists of an amplifier-shaper-digitizer (ASD), digitizes the time and amplitude of the signal. The digitized signal is sent to a trigger data serializer (TDS).
  (2) At the TDS, the strips are buffered and tagged with an identification number for the bunch crossing (BCID).
  (3) From the TDS, pad signals are sent to the pad trigger logic, which identifies a track candidate if there are coincident hits on three out of four layers of pads on both sets of quadruplet sTGC detectors. If a candidate track is identified, the pad trigger logic selects the band of strips in each layer (band-ID) associated with the triggered pads, and distributes the IDs of the bands to the TDSs.
  (4) The TDSs then transmit the strip charges, BCID, band-ID, and ϕ-ID (total 128 bits at 5 Gbps) to the signal packet Router on the periphery of the new small wheel.
  (5) The signal packet Router boards handle all incoming traffic from the TDS chips, serving as a very fast switching-yard between incoming active TDS signals and a limited number of opto-electronic outputs. These signals are sent by fiber (5 Gbps) to track finding processors off-detector where centroids and track segments are calculated and sent to sector logic to be combined with candidate tracks from the Big Wheel.

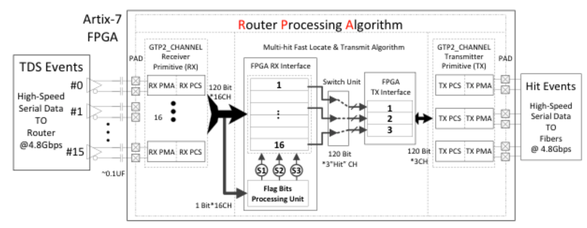
- The customized signal packet router located on the periphery of the NSW, which consists of a repeater to buffer the incoming signal, an FGPA with the routing algorithm, an optional multi-rate transceiver to increase the output speed to 10 Gbps, and the opto-electronics output.

- Radiation levels on the rim are low enough to allow implementation by FPGAs. To reduce latency to < 65 ns, the entire TxRx firmware has been customized, removing unessential functionality and implementing much faster stripped down transceiver firmware in the fabric of the FPGA.

- To minimize the number of optical fibers and the rate of lost TDS signals, a flexible routing algorithm has been developed which is able to route any of the incoming TDS signals to any fiber optic output on an individual FPGA.







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