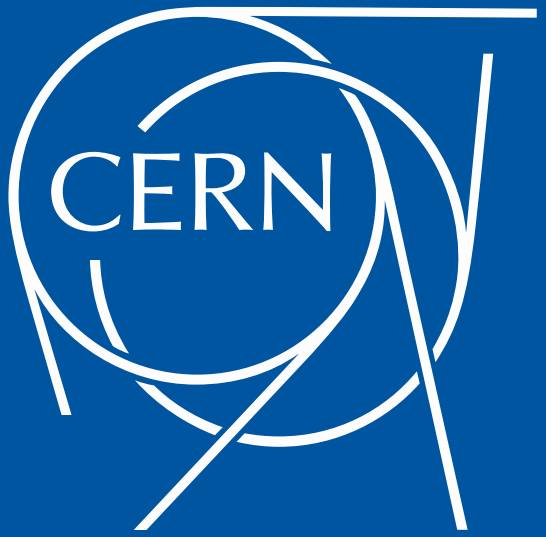
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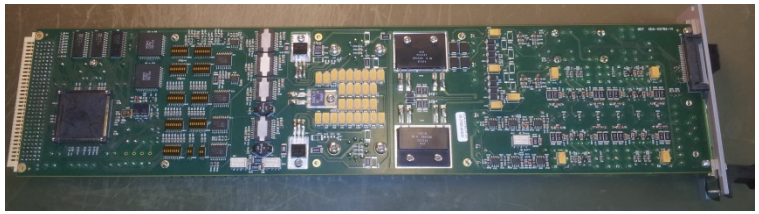
Nikolaos TRIKOUPIS TE-CRG-CI

Results of PSI radiation tests on EH Beam Screen board

Contents

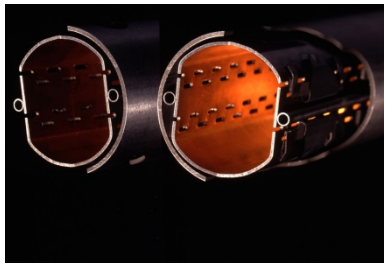
- Application – Cryogenics Crate - Beam Screen
- Radiation evaluation of individual components
- EH BS prototype board installation and results
- Rad tests on reference voltages

EH BS Introduction

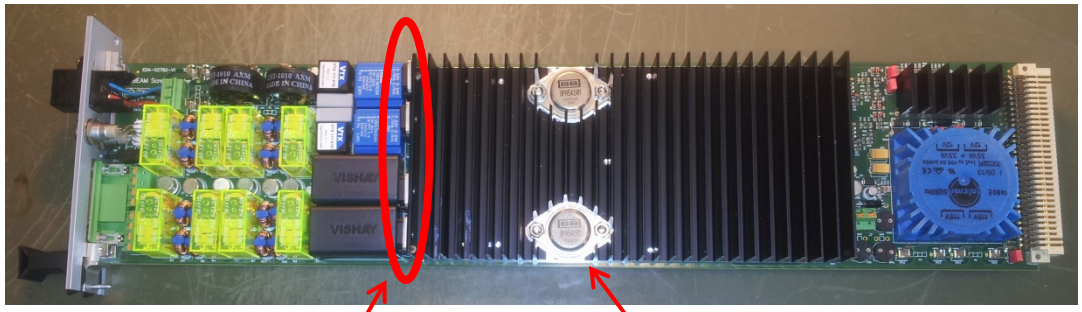


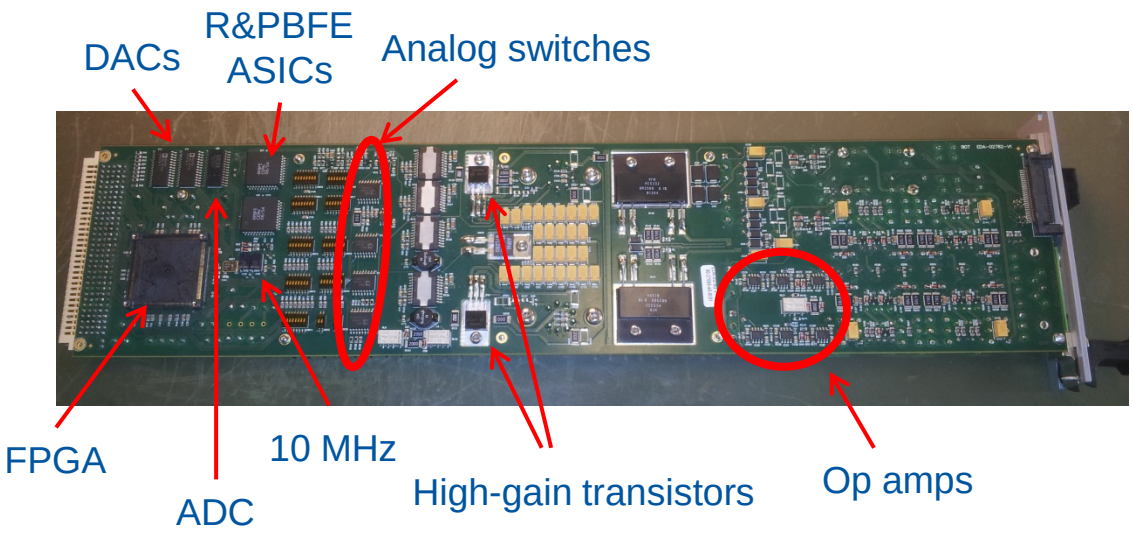
Purpose: Provide power to the Beam Screen of the LHC
to release trapped gas molecules

1. Two independent channels
2. DC (0-60VDC, 0-2A), AC (0-400VAC, 0-4A)
3. Report of delivered power in AC/DC
4. Supports thermocouple or resistive sensor for protection
5. Extensive feedback and diagnostics
6. Safety features



EH BS active parts

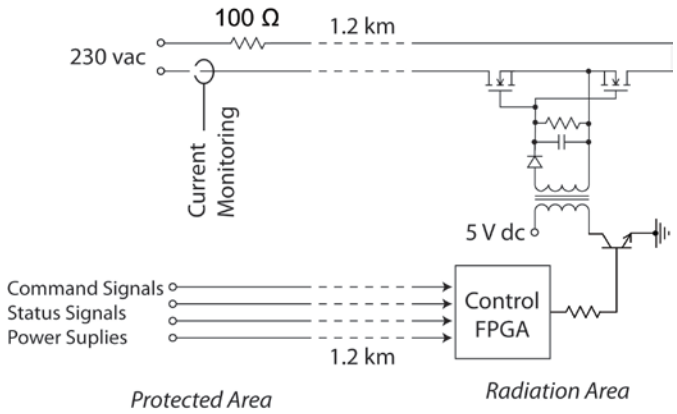




- Power MOSFETs
- High power Op Amps
- Op amps
- DACs
- ADC
- R&PBFE ASICs
- Analog Switches
- FPGA
- ADC
- 10 MHz
- High-gain transistors

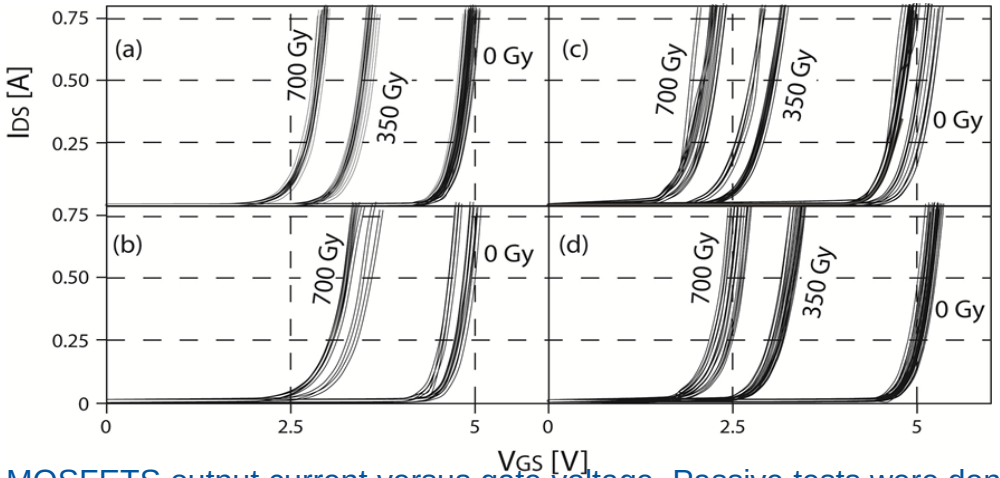
CNRAD for Power MOSFETs

MOSFET Type	Manufacturer	Breakdown Voltage	Drain Current	ON resistance	Heatsink required	Passive Test	Active Test
FCA36N60NF	Fairchild	600 V	34.9 A	0.095 Ω	No	OK	OK
FDP7N60NZ	Fairchild	600 V	6.5 A	1.25 Ω	Yes	OK	?
STFI10NK60Z	STMicroelectronics	600 V	10 A	0.65 Ω	Yes	OK	?



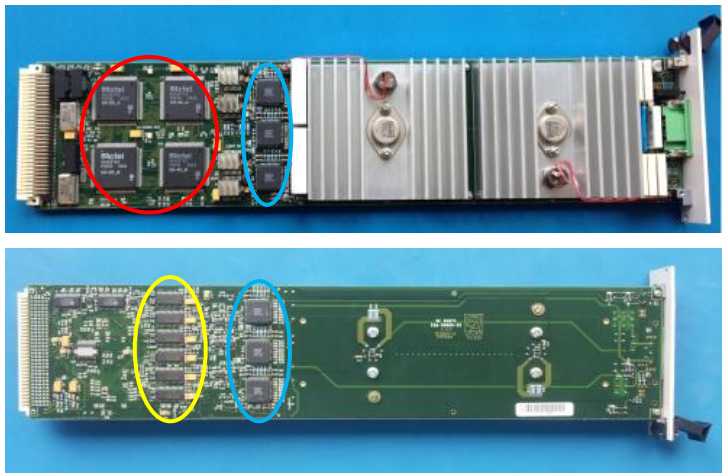
No change on ON resistance observed

Tested
29 JUN 2012 to 03 DEC 2012

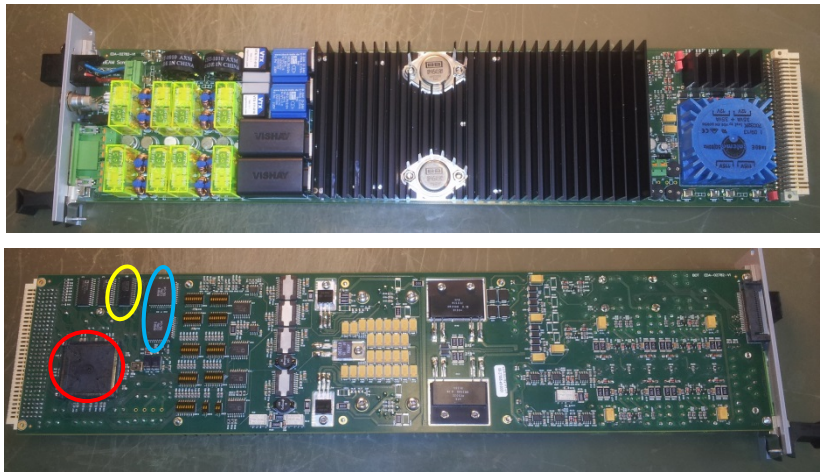


MOSFETS output current versus gate voltage. Passive tests were done for 30 devices of each type, the characteristics were measured before irradiation (0 Gy) and then 10 samples were removed from CNRAD after 353 Gy and the rest at 702 Gy. (a) passive and (b) active data for FCA36N60NF. Passive data for (c) STFI10NK60Z and (d) FCA36N60NF.

Importance of analog switches



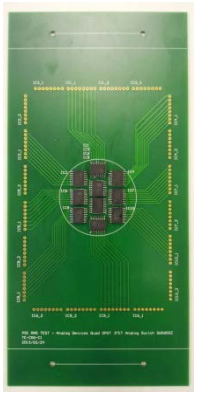
Previous version of EH

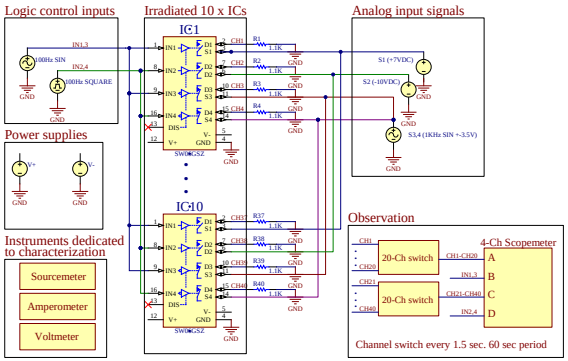


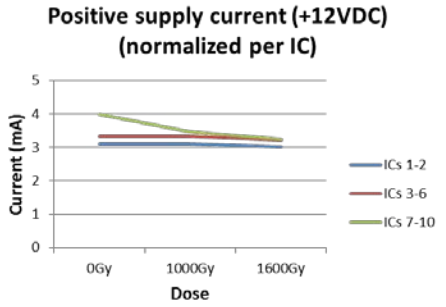
Beam Screen EH

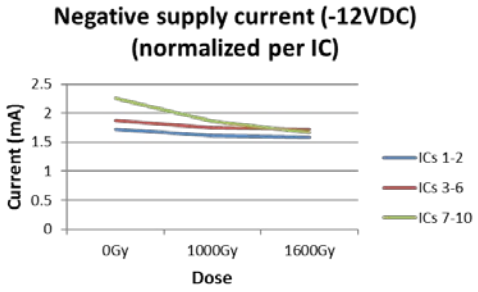
- Reduction in component count: FPGA, ADC, R&PBFE ASIC
- Big cost savings
- Area savings that made the implementation feasible

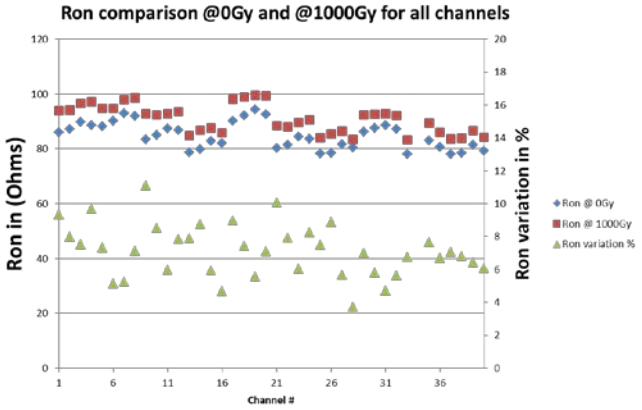
PSI & CNRAD for analog switches

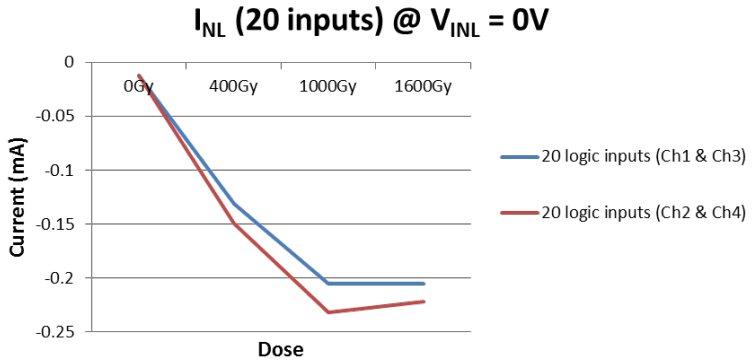








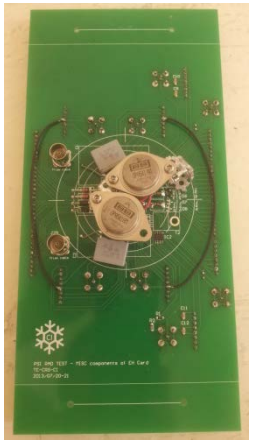


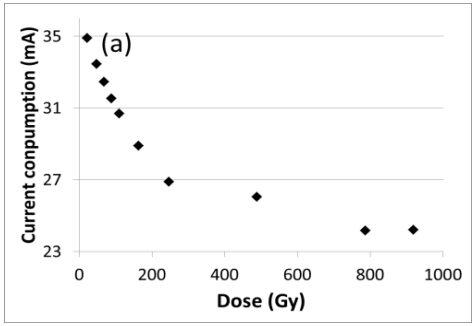


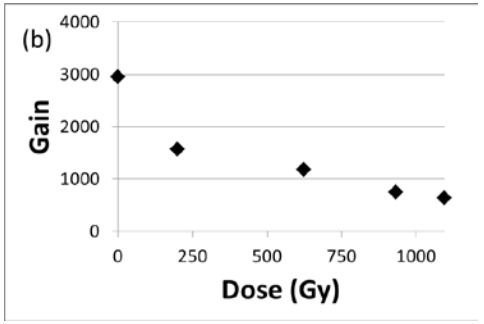
Tested on 24th FEB 2013 (PSI)
Preliminary test 347Gy at CNRAD

Results presented on 25th March 2013 on RADWG

PSI on ancillary components







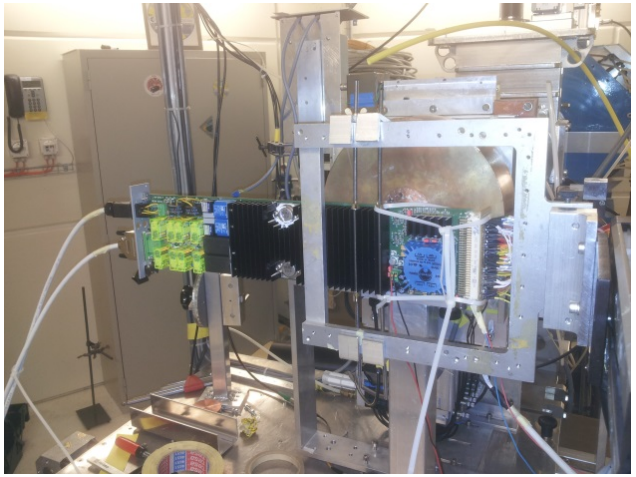
a) Summed current consumption for 2xOPA541AM. b) Gain for the 2N6388G

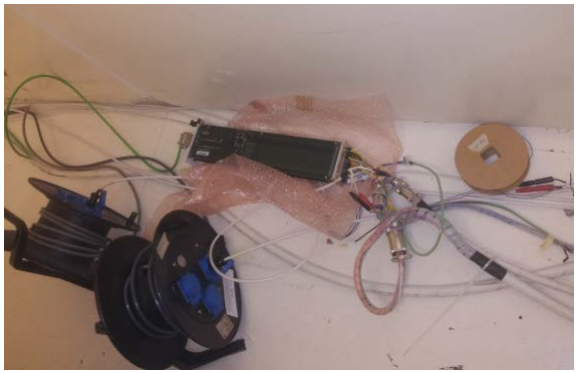
Type	Component	Manufacturer	Purpose	Result
Power Op Amp	OPA541AM	Texas Inst.	Re-qualify	Drift
Op Amp	OPA627AU	Texas Inst.	Re-qualify	OK
Osc 10MHz, 5V	LFSPXO017735	IQD	NEW	OK
Osc 10MHz, 5V	CSX750FCC10.000M-UT	Citizen Fin.	NEW	OK
High-gain transistor	2N6388G	ON Semi.	NEW	Drift
Zener diodes	BZX84B5V6 & BZX84A2V4	NXP Semi.	NEW	OK
Zener diodes	1N5333BG & 1N5350BG	ON Semi.	NEW	OK
82uF polyester	B32526T0826K	EPCOS	NEW	OK
10uF polypropylene	MKP1848S61050JP2C	VISHAY	NEW	OK
47nF X1 polyprop.	BFC233810473	VISHAY	NEW	OK
Diode	PMLL4448,115	NXP Semi.	NEW	OK
Schottky diodes	VS-10BQ100 & VS-30BQ100	VISHAY	NEW	OK

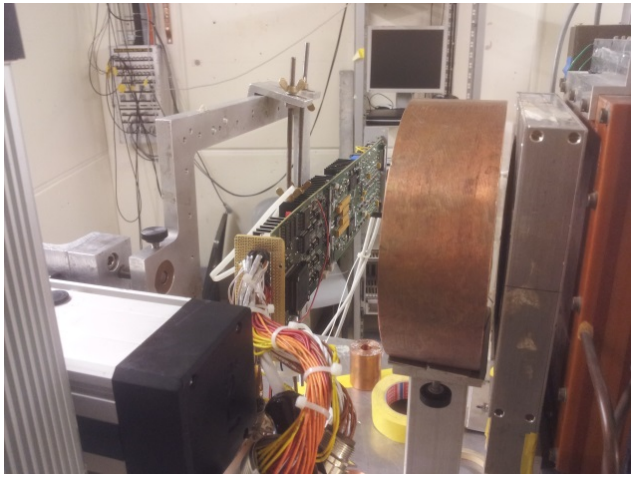
- Power MOSFETs
- **High power Op Amps**
- **Op amps**
- DACs
- ADC
- R&PBFE ASICs
- Analog Switches
- FPGA
- ADC
- **10 MHz**
- **High-gain transistors**

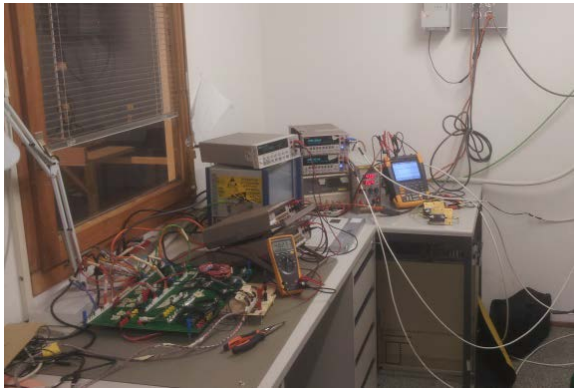
Tested on 20-21 JUL 2013 @ PSI

EH BS prototype test - Installation







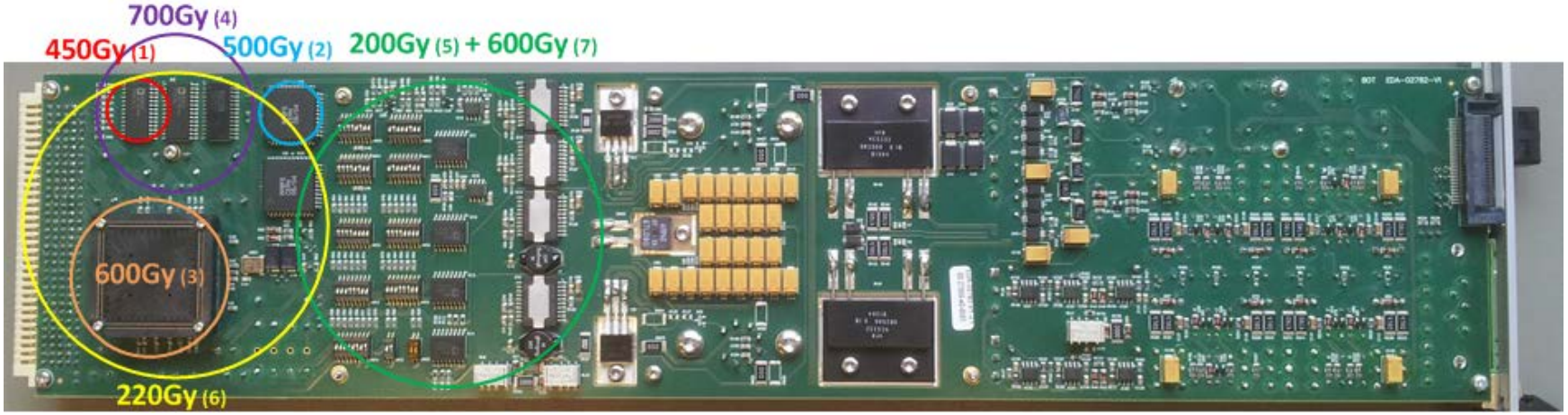


Tested on 2-4 NOV 2013

EH BS prototype test - Plan B…

Hopefully, there was no need to go to plan B

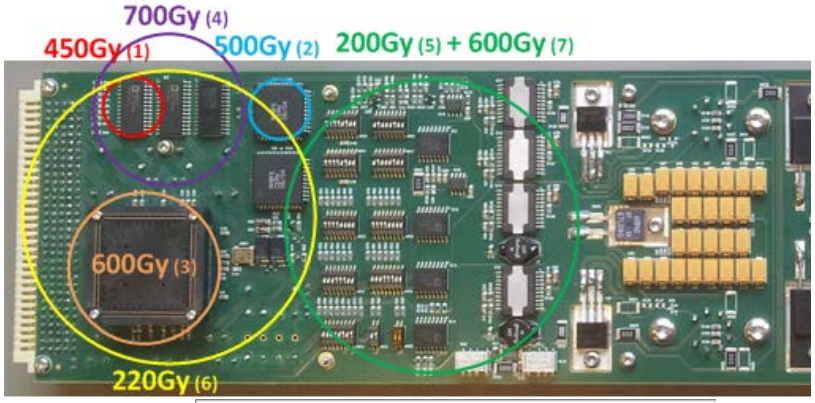
EH BS test – Irradiation plan

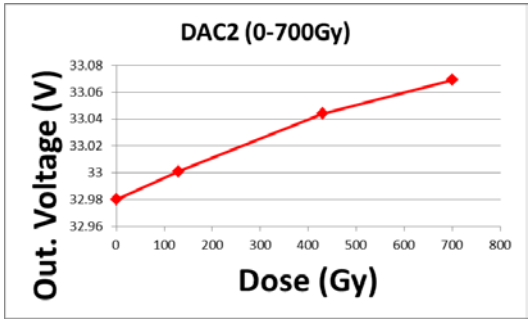


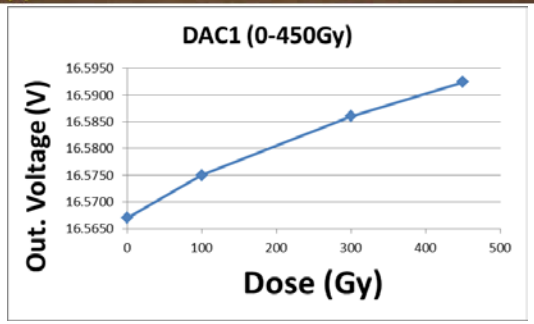
1. DAC1 to 450Gy
2. ASIC to 500Gy
3. FPGA to 600Gy
4. DAC1, DAC2, ADC to 700Gy
5. Analog switches to 200Gy
6. FPGA, DAC1, DAC2, ADC, Osc. to 220Gy
7. Analog switches to 600Gy

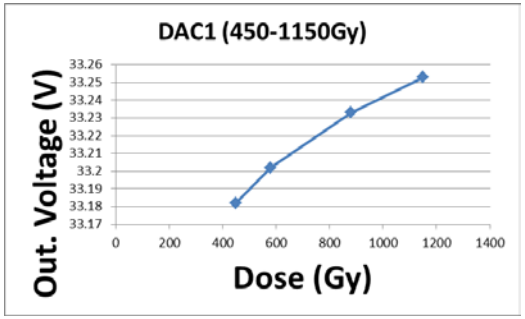
EH BS test – Results - DAC

1. **DAC1 to 450Gy**
2. ASIC to 500Gy
3. FPGA to 600Gy
4. **DAC1, DAC2,** ADC **to 700Gy**
5. Analog switches to 200Gy
6. FPGA, DAC1, DAC2, ADC, Osc. to 220Gy
7. Analog switches to 600Gy





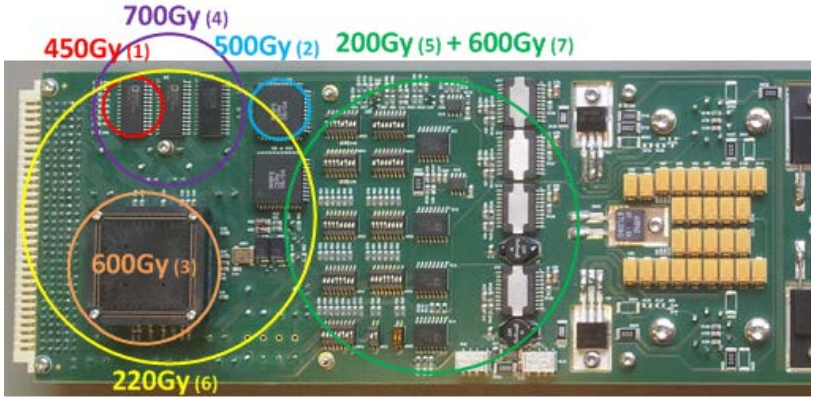




1. DAC1(setpoint1): +0.15% drift for 450Gy
2. DAC1(setpoint2): +0.21% drift for 700Gy
3. DAC2 : +0.27% drift for 700Gy
4. No annealing observed after 12h

EH BS test – Results - ASIC

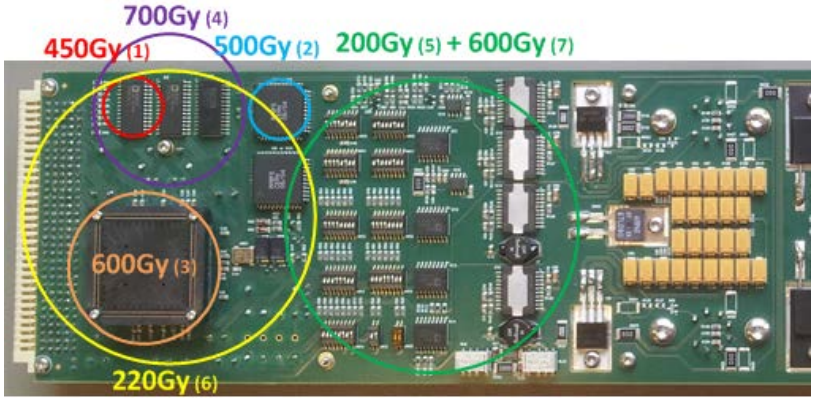
1. DAC1 to 450Gy
2. **ASIC to 500Gy**
3. FPGA to 600Gy
4. DAC1, DAC2, ADC to 700Gy
5. Analog switches to 200Gy
6. FPGA, DAC1, DAC2, ADC, Osc. to 220Gy
7. Analog switches to 600Gy

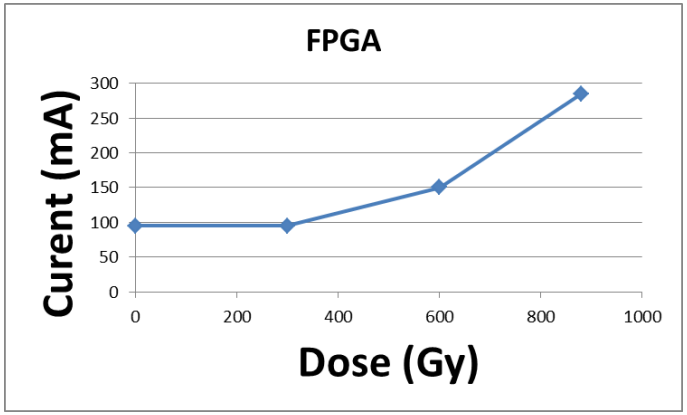


1. No drift, or accuracy change observable
2. No error in calculations or a protection triggered

EH BS test – Results - FPGA

1. DAC1 to 450Gy
2. ASIC to 500Gy
3. **FPGA to 600Gy**
4. DAC1, DAC2, ADC to 700Gy
5. Analog switches to 200Gy
6. **FPGA**, DAC1, DAC2, ADC, Osc. **to 220Gy**
7. Analog switches to 600Gy

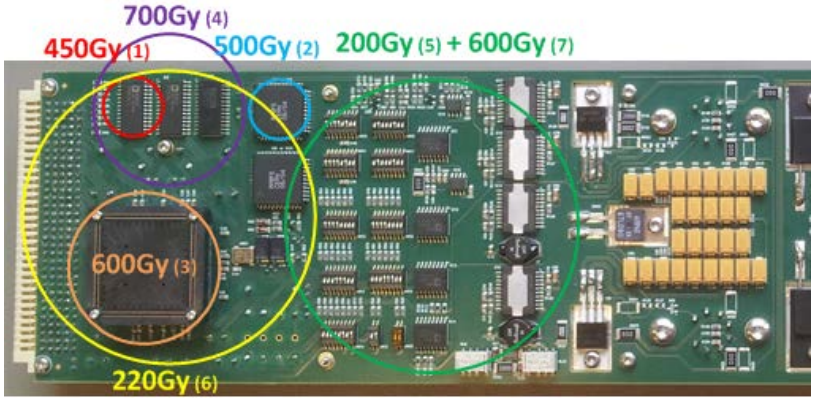




1. Gradual increase of FPGA current after 300Gy.
2. High annealing even after 30min to 230mA.
3. No SEU, drift, error appear during operation

EH BS test – Results – Analog Switch

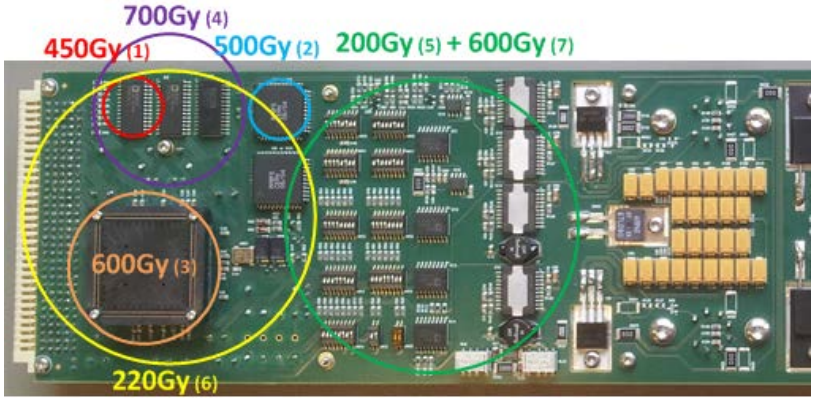
1. DAC1 to 450Gy
2. ASIC to 500Gy
3. FPGA to 600Gy
4. DAC1, DAC2, ADC to 700Gy
5. **Analog switches to 200Gy**
6. FPGA, DAC1, DAC2, ADC, Osc. to 220Gy
7. **Analog switches to 600Gy**

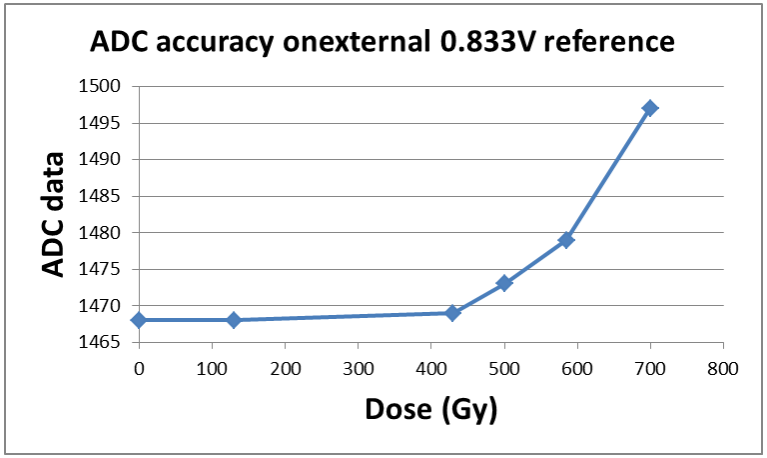


1. No drift, or accuracy change observable
2. No error in calculations or a protection triggered

EH BS test – Results - ADC

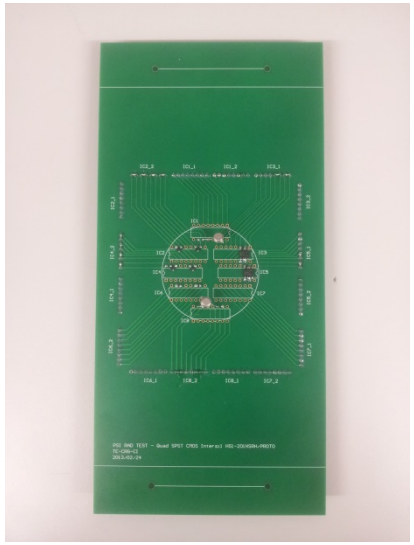
1. DAC1 to 450Gy
2. ASIC to 500Gy
3. FPGA to 600Gy
4. DAC1, DAC2, **ADC to 700Gy**
5. Analog switches to 200Gy
6. FPGA, DAC1, DAC2, ADC, Osc. to 220Gy
7. Analog switches to 600Gy



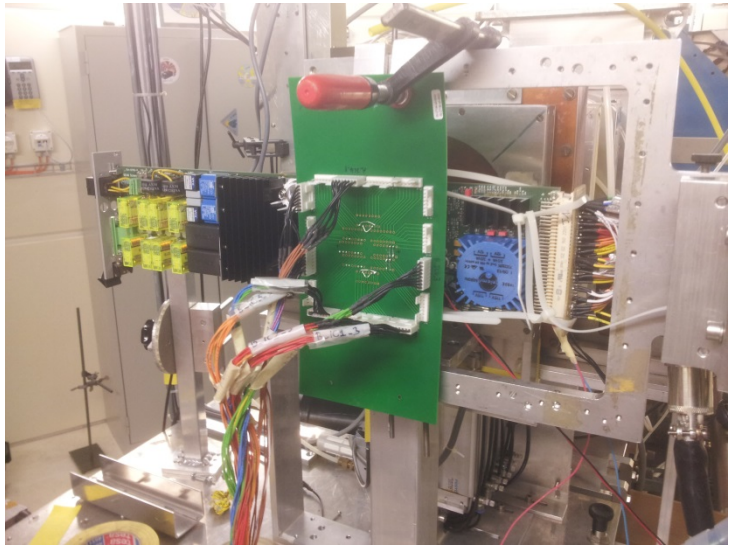


1. Inaccuracies after approx. 450Gy
2. At 700Gy error of 2%. 12h annealing reduced error to 0.48%
3. Error compensated by design (gain error compensation)

References test – Irradiation plan



Board #1 tested
directly on beam

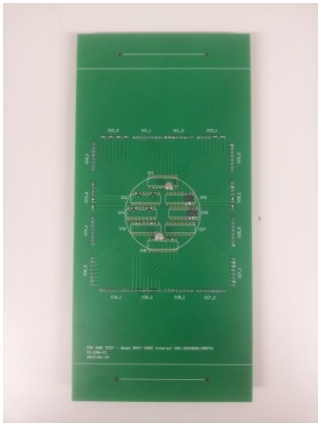


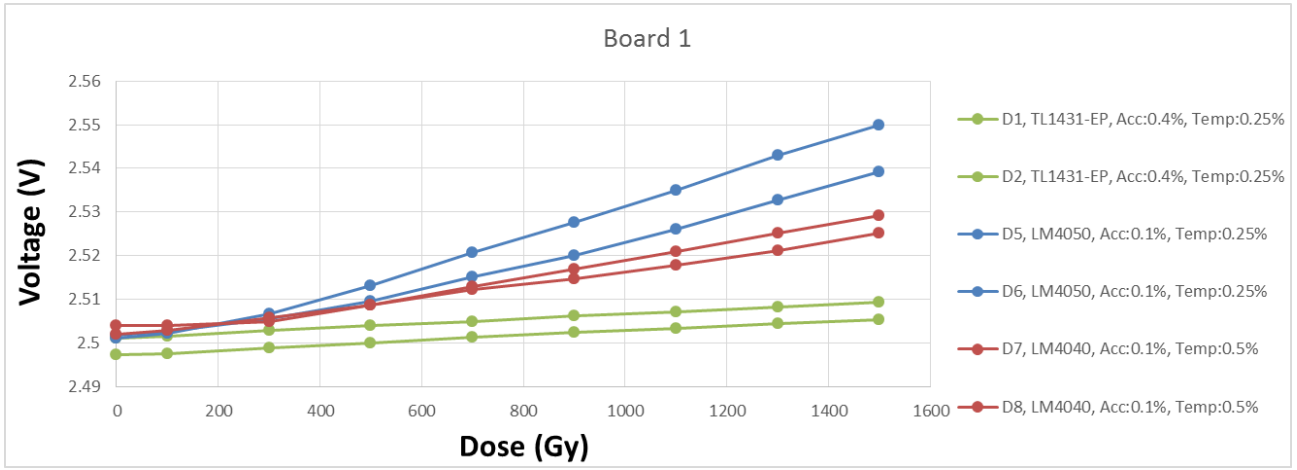
Board #2 tested
parasitically on beam

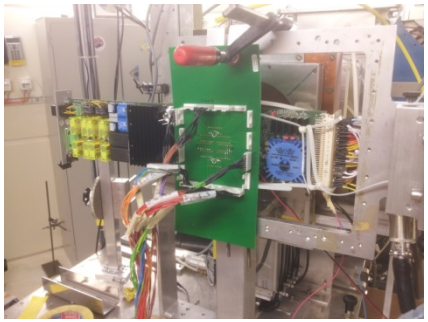
2 components of 4 different types per board

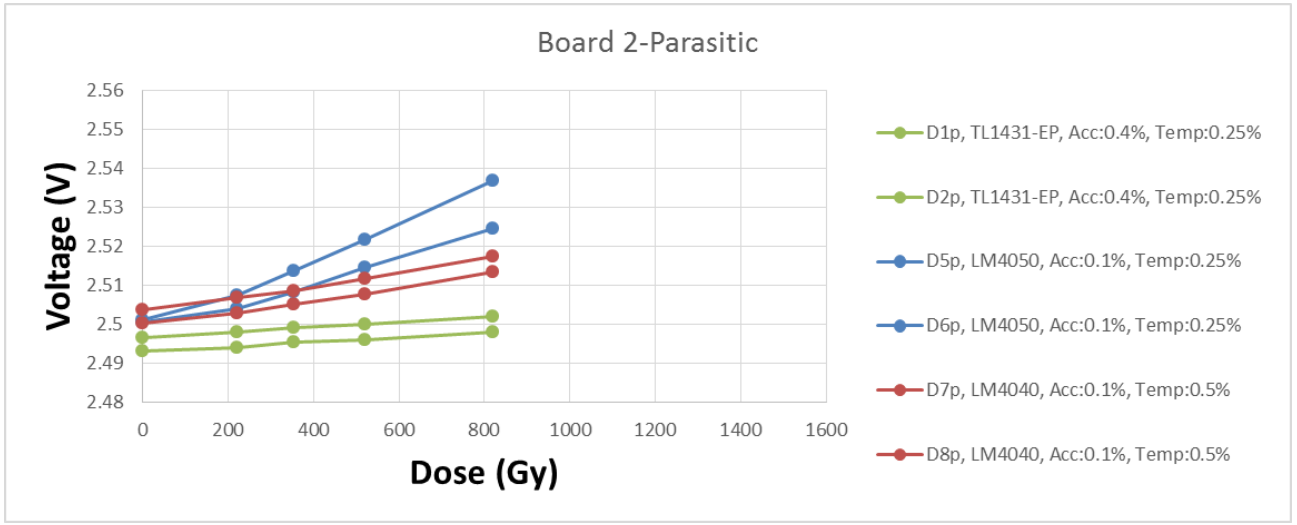
Tested on 2-4 NOV 2013

References test – Results









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