VMM Update
# Front End ASIC for the ATLAS Muon Upgrade

V. Polychronakos

BNL

Design Parameters/Features

- Dual Polarity
- Adjustable Gain (0.5 – 9.0 mV/fC)
- Adjustable peaking Time (25-200 ns)
- Address in Real Time (Fast OR in effect - Mmegas Trigger)
- Prompt digitized (6-bit) Amplitude, Time-over-threshold, time-to--peak (TGC Trigger)
- Peak Detector, Time Detector (<1 ns)
- Discriminators with sub-hysteresis
- Neighbor enable logic (channel to channel and across Ics)
- Sparse readout w/smart token passing,
- Threshold trim, built-in calibration, channel mask, analog monitor, temp. sensor, 600 BGR, 600 mV LVDS

VMM1, First Version, 64 channels, fully functional analog front end, Amp, Timing analog multiplexer outputs
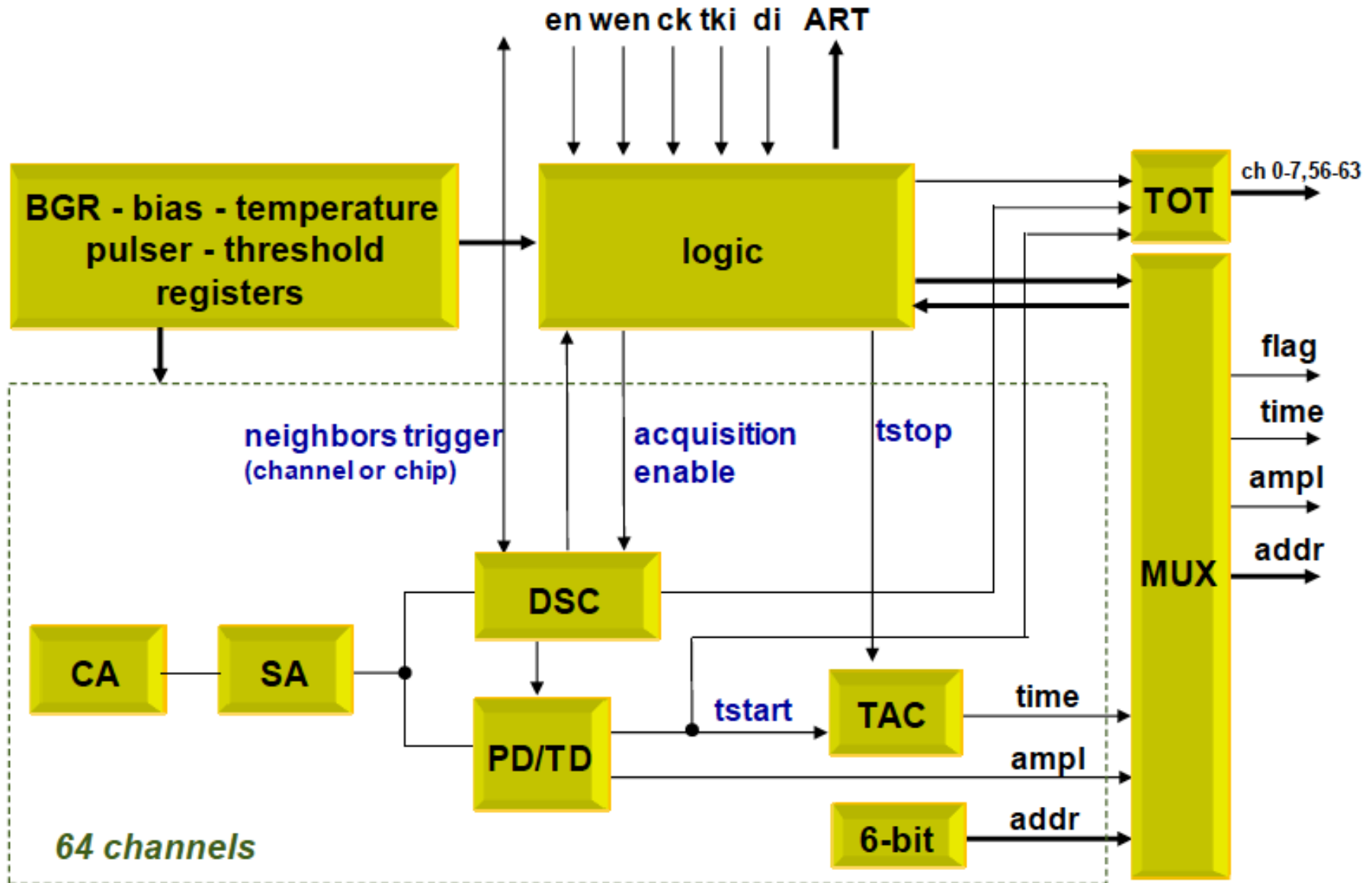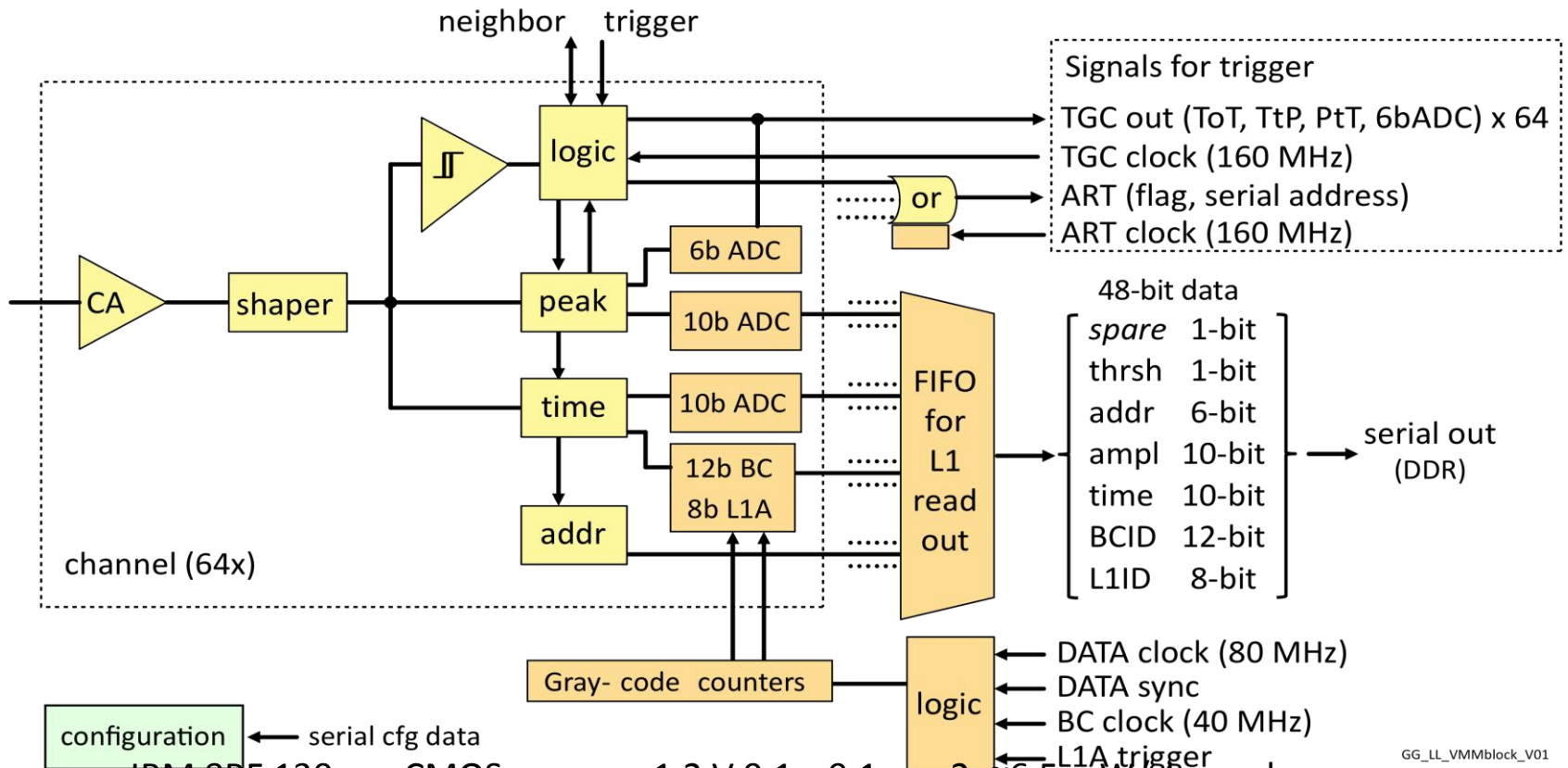
The Second version of the ASIC (VMM2)

- Fixes issues (mostly minor) of the first version
- Includes 10-bit digitizers for amplitude and timing (200 ns)
- Includes a 6-bit Amplitude digitizer at ~40 ns conversion time
- Includes 4 word buffer, simultaneous read/write, can continuously be read out at both phases of 200 MHz clock in DDR mode → 800 Mbps
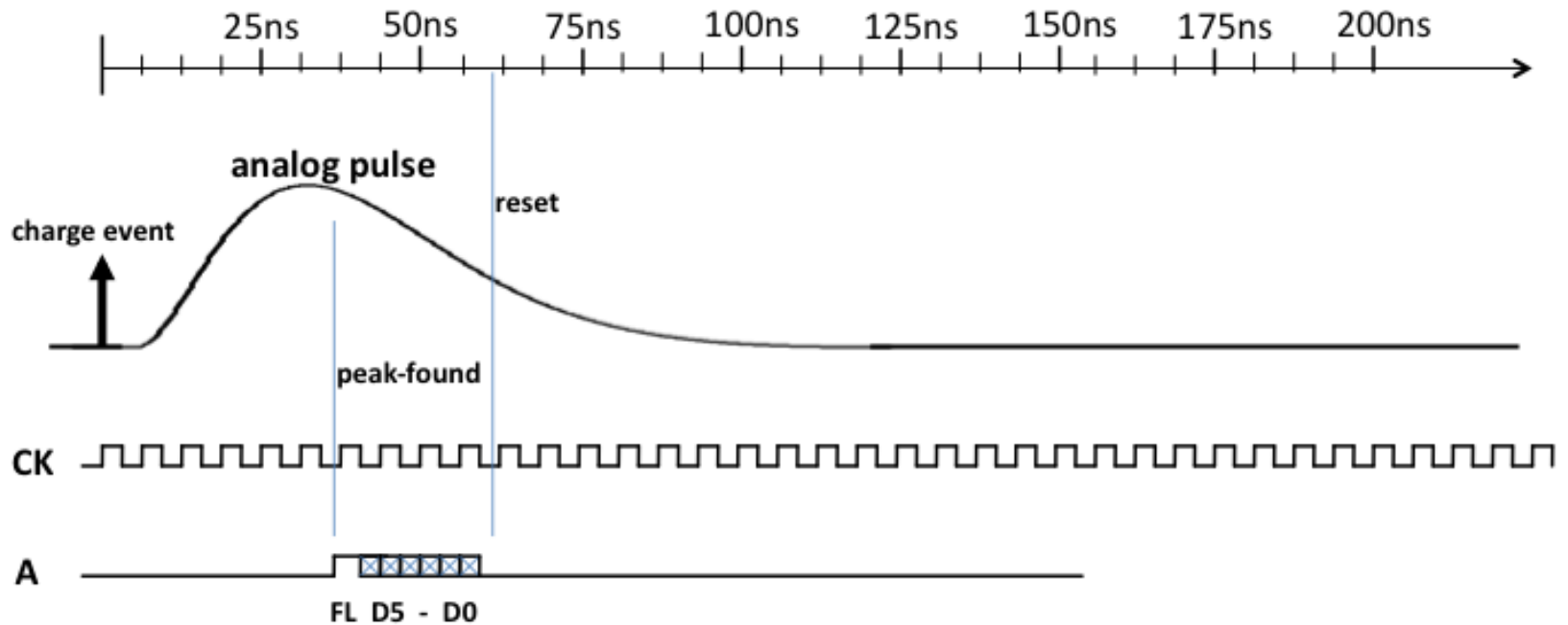
G. De Geronimo, BNL Instr. Div.

VMM Architecture

IBM 8RF 130 nm CMOS process, 1.2 V 9.1 x 9.1 mm2, ~6.5 mW/channel

VMM2 Readout
(May be modified in final version)

4-deep buffer

~~2-deep~~ buffer
Smart token moving
continuously from
1 word to next

160 MHz Clock

Companion ASIC

Readout
Control

SYNC

VMM

Ch.3

Ch.35

Ch.62

FLAG+D0

D1

DDR Readout

200 MHz Clock
Uses both phases
Effectively 800 Mbps

Deserializer

Ch
ID

Router
Control

CAM

FIFO−50 Deep

channel 0

channel 1

48−bits

channel 63

Token Advances by Clock until FLAG detected

Check FLAG, if 1 send SYNC, read next word

SYNC

Read last (48th) bit

Drop of SYNC advances Token

Clock

SYNC

Data Ch. 3   Data Ch. 62   Data Ch.35   Data

Trigger Feature 1- Address in Real Time (ART)

VMM1 ART SERIALIZER - v2
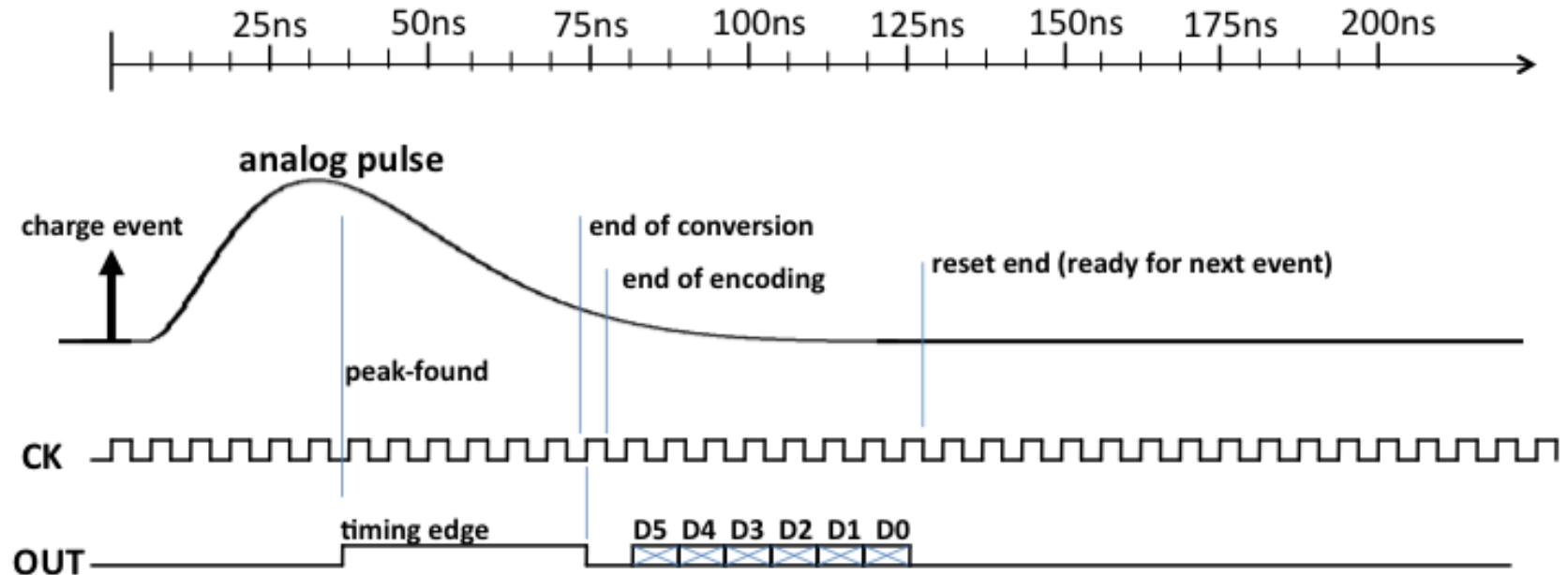

Assumes 160 MHz clock provided externally
ART serialized in one line A
Data D5-D0 shifted at each clock edge
LVDS 600mV +/- 150mV

At every bunch crossing ART provides the 6-bit address of the channel with the earliest signal above threshold

Can be used as a fast OR

Trigger Feature 2- Prompt 6-bit amplitude per Channel

VMM1 FAST DIGITIZER PER CHANNEL

Assumes 160 MHz clock provided externally
Conversion starts at pulse, ends ~50ns after peak
Dead time from charge event ~125ns
LVDS 600mV +/- 150mV

Summary, Schedule - Availability

- VMM2 design completed about a month ago
- Layout, simulations in progress, expect to be completed end of November (next MOSIS MPW run)
- VMM is a very large chip (~ 100 sq.mm), cost 230 k$US/40 samples!
- Decided to go for a dedicated run (450 k$US) sharing the wafer with a smaller BNL ASIC which will reduce the cost by ~ 100 k
- The cost above includes processing of 6 wafers, ~800-1000 chips
- Chips available ~May 2014 if submitted in early December
- Package in BGA 350 pins (21x21 mm2)
- In the process of applying for Commerce Department export license
- What remains for the final version is SEU mitigation logic and final decision on digital buffer size and management
- Several Readout boards for ATLAS under development, SRS compatible hybrid under discussion