Mini-2 and MMFE-8 Status at U. Arizona

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Overview

- AZ cards under development
  - Mini-2: MM front-end board for VMM2 **bench evaluation** and **for lab use with MM test chambers** with **Panasonic connectors**
  - MMFE-8: Demonstrator (V0) MM front-end board for MM NSW chambers with **Zebra connectors** (and S6 FPGA for "Companion ASIC")
  - FMC-S6: FMC card for GLIB board for readout of the Mini-2 (and possibly MMFE-8)
- Little progress on Mini-2 and MMFE-8 pending VMM2 pinout (available 1/15/14)
- BNL does not endorse the AZ development, preferring to use BNL DAQ board a la VMM1
  - Hope for convergence at the MM electronics meeting next week

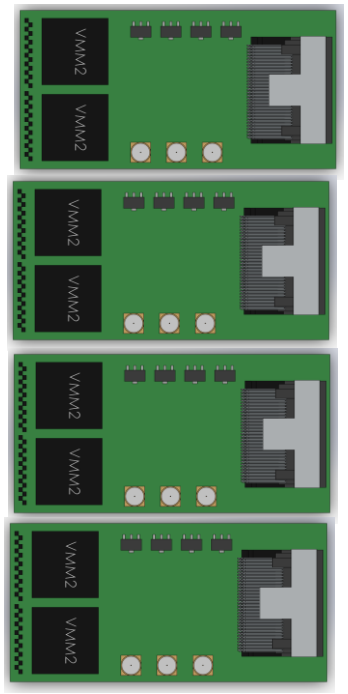
Philosophy

- There will be significant pressure to validate VMM2 and MMFE-8 as soon as VMM2 becomes available
- Our priorities
  - **Simple** front-end board (Mini-2) to test VMM2 shortly after they are available
  - Demonstrator MMFE-8 for full size MM's ready soon thereafter (see schedule)
- Long-term issues
  - MMFE-8 Companion ASIC
  - To SCA or not to SCA

Readout of Mini-2

The Spartan 6 on the S6-FMC is used to translate voltage levels to/from VMM

The AD7298 or ADS5281 (plus FMC adapter) is used to digitize analog VMM data



4 x Mini-2, each containing 2 VMM ASICs

4 x miniSAS cables and 16x SMA cables

GbE out (UDP packets) to MATLAB

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The Virtex 6 contains the logic to configure and readout the VMM

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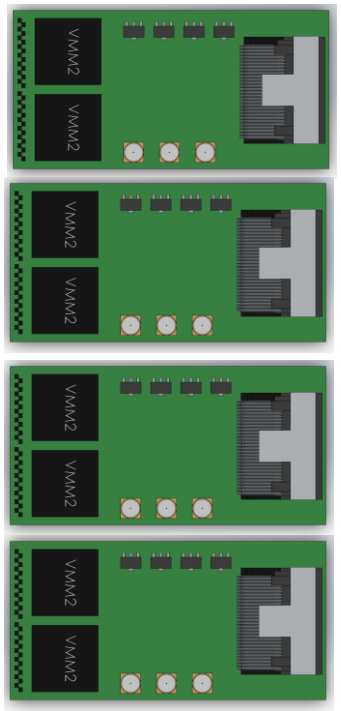

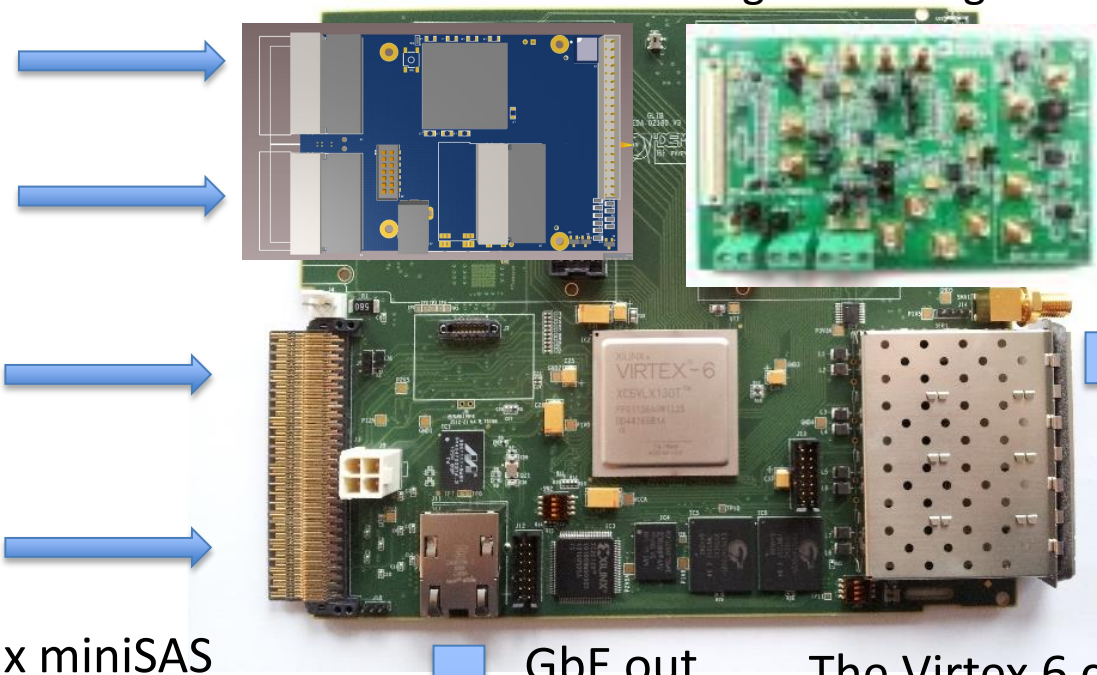

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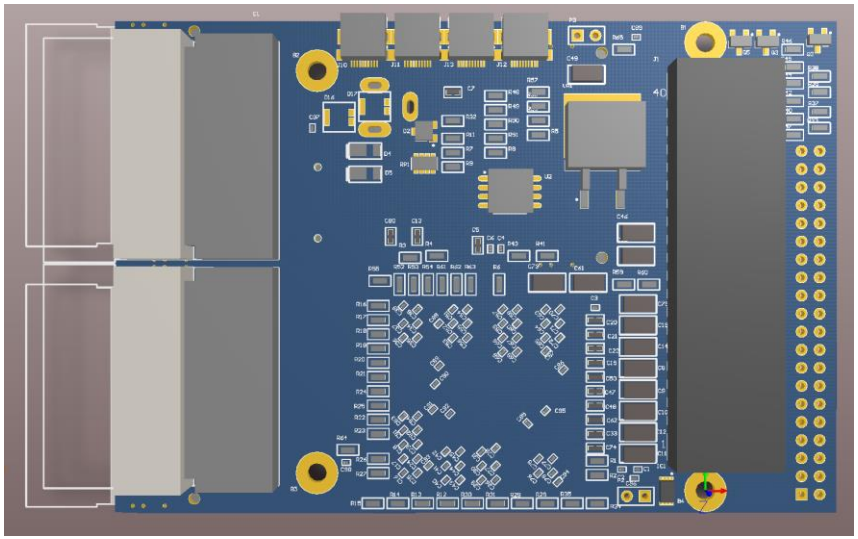
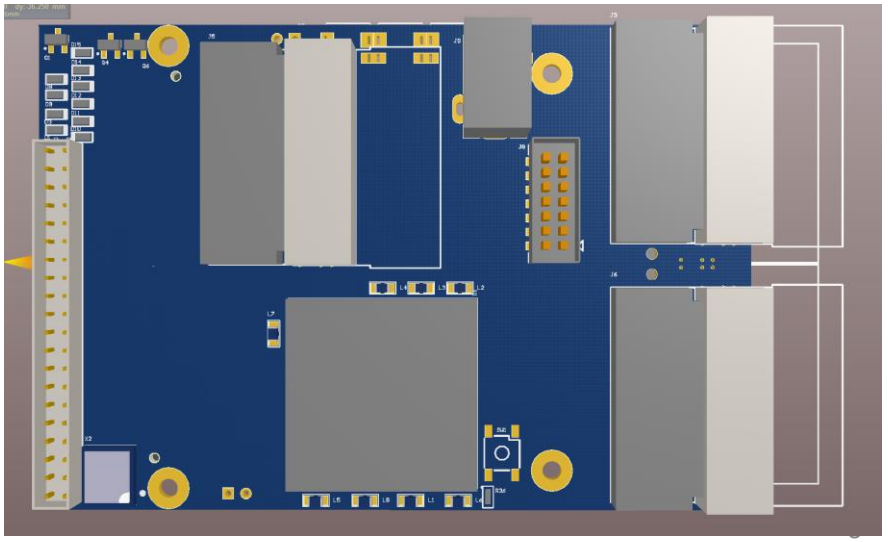
S6-FMC Status

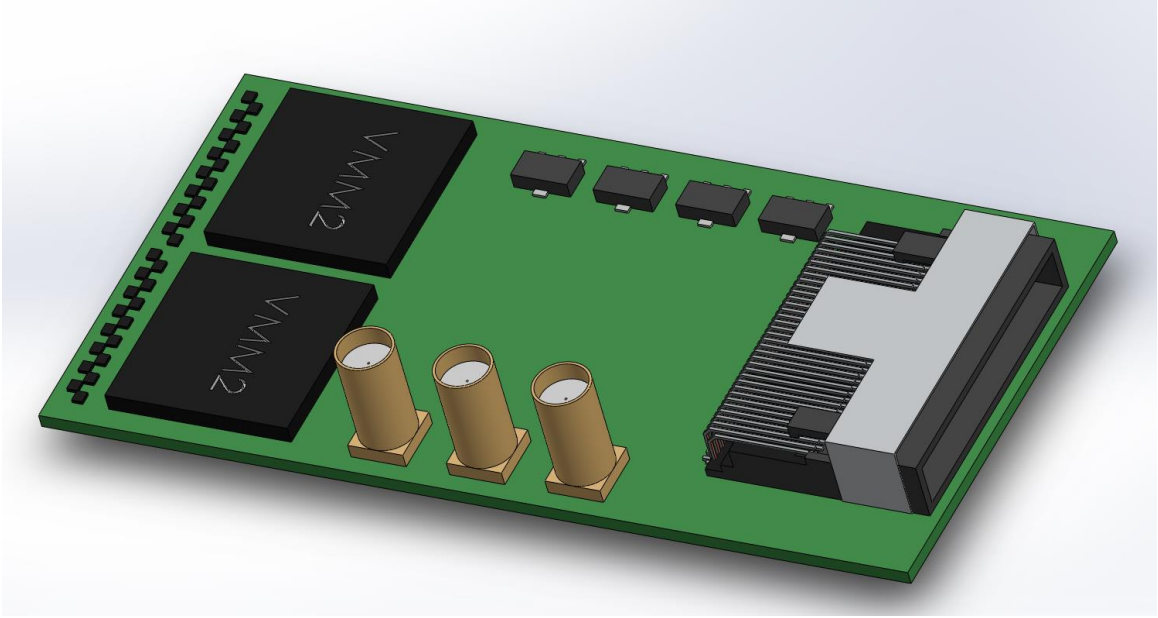
- Final checking before layout
  - Spartan 6 used for voltage translation to/from VMM
  - Fifth mini-SAS connector can be used as output for MM trigger processor (with second S6-FMC)





Mini-2 Status

- Schematic pending VMM details, instead will focus on RO firmware
- Approximate size < 50mm x 100mm



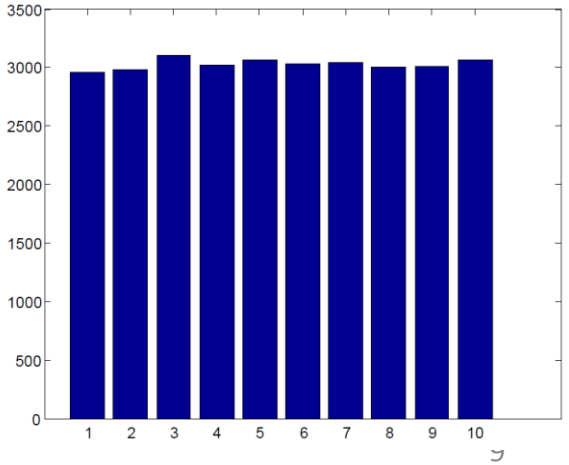
ADC-FMC Status

- Order on hold pending discussions with BNL
  - 1 MSPS, 12-bit SAR
  - 8 channels
  - Serial data out
  - Uses FMC adapter card to made with GLIB or Xilinx evaluation board
  - 50 MSPS ADC also available

Readout Software for Mini-2

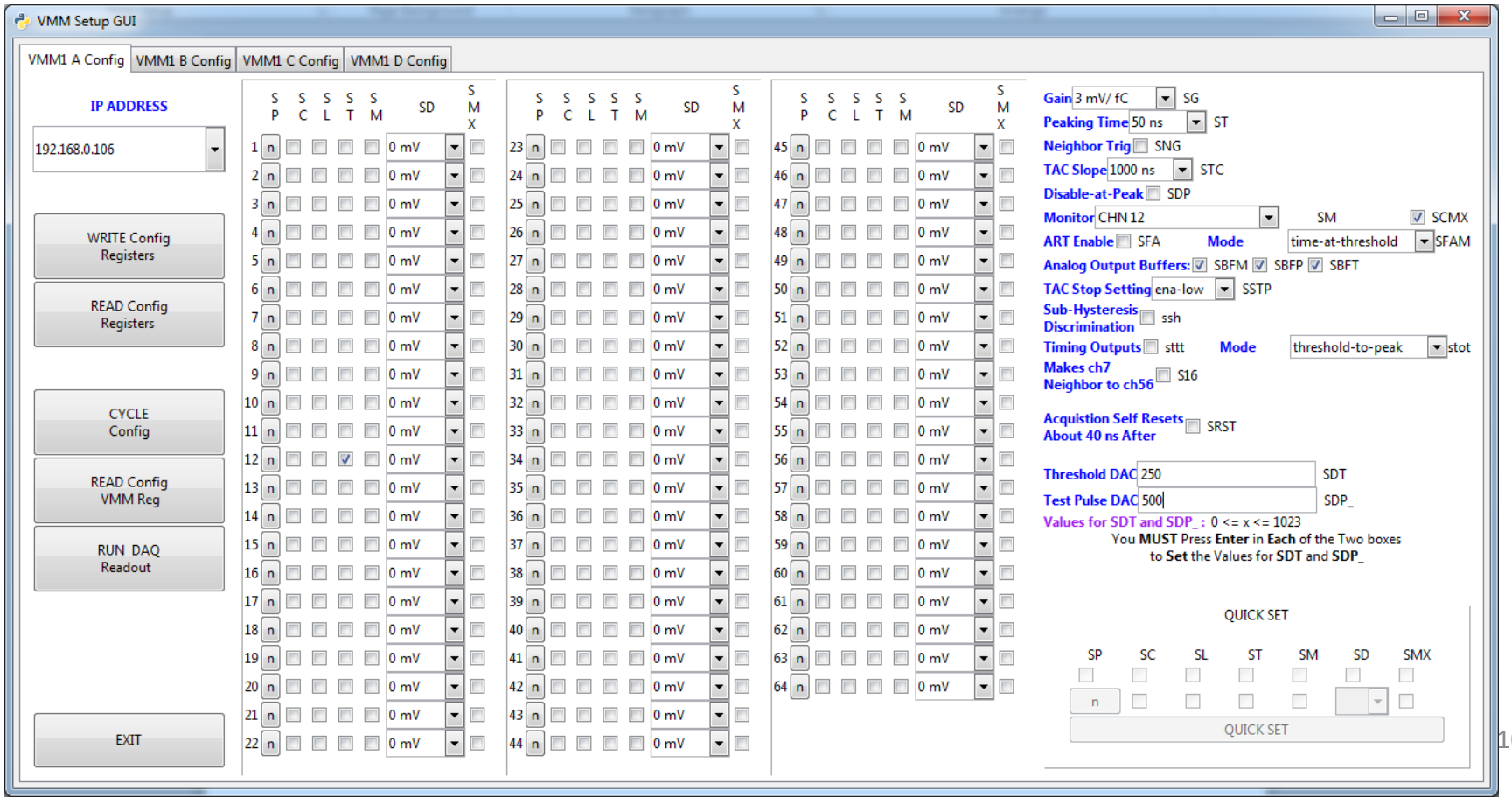
- One can use Xilinx V7 or K7 boards in place of the GLIB (V6)
- Ouput data are UDP packets over GbE
- Readout software options
  - MATLAB (AZ)
  - QT (G. Iakovidis/NTUA)
  - LabVIEW (BNL?)

- Figure on right shows simple accumulating histogram from UDP data in MATLAB



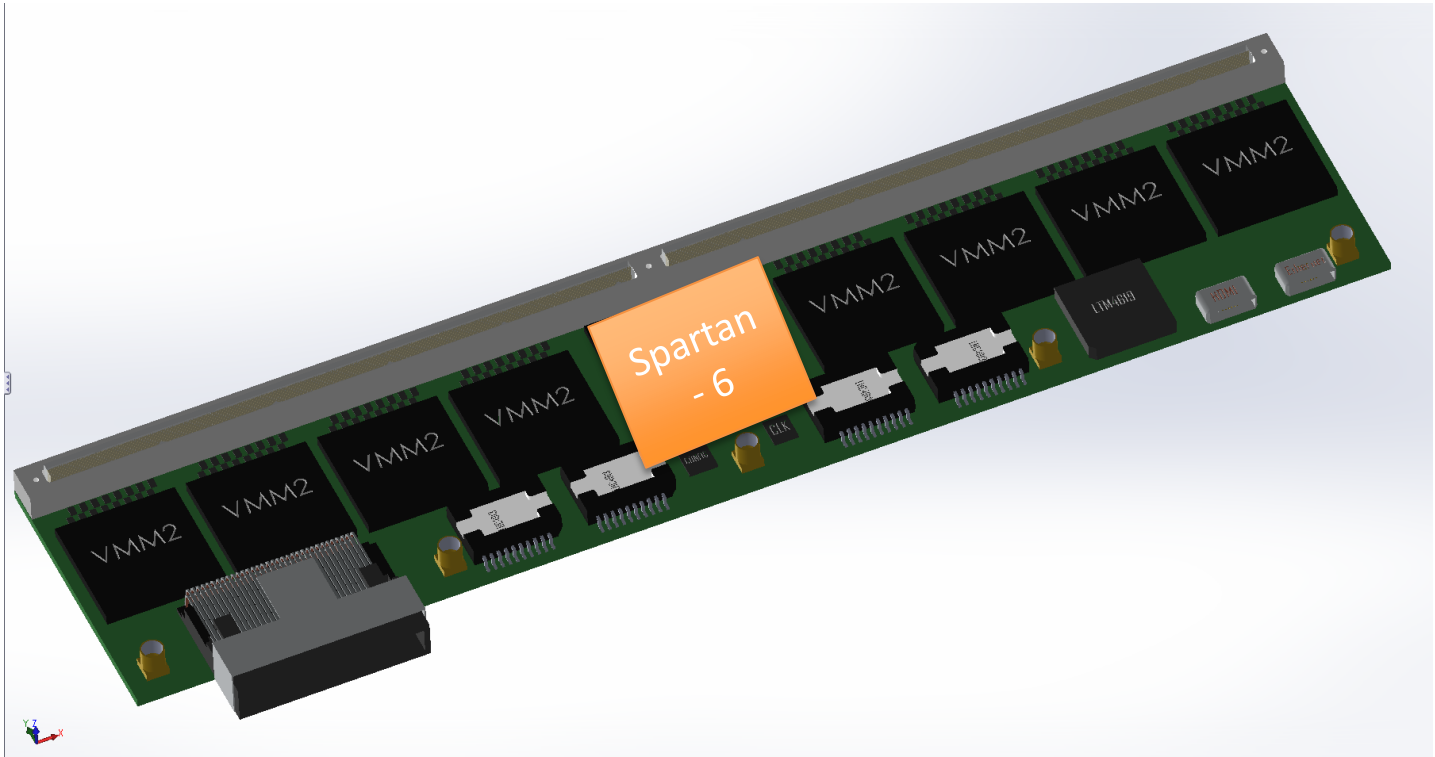
Readout Software for Mini-2

- Configuration is via Python GTK gui whose output is read by MATLAB



MMFE-8 (Demonstrator) Status

- Schematic pending VMM details
- Readout schemes are still evolving – UDP out over GbE using GLIB (or equivalent) or standalone are baseline schemes



Present AZ Schedule

- Apr 2014 – Mini-2 ready for assembly with VMM2
- Jul 2014 – Demo MMFE-8 (FPGA) ready for initial assembly with VMM2
- July 2015 – Prototype MMFE-8 (ASIC) ready for initial assembly VMM
  - Date driven by companion ASIC !!
  - Date driven by companion SCA (and prior understanding)?

Conclusions

- We presented the status of the AZ Mini-2 and MMFE-8 demonstrator boards
- We presented the readout scheme (data) for the Mini-2
  - Simple Mini-2 using COTS ADC
  - Based on GLIB or Xilinx evaluation boards for configuration and readout
  - Simple software (MATLAB) into a host PC
- This results in an efficient system that can be used for bench-testing or MM test chamber evaluation in the lab
  - More discussions to follow next week at the MM electronics workshop