2nd CERN Advanced Performance Tuning workshop

Report of Contributions

https://indico.cern.ch/e/280897

Contribution ID: **1** Type: **not specified**

Introduction

Thursday 21 November 2013 09:00 (30 minutes)

Presenter: NOWAK, Andrzej (CERN openlab)

Session Classification: Talks

Contribution ID: **2** Type: **not specified**

Physics Software and Tuning Challenges + Discussion

Thursday 21 November 2013 09:30 (45 minutes)

Presenter: INNOCENTE, Vincenzo (CERN)

Session Classification: Talks

Contribution ID: **3** Type: **not specified**

An update on perf_events

Thursday 21 November 2013 10:45 (30 minutes)

In this talk, we give an overview of the latest developmements in the Linux kernel performance monitoring interface, perf_events, and related tools, such as perf. In particular, we describe load/store sampling support, event grouping, multi event profiling, Energy consumption, uncore counters, Haswell processor support.

Presenter: ERANIAN, Stephane (Google)

Session Classification: Talks

Contribution ID: **4** Type: **not specified**

Improving perf_events measurement correctness

Thursday 21 November 2013 11:15 (10 minutes)

In this presentation, we talk about a correctness issue in the Performance Monitoring Unit (PMU) of recent Intel processors with Hyperthreading enabled. This issue introduces cross-threading corruption when hyperthreads measure incompatible events on sibling counters. As such, certain event combinations may produce unreliable results. We present an innovative approach to avoid the problem by introducing cross-thread dynamic event scheduling. We conclude with the implemented protocol's results and the challenges it raises.

Presenter: DIMAKOPOULOU, Maria (Google)

Session Classification: Talks

Contribution ID: **5** Type: **not specified**

RAS and memory error reporting with perf

Thursday 21 November 2013 11:25 (30 minutes)

Strategies for RAS (Reliability, availability and serviceability) are necessary for enterprise systems in order to increase data integrity and system uptime. The current implementations in the Linux kernel to collect hardware errors are architecture dependent or even vendor specific. In order to unify hardware error reporting over architectures a new approach is needed. The talk shows how the perf event subsystem can be used for this. It also gives details about perf persistent events that keep running in the system after the creating process terminated.

Presenter: RICHTER, Robert (Calxeda)

Session Classification: Talks

Contribution ID: **6** Type: **not specified**

AMD IBS and northbridge counters in perf

Thursday 21 November 2013 11:55 (15 minutes)

Presenter: RICHTER, Robert (Calxeda)

Session Classification: Talks

Contribution ID: **7** Type: **not specified**

MAQAO: an analysis and optimization toolchain

Thursday 21 November 2013 14:00 (30 minutes)

MAQAO (Modular Assembly Quality Analyzer and Optimizer) analyzes binary codes and provides application developers with reports to optimize their code. The tool mixes both static code quality evaluation, and dynamic profiling and characterization. This is based on the ability to reconstruct low-level and high-level structures, such as basic blocks, loops, functions, and call-sites. Another main feature of MAQAO is its extensibility. Users can easily write their own plug-ins, using the embedded scripting language Lua. It allows fast prototyping of new tools based on MAQAO. We will present the three currently released modules. The first one is the profiler module (PERFEVAL) which aim is to detect function and loop hotspots. The second one is the code quality analyzer tool (CQA) which evaluates the code generated by a given compiler. Finally, we will present MIL, our binary instrumentation language.

Presenter: CHARIF-RUBIAL, Andres S. (Exascale Computing Research Laboratory, Versailles)

Session Classification: Talks

Contribution ID: **8** Type: **not specified**

Intel VTune Amplifier: A Bridge to Performance, Parallelism, and Power (introduction to hardware collection)

Thursday 21 November 2013 14:30 (20 minutes)

We're going to present Intel VTune Amplifier XE as Intel's flagship performance analysis product and focus on a few aspects of HW-assisted SW analysis, including performance, power and threading efficiency, in the example of an N-body application run on both CPU and GPU. Additionally, in the process of our case study we will identify opportunities for further improvement of the tool and will ask the audience to share their opinions. CPU analysis is expected to be covered in the talk, while the GPU side will be left for offline studying because of time constraints.

Presenter: BRATANOV, Stas (Intel)

Session Classification: Talks

Contribution ID: **9** Type: **not specified**

Top Down Analysis –Never Lost With Perf Counters

Thursday 21 November 2013 14:50 (40 minutes)

Optimizing an application's performance for a given microarchitecture has become painfully difficult. Increasing microarchitecture complexity, workload diversity, and the unmanageable volume of data produced by performance tools increase the optimization challenges. At the same time resource and time constraints get tougher with recently emerged segments. This calls for accurate and prompt analysis methods, adding further to the difficulty.

Top-Down Analysis is a practical method to quickly identify true bottlenecks in out-of-order processors. The presented method uses designated performance counters in a structured hierarchical approach in order to quickly and, more importantly, correctly identify dominant performance bottlenecks. The developed method is adopted by multiple in-production tools including VTune. Feedback from VTune average users suggests that the analysis is made easier thanks to the simplified hierarchy which avoids the high-learning curve associated with microarchitecture details. Characterization results of this method are reported for the SPEC CPU2006 benchmarks as well as key enterprise workloads. We will walk through field case studies where the method guides field software optimizations, in addition to architectural exploration study for most recent generations of Intel Core products.

Presenter: YASIN, Ahmad (Intel)

Session Classification: Talks

Contribution ID: **10** Type: **not specified**

Intel Architecture and GOODA

Friday 22 November 2013 08:00 (1h 30m)

Presenter: LEVINTHAL, David (Google)

Session Classification: Talks

Contribution ID: **11** Type: **not specified**

ARM in the server space

Friday 22 November 2013 10:00 (15 minutes)

Presenter: RICHTER, Robert (Calxeda)

Session Classification: Talks

Contribution ID: **12** Type: **not specified**

Introduction to ARMv8

Friday 22 November 2013 10:15 (20 minutes)

ARM business model of designing and licensing low-power IP building blocks has been phenomenally successful in transforming the mobile industry. The introduction of the ARMv8 architecture opens up low-power 64-bit computing in the same way. This talk will introduce the ARMv8 architecture and describe the debug and performance monitoring capabilities baked into it. It will give an opportunity to learn more about ARM and ARMv8.

Presenter: WILLIAMS, Michael (ARM)

Session Classification: Talks

Contribution ID: **13** Type: **not specified**

Utilizing Performance Bottleneck Analyzer to Debug Issues on Intel's Future SOCs

Friday 22 November 2013 10:55 (45 minutes)

The presentation will cover the methodologies of the PBA (Performance Bottleneck Analyzer) toolset which has been maintained by Intel engineers for 7+ years to analyze workloads on future architectures. Using examples from software vendors we will show how PBA was able to find and fix issues that could not be identified with any other methodology or toolset on Intel's future SOCs. PBA recreates very long flows of execution on the processor and then combines knowledge of processor events, power state and static assembly analysis to find and prioritize bottlenecks on Intel's latest architectures. Filters are then applied to the data set to better call out issues that are impacting user experience, power or slow transactions to ensure the developer concentrates on the right issues to fix their problem. We will also showcase all of the functionalities using field examples from major software vendors. The talk will focus on how the collaborative framework has been used to share methodologies across multiple software vendor accounts and disciplines. We will also focus on some new capabilities allowing us to collect more performance monitoring data for less overhead than previously realized and syncing the run with multiple types of media.

Presenter: CHYNOWETH, Michael W (Intel)

Session Classification: Talks

Contribution ID: **14** Type: **not specified**

Software profiling on ARM

Friday 22 November 2013 10:35 (20 minutes)

This presentation will give a brief overview of ARM's software profiling tools. This will mainly cover the Streamline tool for sampling-based profiling and software instrumentation, but also look at hardware trace.

Presenter: GRANT, Al (ARM)

Session Classification: Talks