Consequences of 1MHz, 20us trigger on pixel detector

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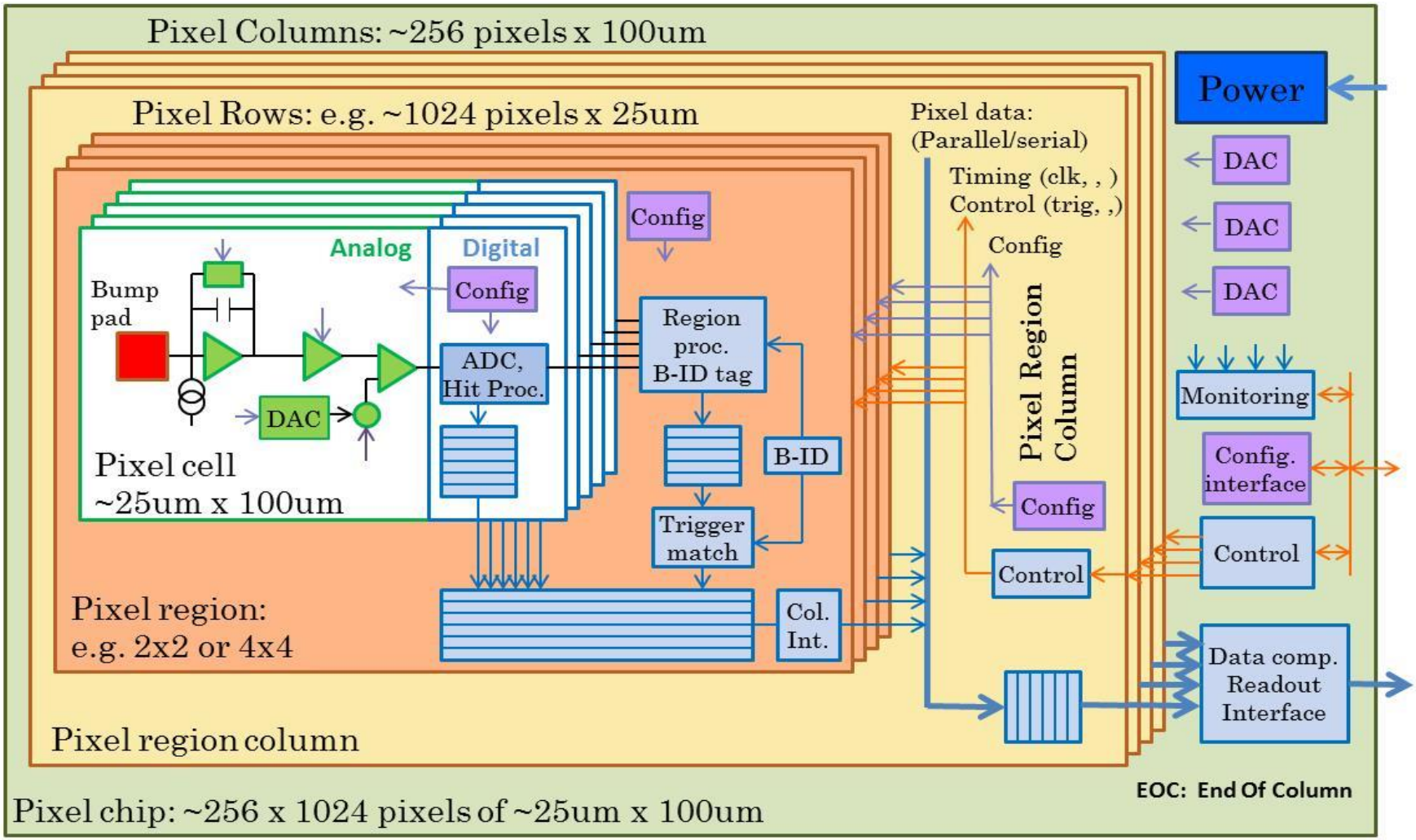
Basic CMS HL-LHC assumptions

- Cluster size: ~4 (average)
  - Cluster size and shape varies significantly over pixel detector:
    - Middle barrel, End barrel, End cap disks, Tracks from collision point, Machine background/halo, Loopers, monsters, etc.
  - Depends on sensor type, thickness and radiation damage.
- Rate: Worst case HL-LHC (layer locations as in Phase1)
  - **Layer 1** (3.0cm): ~500MHz/cm^2 tracks -> **~2GHz/cm^2 hits (TBC)**
  - Layer2 (6.8cm): **~½** of layer 1
  - Layer3 (10.2cm): ~½ of layer 2 -> **~¼** of layer 1
  - **Layer4** 16.0cm) : ~½ of layer 3 -> **~1/10 of layer 1** (50MHz/cm^2 tracks, 200MHz/cm^2 hits)
  - End-cap disks ?.
- Pixel size: ~25x100um = 2500um^2
  - Or 50um x 50um (same area but square)
  - (50um x 100um if more area required per pixel, No major effect on readout rate)
- Pixel chip: ~6.5 cm^2 , ~256k pixels, Pixel Regions (PR): 4 x 4 or 2 x 2
- Tracks/hits per Readout Out Chip (ROC) per Bx:
  - **Layer 1**: 50KHz/pixel, 75 tracks/ROC/Bx, **300hits/ROC/Bx**
  - **Layer 4**: 5KHz/pixel, 7.5 tracks/ROC/Bx, **30hits/ROC/Bx**
- L1 Trigger: 1MHz (500KHz), 20us (10us)

General pixel (chip) architecture



- Pixels: ~256k, Chip size = ~2.6cm x ~3cm
- ~1G transistors, ~3Watt

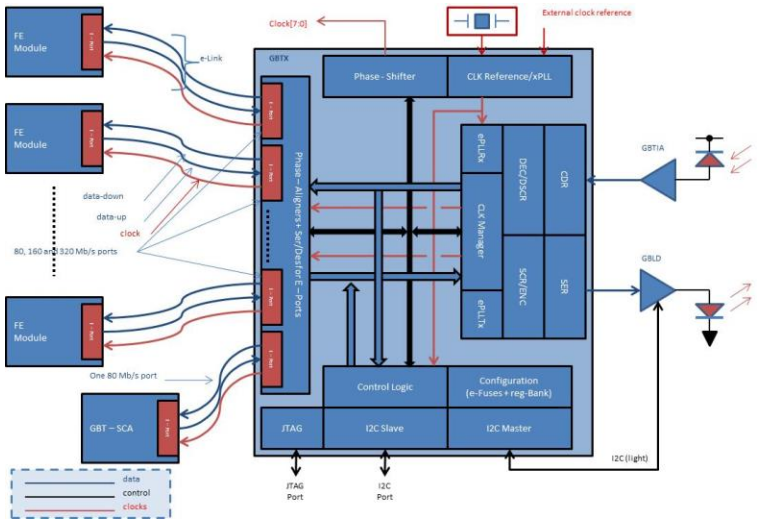
Readout rate and data formatting

- Readout link bandwidth depends on many aspects.
  - Hit rates, Trigger rates, Required data (e.g. 4b ADC), Readout format, Use of Pixel Regions (PR), Clustering approach (extraction).
- Not (yet) using readout re-formatting across Pixel Regions.
  - Data reduction: 10-20%
- Not (yet) on-chip track position extraction: Cluster center
  - Requires intelligence in EOC: Correlate date from different pixel columns
  - Handling of "strange"/broken clusters
  - Data reduction: 25% - 50%
  - Keep this option as a possible "safety factor" for the future.
- Readout formatting: As function of pixel region and data
  - Event header: 32 bit event header (12b B-ID , 12b E-ID, 8b diverse))
  - 1 x 1 Binary Binary: 18bit pixel address = 18bit
  - 1 x 1 TOT: 18bit address + 4bit TOT = 22bit
  - 2 x 2 Binary: 16bit PR address + 4bit hit map = 20bit
  - 2 x 2 4 TOT: 16bit PR address + 4 x 4bit TOT = 32bit
  - **2 x 2 1-4 TOT** 16bit PR address, 4b hit map, 1-4 4b TOT = **24 – 36bit**
  - 4 x 4 Binary 14bit PR address, 16b hit map = 30bit
  - 4 x 4 16 TOT 14bit PR address, 16 x 4 bit TOT = 78bit
  - **4 x 4 hit map, 1-16 TOT** **14bit PR address, 16b hit map, 1-16 4bit TOT: 34 – 95bit**
  - 4 x 4 1-16 Adr + TOT 14bit PR address, 1 – 16 4bit adr + 4bit TOT: 22 – 142 bit
  - Track extraction: 18bit center pixel adr, 3+3 bit interpolation, 8 bit charge = 32

LP-GBT: OPTICAL LINK INTERFACE CHIP

- LP-GBT user bandwidth 2xGBT: ~6.4Gbits/s
  - Single and multiple bit error correction
  - **5 E-links @ 1.2Gbits/s**
  - 10 E-links @ 640Mbits/s
  - 20 E-links @ 320Mbits/s
  - 40 E-links @ 160Mbits/s
- What if ~10Gbits/s user bandwidth (No data protection)
  - (4 E-links @ 2.4Gbits/s)
  - **8 E-links @ 1.2Gbits/s**
  - 16 E-links @ 640Mbits/s

  We do not care about a few corrupted hits (noise) as long as event sync not lost.

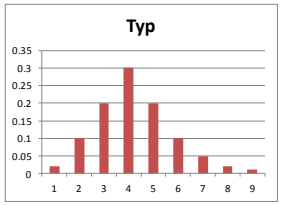


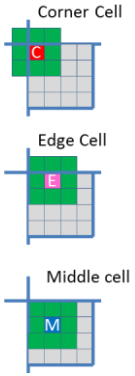
- E-links at 1.2Gbits/s
  - Feasible on 2-10m low mass electrical links
    - Cable: Alu/copper micro coax or twisted pair, Alu capton flat cable, ?
    - Limited complexity cable driver/receiver
    - Feasible with limited power in 65nm and very high radiation
  - Enables very nice readout/system flexibility.
  - Also appropriate if link chip on module (local on module connections)

  Gain of using higher speed E-links ?
- Assumption: Opto part not on pixel module (radiation, size)

READOUT OF INNER BARREL LAYER @1MHZ

- **Inner layer: Hit rate 2GHz/cm², 1MHz trigger**
- Data rates calculated with simplified statistical model
  - Generic cluster size distribution
  - Pixel Region organization
- First conclusions
  - **~1 LP-GBT (6.4Gbits/s) required per pixel chip for layer 1**
  - ~30% reduction if only Binary
  - ~30% effect of encoding and PR when having TOT/ADC
  - ~50% reduction possible using on-chip track position extraction





	PRs/trg/chip	Bits/trg/chip	Data rate	Chips/link
1x1 Bin	3.46E+02	6.25E+03	6.25E+09	1.02
1x1 TOT	3.46E+02	7.64E+03	7.64E+09	0.84
2x2 Bin	2.21E+02	4.45E+03	4.45E+09	1.44
2x2 4 TOT	2.21E+02	7.09E+03	7.09E+09	0.90
2x2 1-4 TOT	2.21E+02	5.83E+03	5.83E+09	**1.10**
4x4 Bin	1.48E+02	4.45E+03	4.45E+09	1.44
(4x4 16 TOT)	(1.48E+02)	(1.16E+04)	(1.16E+10)	(0.55)
4x4 1-16 TOT	1.48E+02	4.88E+03	4.88E+09	**1.31**
4x4 hitmap, 1-16 TOT	1.48E+02	5.87E+03	5.87E+09	1.09
Track extraction	8.19E+01	2.65E+03	2.65E+09	**2.41**

Opto links per pixel module

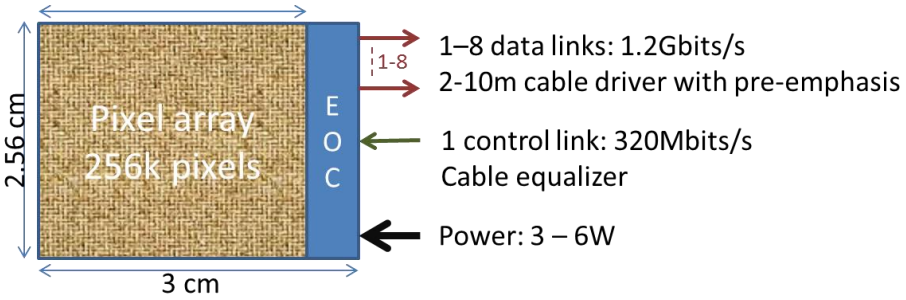
- 1MHz trigger rate
- Opto link rate: 6.4 Gbits/s with multi bit corrections (needed ?)
  - Module types
    A. *Layer 1-2 : 4 pixel chips with 2 – 4 LPGBT links*
    B. *Layer 3-4: 8 pixel chips with 1 - 2 LPGBT links*
- **If ~10Gbits/s link: (links per module)**
  Module type A (inner layers, 4 ROCs) needs 1-2 links
  Module type B (outer layers, 8 ROCs) needs 1-2 links

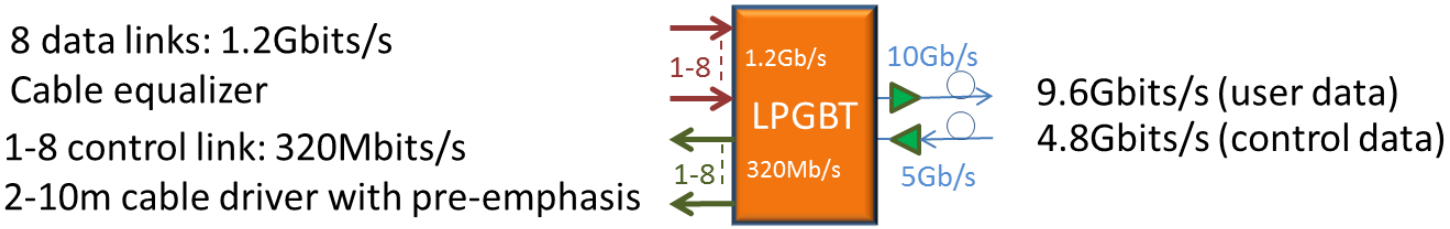
End cap disks can most likely be made of module type B (or a possible C type ?)

	2 x 2 1-4 TOT		4 x 4 1-16 TOT		Cluster interpol.		Module	
Layer	Chip rate	Chips per link	Chip rate	Chips per link	Chip rate	Chips per link	Chips per module	Links per module
1	5.83E+09	1.10	4.88E+09	**1.31**	2.65E+09	2.41	4	4 (2)
2	2.93E+09	2.18	2.45E+09	**2.61**	1.34E+09	4.77	4	2 (1)
3	1.48E+09	4.32	1.24E+09	**5.15**	6.87E+08	9.31	8	2 (1-2)
4	6.12E+08	10.46	5.16E+08	**12.40**	2.94E+08	21.76	8	1 (1)

PIXEL MODULES FOR 1MHZ TRIGGER

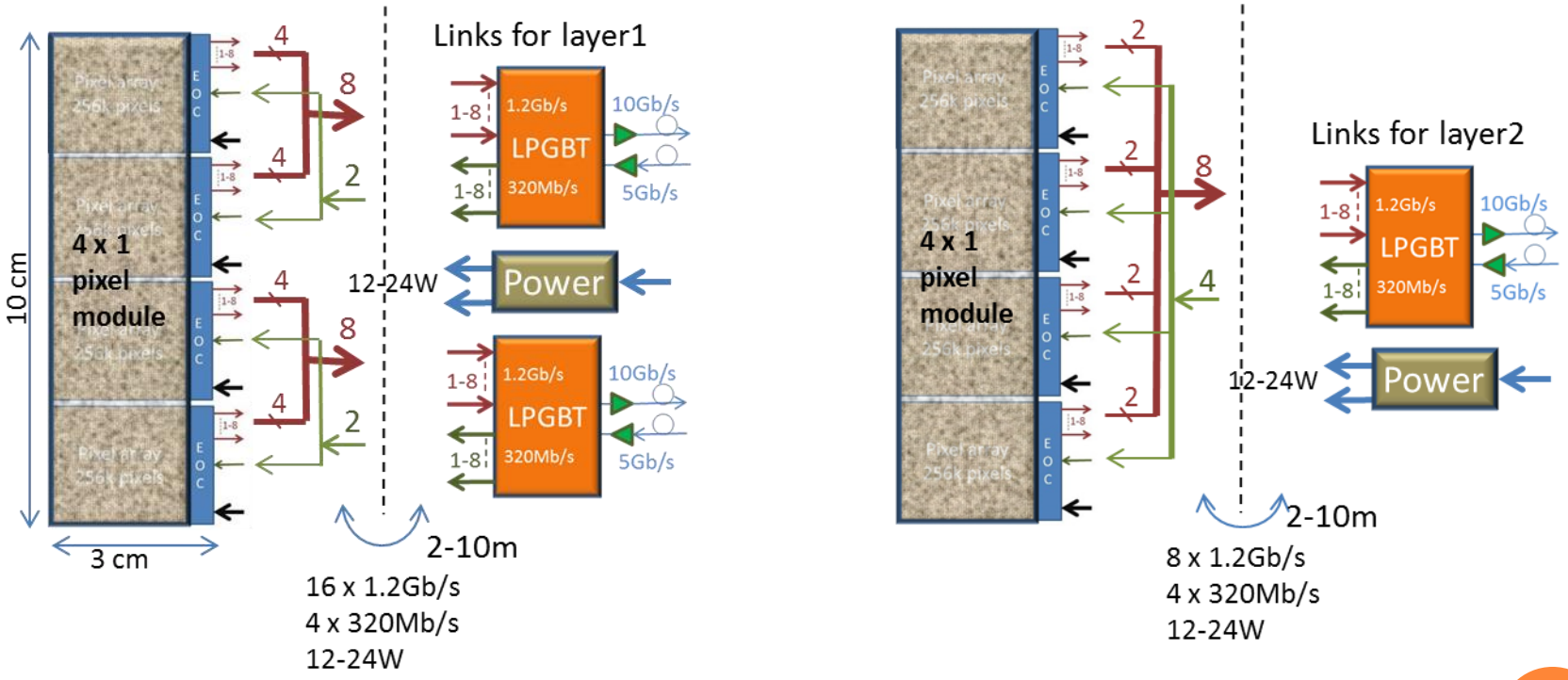
- 1x4 pixel chip modules for Layer 1 & 2
- 2x4 pixel chip modules for Layer 3 & 4 and forward disks
- Electrical links: 1.2Gbits/s on capton, micro coax/pair
  - Only point to point connections
  - Pre-emphasis drivers
  - Equalizer(filter) receivers
- Pixel chip:
  - 1-8 **1.2**Gbits/s data links
  - 1 320Mbits/s control/timing link
  - Power: 0.5 – 1 W/cm^2
- No pixel module controller
- LPGBT:
  - 8 x 1.2Gbits/s data links = 10Gbits/s (user data !)
  - 8 x 320Mbits/s control/timing links = < 5Gbits/s down link (much less would be OK)





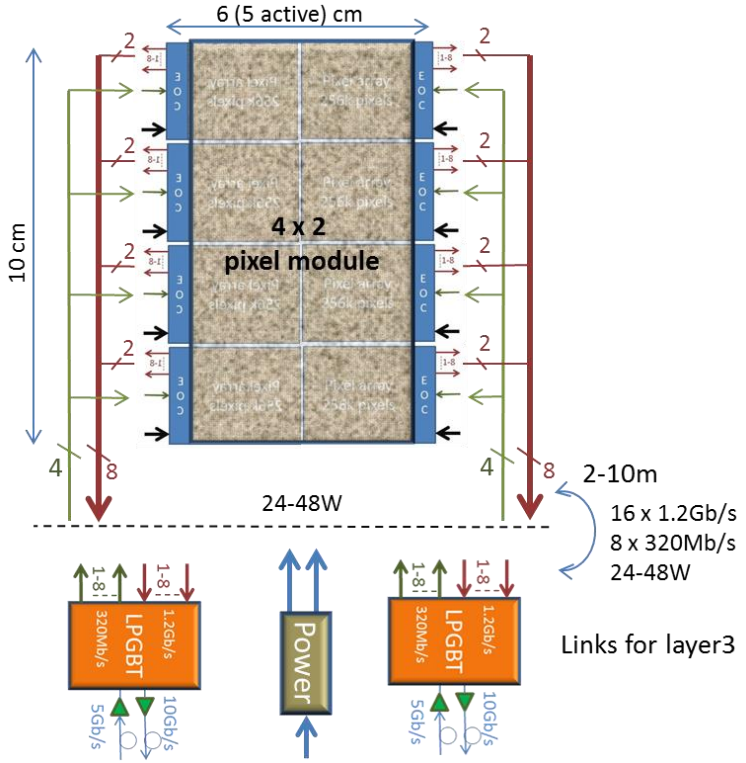
4X1 PIXEL MODULE: A

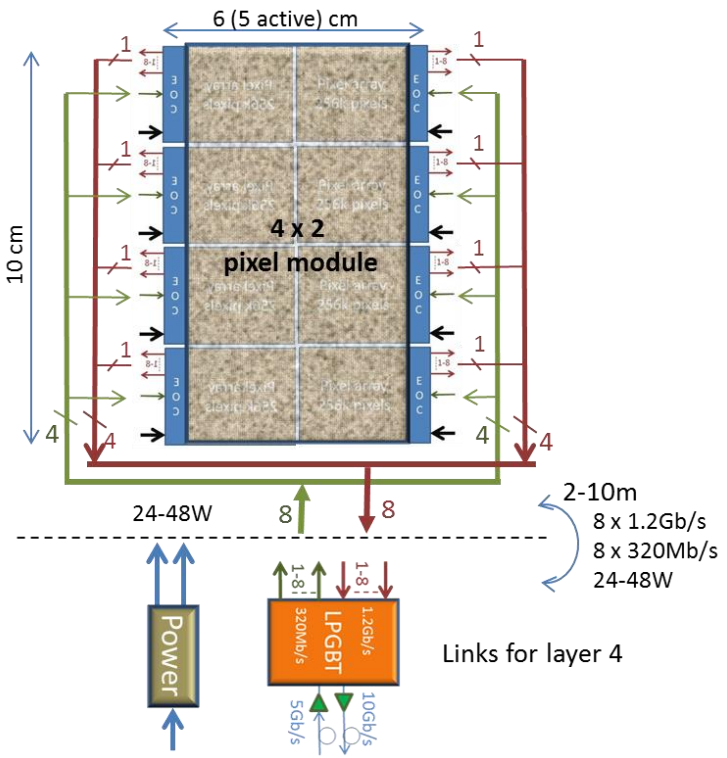
- Same 4x1 pixel module for layer 1 & 2
- Different link configurations
  - Layer 1: 2 x 10Gb/s links (3 x 6.4Gb/s links)
  - Layer 2: 1 x 10Gb/s link (2 x 6.4Gb/s links)



4 x 2 PIXEL MODULE: B

- Same 4x2 pixel module for layer 3 & 4 & disks
- Different link configurations
  - Layer 3: 2 x 10Gb/s links (3 x 6.4Gb/s links)
  - Layer 4: 1 x 10Gb/s link (2 x 6.4Gb/s links)





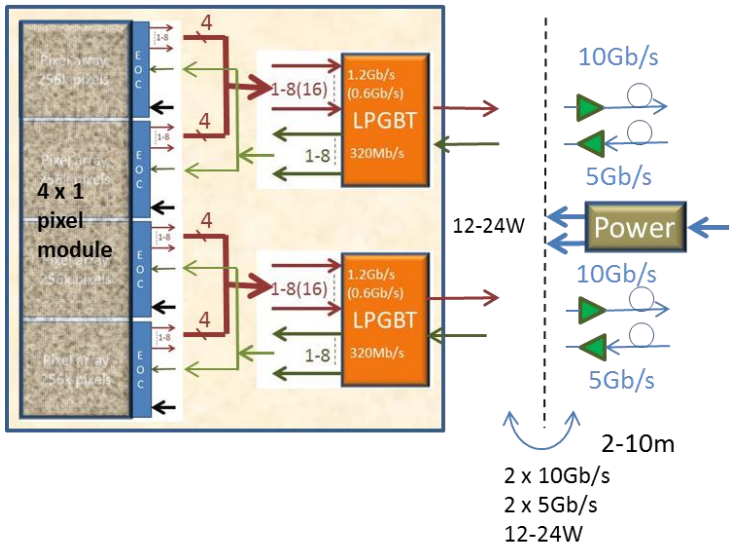
Option B: LP-GBT on pixel module

- Two variants of each pixel module type with 1/2 links ?
- Where to put LP-GBT ?:
  Cooling: Will not be such a low power chip (1/2 – 1 W ?)
  A. In middle of hybrid on top of sensor
  B. Extensions at the ends
  C. On the side
- Is it sufficiently radiation hard:
  - Likely not as very high speed at limit of technology
    - We will not know before very late !
  - Use it a ½ speed ?
    - But then we need twice as many
  - SEU rates in our extreme radiation environment ?
- Delicate high speed cupper/alu link
  - Special very radiation hard cable driver and receiver
- How to power it ?
  - It may need higher supply voltage than our highly power optimized pixel chip design.
  - Will not have on-chip DC/DC.
  - What if we use serial power ?.

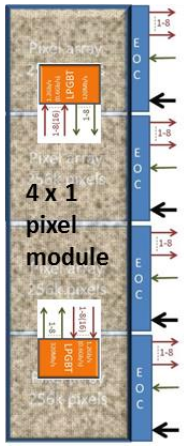
  Will most likely need its own dedicated power
- In the ideal world where we could put the Opto on the pixel module;
  - Radiation tolerance, compactness ?

One would most likely use the same pixel chip – LPGBT communication (no cable driver/receiver).

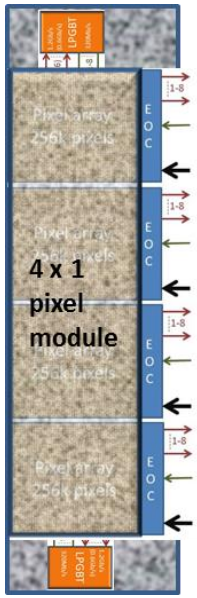
Make pixel chip (and LPGTB) so both options can be used (cable drivers/receivers)



On top

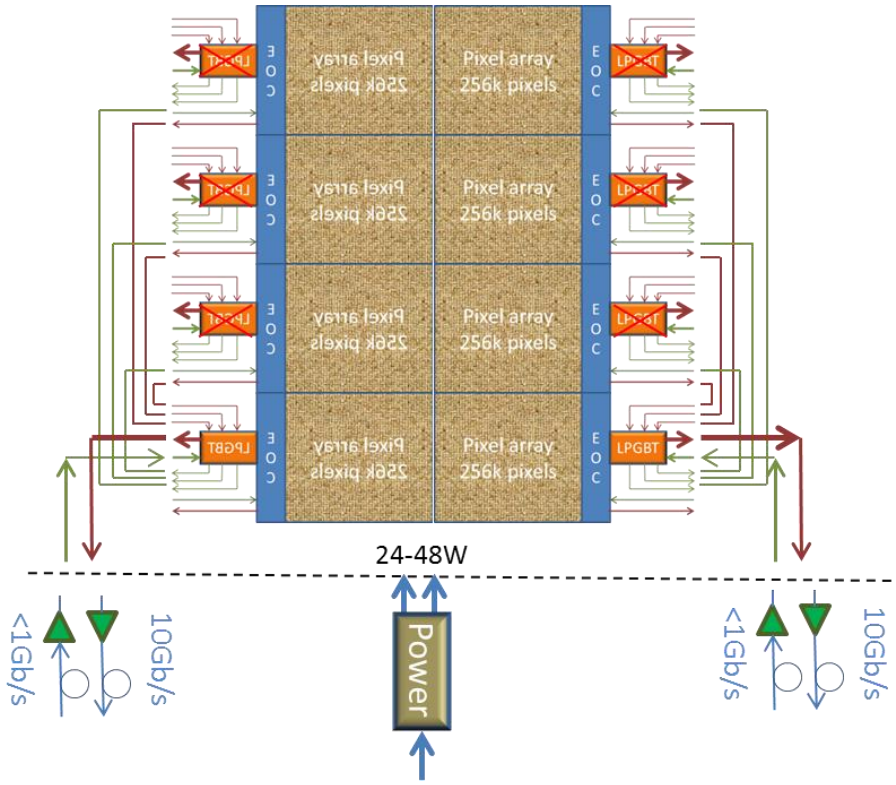


At ends



Option C: "LP-GBT" in pixel chip

- We still have the problem of the opto and related drivers/receivers to/from remote board
- One opto link per pixel chip not optimal for outer layers
  - Build-in "LP-GBT" concentrator and fanout function and only use link for ½ or ¼ of the chips.
- What link speed ?.
  - 10G: Speed degradation with radiation is a significant risk
  - 5G: More links and possibly still non trivial to integrate and get to work for our very high radiation levels ?.
  - Low speed down link for timing/control: 320Mbits/s
- Other
  - Dedicated module controller and link chip
  - Only serializer in pixel chip and timing/control from fan-out from LPGBT on remote module.
  - ?



Pixel phase 2 spaghetti

- Pixel detector: ~1000 modules
- Each module needs 12 – 24 1.2Gbits/s E-links
- Needs ~15k electrical "low mass" links
  - What is a low mass electrical link ?.
    - Distance, Speed, Cable, Driver, Receiver , ,
  - Routing/Installation ?
  - Material and physics impact ?
- How to improve:
  - Lower trigger rate: ½ (500KHz)
  - (Confirm hit rates)
  - On chip track/cluster extraction: ½ ?
    - Local intelligence in very hostile radiation environment
  - Higher speed links: 2 – 10Gbits/s ?
    - How much "copper" needed for this ?
    - High speed circuits in radiation environment ?.
  - Opto on pixel module (Readout = VCSEL)
    - Can it survive radiation ?
    - Speed: 5 – 10Gbits/s ?
    - Power, compactness, ,

Summary of 1MHz trigger

- 1MHz trigger will be a significant challenge for the pixel system (not so much for the pixel chip)
  - Low mass requirements
  - Opto in pixel volume ? (radiation, compactness)
    - Where else to put Opto: 2-10 m
- Requires 1-2 10Gbits/s data links per pixel module (both Type A and B)
  - Data reduction: Lower trigger rate, track location extraction
- Remote opto: Connection from pixel module to optical link: 2-10m
  A. **Modest E-link speed to LPGBT: 1.2 Gbits/s**
     - 12-24 E-links per pixel module
     - ~15k Low mass cables !
     - **Flexible and modular approach to deal with different data rates on different modules and has a factor 2 safety factor in available output bandwidth of ROC (use 4 of 8 outputs)**

     CABLE SPAGETTI AND MATERIAL !.

  B. LPGBT on module: 10Gbits/s up + 5Gbits/s down
     - Few (2 x 2) high speed electrical links per module
     - High mass cable + Complex high speed link driver/receiver required ?
     - Can LPGBT survive radiation ?

  C. Build-in modest speed "GBT" in pixel chip.
     - Multiple intermediate speed (2-5Gbits/s) electrical links
- Local opto:
  - Radiation hardness ?
  - Compactness ?
  - Link Speed ?
  - LPGBT or custom chip or built-in ?
  - Only driver (laser) and remote receiver (PIN) ?

Summary & conclusions

- **1 MHZ trigger** rate is a major challenge for the readout of the pixel detector:
  - Highest hit rates of all detectors
  - Highest constrains on space/mass/power
  - Extremely hostile radiation environment

  Seems feasible at cost of material budget !
- **20us trigger latency can imply larger pixels**
  - Pixel size will be dictated by what we have to put in each pixel in the ROC: Analog + **Buffering**
  - Storage (SRAM) cells will have to be large because of radiation.
    - To be studied in detail
- Pixel contribution to trigger:
  - Data bandwidth out of pixel detector is the bottleneck
  - Complex processing in ROC will be difficult
    - Radiation, Power, Area, Complexity
  - **Limited time to evaluate ideas and global gain**
- **Differences to ATLAS may require dedicated CMS pixel chip**
  - ATLAS
    - L0: **500KHz, 6us**, (10% ROI)
    - (L1: 200KHz, 20us)
  - Technology and building blocks will come from RD53

What we need to study/understand

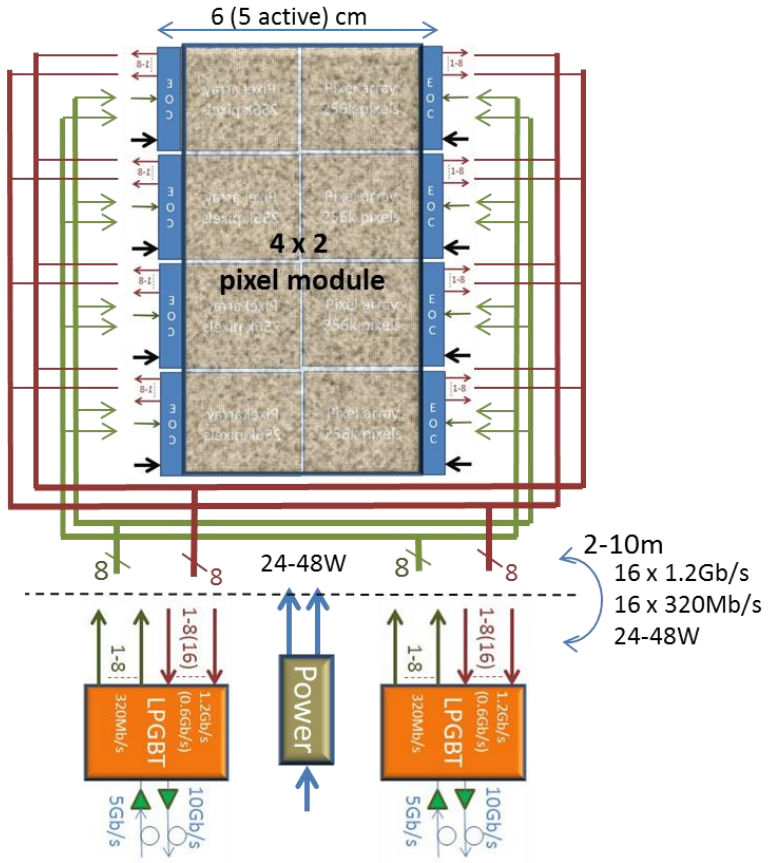
- Can opto be used within pixel volume
  - At least for readout: VCSEL + driver + serializer
  - Radiation, size, power
- Where can (opto) services be located: 2 – 10m ?
  - Full detector layout required ?
- What is a low mass electrical link ?
  - Rate, Length, Mass, driver/receiver complication, power
- Confirm assumed hit rates: Track rate, cluster size
  - How does this depend on sensor and layout ?
- Additional data for pixel trigger at L1 ?
  - Seems difficult !
- Room for data storage in pixel region with radiation hard storage cells ?
- (Why does CMS "need" a 1MHZ trigger rate when it has a track trigger ?)
  - ATLAS aims at 500KHz, without track trigger !.

Backup

4 x 2 PIXEL MODULE WITH LINK REDUNDANCY

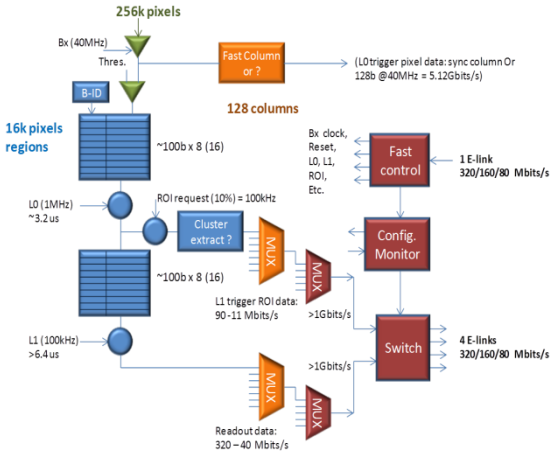
- Requirements:
  - Two control inputs per pixel chip with automatic selection of the correct/active one.
- Redundant mode:
  - Only one of the links active.
  - ½ data bandwidth
- Full bandwidth mode:
  - Data from one pixel chip will be split across the two links.
  - Control from one link and data to two links.

Notice: Only point to point links



Pixel contribution to trigger ?

- **Many questions and challenges**
- **Self seeded (push): On what basis ?**
  - Double layer Pt cut a la TT: NO
    - Requires very high rate connections between pixel chips on different layers, + chip overlaps.
    - Chip to chip bandwidth (minimum): ~50 Gbits/s (inner)
      - 75 tracks/IC/Bx x 40MHz x ~18bits (optimistic)
    - Connectivity nightmare in "low" mass pixel detector
  - "Pt cut" based on cluster shape: NO
    - Depends strongly on sensor type and sensor thickness that is not yet fixed.
    - Requires local intelligence to analyze all clusters in real time
      - We are already very tight in resources for buffering/logic/triggering
      - Has to be done in extremely hostile radiation environment
    - Can this work across whole pixel barrel + endcap ?
    - What is rate reduction and what is physics gain ?
  - Send coarse information for each cluster @ 40MHz: NO
    - Requires local and intelligent cluster extraction.
    - Requires ~50Gbits/s per chip on top of normal readout (5Gbits/s) (inner)
  - **Possibly do one of these for outer layers only (1/10 rate of inner layer): ?**



- **ROI based (Pull, as ATLAS)**
  - Two level trigger ?: Rates, Latency and ROI fraction
    - High rate L0 trigger: 10MHz ?, 3-6us ?, 10% ROI ?.
    - Low rate L2 trigger: 100KHz ?, 100us ?.
  - What to send ? (Full or only coarse cluster information)
  - **Groups still working on this if there is some significant gain at reasonable cost (complexity and data rates from pixel front-ends)**
- **Data bandwidth out of the pixel detector is the bottleneck (+ROC complexity)**
  - Low power, Logic/buffer density, Radiation, Communication and links, etc.
  - **New realistic ideas must be verified soon !.**