Status and plans of RD53

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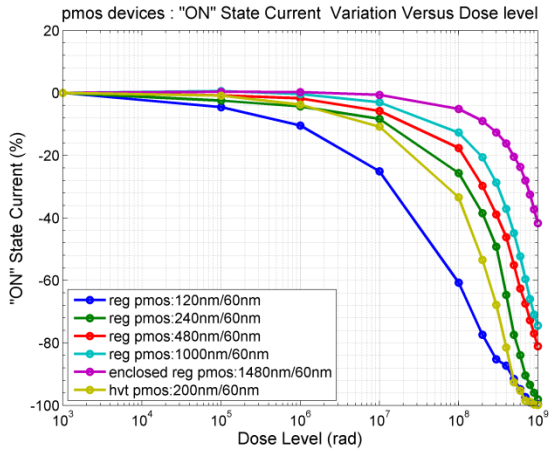
General

- Spokes persons and Institute chair elected
  - SP's: ATLAS: Maurice Garcia-Sciveres, LBNL
CMS: Jorgen Christiansen, CERN
  - IB chair: Lino Demaria, Torino
- We have had our first formal IB meeting
  - 2-3 times per year
- Planning first (2nd) RD53 workshop for spring 2014 at CERN
  - Finding good date is a real pain.
- 3 additional institutes have requested to become members: OMEGA, Milano, Czech Technical University + institute of physics, (Sevillia ?, Taiwan ?).
  - We have a preference to get organized before welcoming new institutes.
- MOU in the pipeline.
- RD53 is getting rather well known as a good example of a focussed ATLAS/CMS R&D:
  - Now we have to prove that this works efficiently !.
- Some working groups have gotten started (to get organized)
- Some RD53 institutes have gotten funding (INFN)

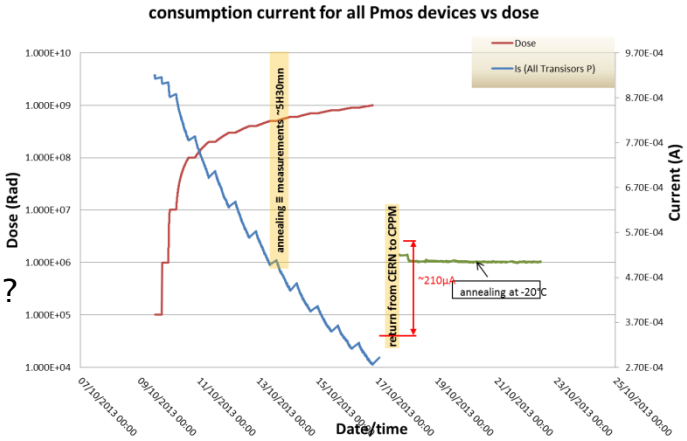
Radiation WG

- Goals: Radiation test and qualification of 65nm
  - Radiation test procedure -> Report
  - Test of basic devices -> Report
  - Test of digital cells (standard cell library)
  - Spice models of radiated devices
  - Recommendations to designers
  - (Evaluation of alternative technologies if required)
- Convener: Marlon Barbero (CPPM)
- 2 meetings held
- Coordination of radiation test structures and radiation tests
- Radiation test procedure document in the pipeline
- If chips kept cold (-20 – 20 deg. C) then signs of problems with PMOS at ~100Mrad radiation levels
  - Annealing:
    - -20: None ?
    - Room: Some annealing, but how much ?
    - Hot (80 – 100): Good annealing but how much and how fast ?
  - **Annealing will be a critical aspect for pixel phase 2**
    - Running scenario: -20 deg with ~2weeks at room temperature per year
  - We should soon have more annealing results from CPPM with CERN test structures.

We will get 100MRad per year in inner layer !



CPPM



Analog WG

- Goals:
  - Analog front-end(s)
    - For different sensors
    - Different architectures (TOT, ADC, Auto zeroing, etc.)
  - In the end we will need 1-2 for ATLAS/CMS
    - Area, power, noise, dead-time, radiation tolerance, linearity, simplicity, , ,
  - Basic analog building blocks (references, bias DAC, etc.)
    - Coordination with IP blocks WG
- Convener: Valerio Re
- First meeting with presentation from institutes
  - Many groups wants to look at “their” specific architecture
- To be defined how work across groups and different architectures can be best optimized for our final goal.
  - Not just individual non-connected designs

Simulation

- Goals:
  - One common simulation and verification framework
  - Evaluation of different architectures with this framework
  - Definition of how to include IP block in simulation
  - Verification of final designs
- Convener: Tomasz Hemperek (Bonn)
- First meeting with presentations of groups interested:
  - Bonn, Perugia, CERN, NIKHEF (mixed signal, DFT), (LBNL, PISA, RAL
- Simulation language/tool
  - System Verilog + UVM (Mini workshop @CERN)
  - C++ or other
- First goals:
  - Tool/language
  - General framework architecture
  - Shared repository
  - Defined interfaces
  - Define who contributes what

IP blocks

- Goal: Implement required basic building blocks
  - Define list of required IPs and who makes what
  - Standardized requirements for IPs
    - Use of metal layers, pins, analog/digital isolation, , ,
  - For each IP: Specifications, design, prototyping, test, radiation hardness, documentation, simulation model, available on IP repository for RD53
- Convener: Not yet assigned
  - J.C. will bootstrap until “things” more clear and convener can be found
- Short term goal:
  - List of IPs (20 – 50) and make interest matrix across RD53 groups
  - Assign an institute(s) to each needed IP

Top level

- Goals: Define appropriate schemes and tools to integrate complex mixed signal functions into working pixel chip
  - Layout (e.g. Technology options, layer mapping), powering, noise coupling , Final design verification,
- Convener: not yet assigned
  - M.G.C. will bootstrap until “things” more clear and convener can be found
- Short term goals:
  - Understand what is covers and what is required

I/O

- Goals
  - Define standardized I/O interface of pixel chips
  - Define and implement I/O blocks
    - Some overlap with IP blocks

  Standardized pixel chip interfaces also allows to standardize pixel chip test systems
- Convener: Not yet assigned

Additional domains for “RD53” ?

- **TSV (affects TOP, IO and IP WGs)**
  - **Coarse TSV to get power and IO signals out on back side and have much less module overlap caused by wire-bonding.**
- **Standardized/common test systems: hardware, firmware, software**
  - **For “near” final pixel chips (not for small block submissions)**
- **High speed readout on low mass cables**
  - Speed, distance, cable, ,
  - Interface to optical links (LPGBT)
- **Powering**
  - DC/DC versus Serial powering
  - On-chip power conversion
  - Off-chip power conversion
- Module design/cooling
- Other ?