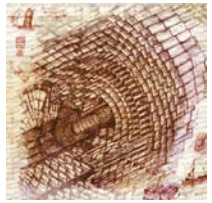

Would a DC-DC Conversion Scheme as in Pixel Phase-1 Upgrade work for a Pixel Detector at Phase-2?

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Phase-2 Pixel Electronics Meeting

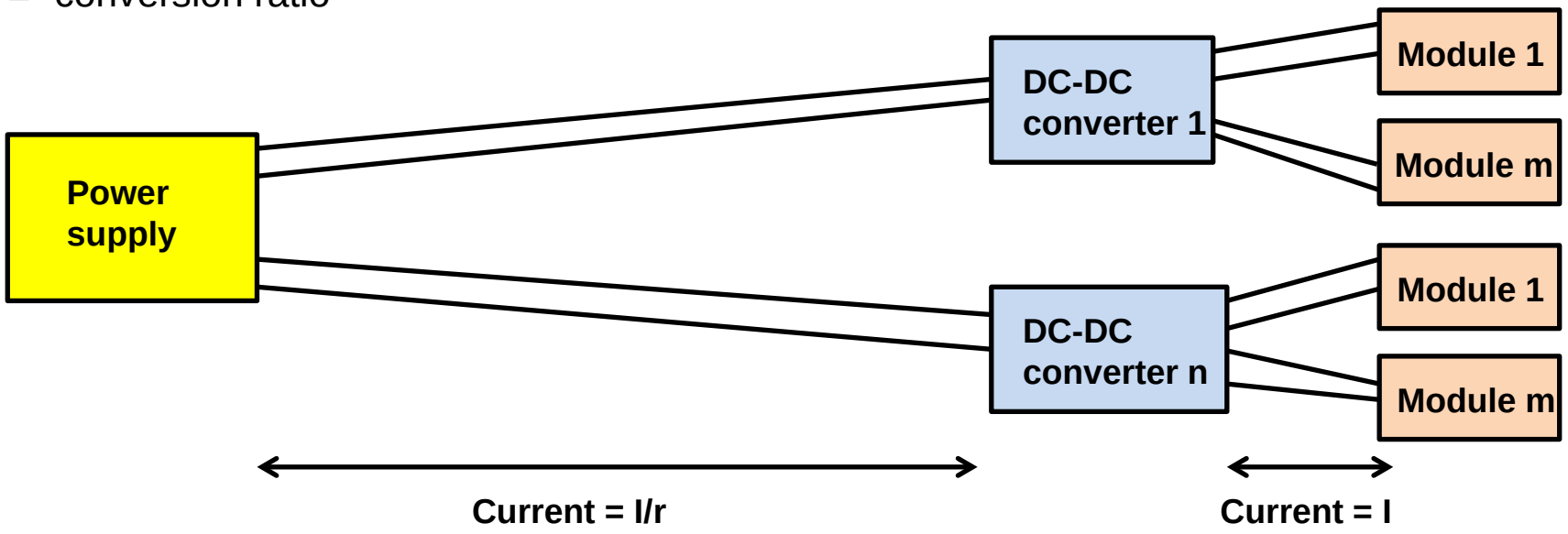
November 20th, 2013

Outline

- DC-DC conversion basics
- Power system for the Pixel Phase-1 Upgrade
- Requirements for Phase-2 Pixel upgrade
- Go through requirements, confront them with today‘s reality, explore consequences
  - Radiation hardness
  - Conversion ratio
  - Output current
  - Space and mass
  - …
- Conclusions

DC-DC Conversion Basics

Power is supplied at a higher voltage and lower current: P = U x I = (rU) x (I/r)
r = “conversion ratio“



Advantages on input side:

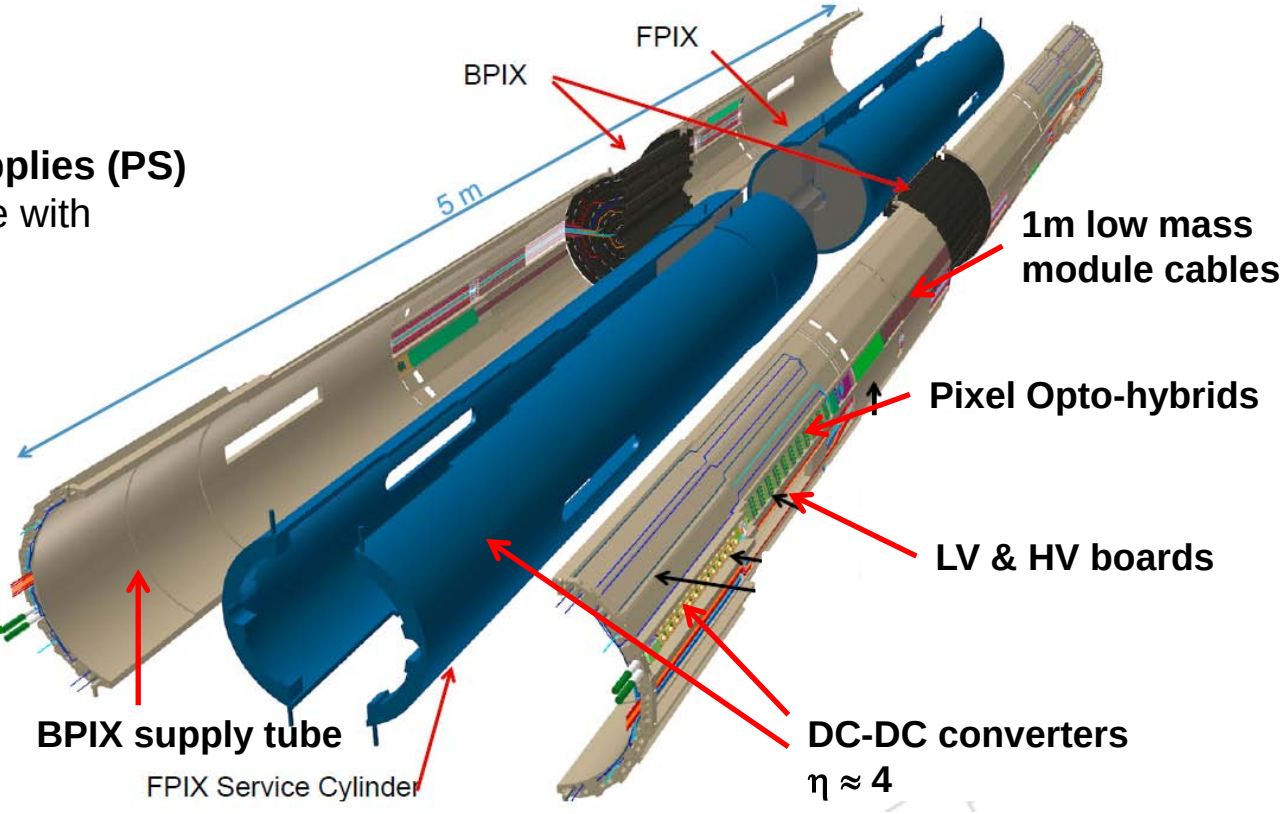
- **Voltage drops dU = R_{cable} x I go down by r**
  → for the same voltage drop than without DC-DC converters,
  thinner cables or PCBs can be used inside the sensitive volume→ reduction of material
  Obviously this is only the case if the conversion takes place close to the modules!
- **Ohmic losses P = dU x I = R_{cable} x I^2 go down by r^2**
  → higher overall efficiency, lower heat load on cables, smaller power supplies

Phase-1 Pixel Powering: Overview

CAEN A4603 power supplies (PS)
Modified to be compatible with
DC-DC conversion

- **Pixel modules need:**
  - ~1.7V for analogue electronics
  - ~2.5V for digital electronics
  - Bias voltage: 0 - (-600V)
- In addition: 2.5V for auxiliary electronics

Multiservice cables (MSC)
43m + 5m + 0.5m (new)



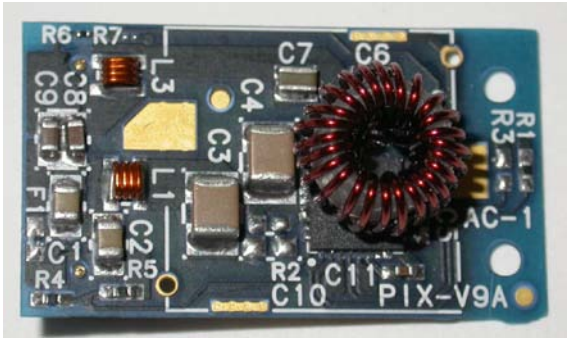
Phase-1 Pixel Powering: History & Motivation

- DC-DC buck converters were originally developed for Phase-2 outer tracker
- Phase-1 Pixel detector has 1.9 x the number of channels as present pixel
  → factor 1.9 larger currents (voltages do not change)
  → power losses on supply cables $P_{loss} = R_{cable} \times I^2$ increase by $1.9^2 = 3.6$
- Calculations (Willi Bertl, PSI) showed that this power cannot be delivered by the power supplies and that cable channels would heat up
- Development and installation of new, more powerful power supplies felt to be incompatible with installation during Winter technical stop; no space for additional cables in cable channels
- R&D on a step-2 on-chip charge pump DC-DC converter (Beat Meier, PSI) was not pursued
- Decision to install buck converters with a conversion ratio of 3-4 on the pixel supply tube (June 2009), 1-2m from the actual pixel modules
- Some people claim that the DC-DC converters reduce the material budget of the Phase-1 pixel detector, but this is not true!

Pixel DC-DC Converters

DC-DC converters optimized for the phase-1 pixel upgrade

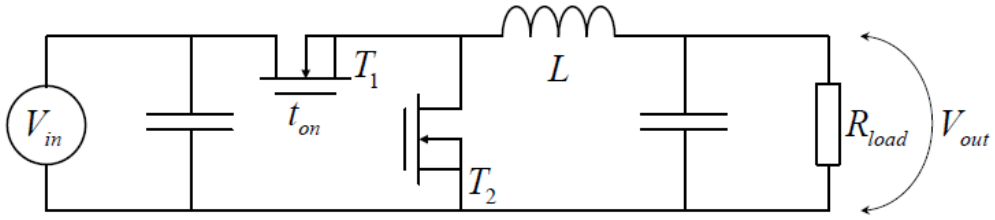
V_{in} = 10V and V_{out} = 3.0V or 2.4V → r ~ 3-4
Switching frequency f_s = 1.5MHz
2-layer PCB
Toroidal plastic core inductor L = 450nH
Pi-filters at in- and output



AC_PIX_V9 A: 2.8cm x 1.6cm; ~ 2.0g

ASIC: AMISx/FEASTx by CERN-PH-ESE
(St. Michelis, F. Faccio)
AMIS I3T80 0.35µm CMOS (ON Semiconductor)
Includes: power transistor, drivers, control logic, feedback loop to regulate output voltage

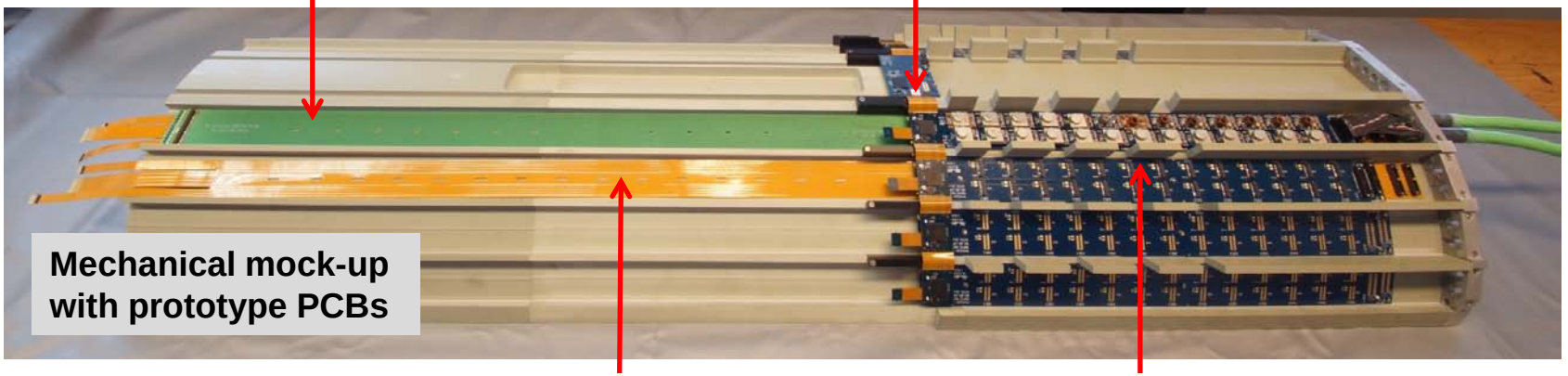
Copper shield



Supply Tube Power Electronics (BPIX)

Low voltage extension boards
2 boards above each other (not visible)
75cm long
100g each

CCU ring board
Used to control DC-DC converters, POHs, DOHs, modules etc.
54g



HV flex board

DC-DC bus boards
each with 26 DC-DC converters
45cm long
~120g (without converters)

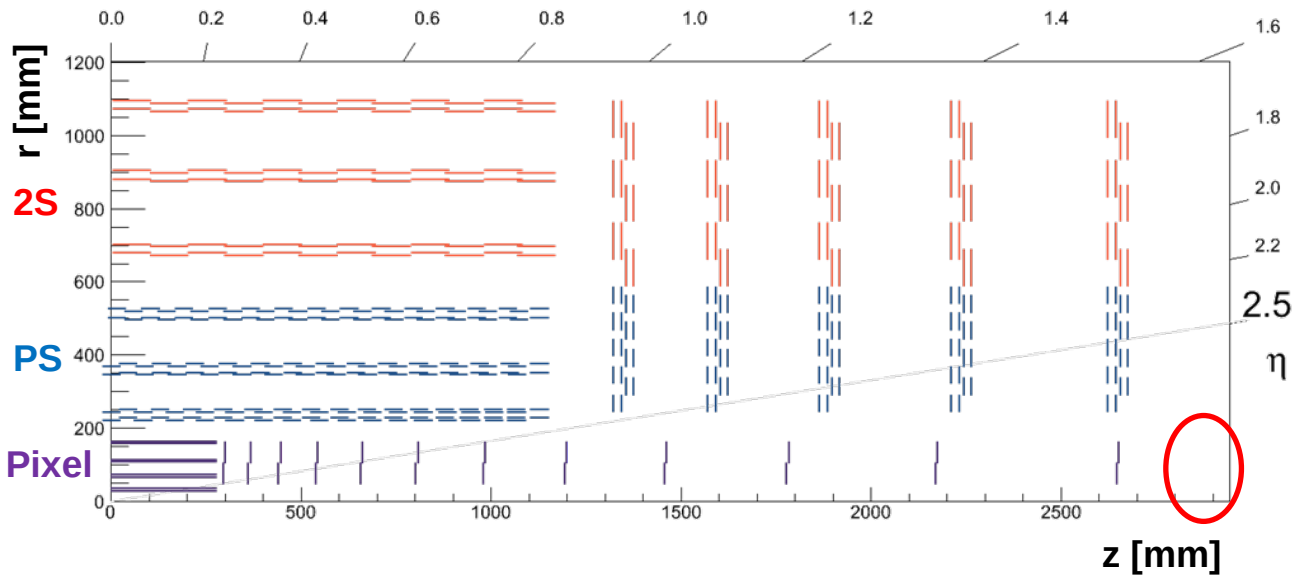
- 4 half shells x 8 slots x 300g = 10kg just to bring LV across a distance of 1.2m with a voltage drop of 100 – 200mV
- Converters are cooled via aluminium bridges from CO_2 pipes

Requirements for Pixels at Phase-2

Quantity	Phase-1	Phase-2
# of barrel layers	4	4
# of disks per side	3	6 – 10 (12?)
ROC power density	0.3 W/cm^2	0.3 - 0.6 W/cm^2
ROC voltage(s)	1.7V & 2.5V	1.0V - 1.2V
ROC current density	0.15 A/cm^2	0.3 - 0.6 A/cm^2
Distance of DC-DC conv. from pixel detector	0.5 - 2 m	5 - 10 m (???)
Fluence	2 x 10^{14} n_{eq}/cm^2	2 x 10^{15} n_{eq}/cm^2
Total Ionizing dose (TID)	100-200 kGy	1 MGy

- Irradiation levels for Phase-1 are for a position of r ~ 16-20cm and z ~ 1-2m
- For phase-2 I cannot just scale up; I need to know the position
- I assumed r = 20cm and z = 3m (~ bulkhead) → next slide

Requirements for Pixels at Phase-2

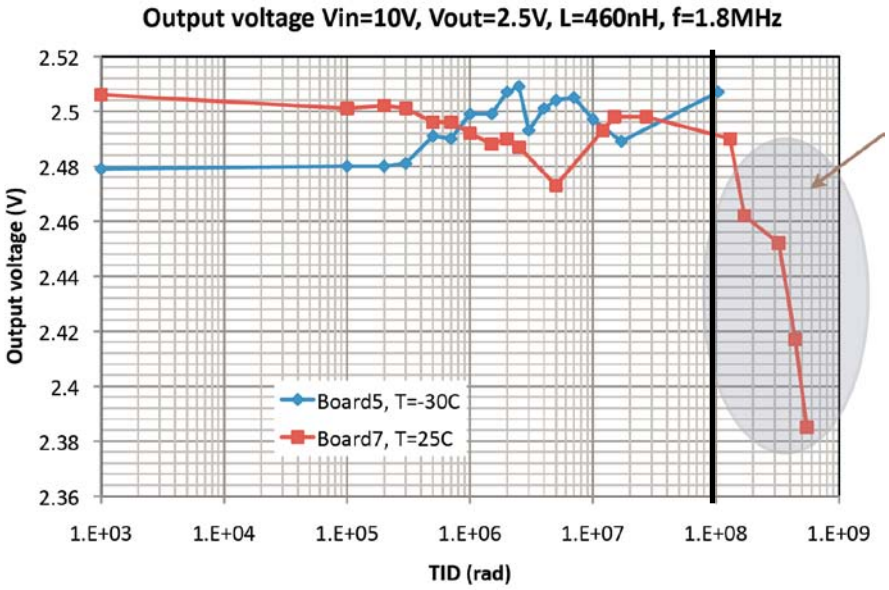


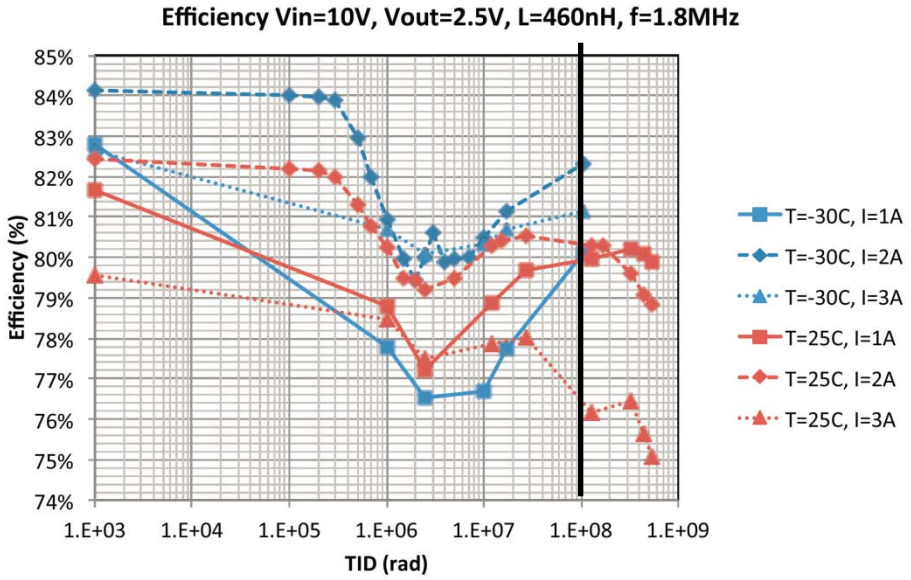
- I do not know where the DC-DC converters would be installed
- I had assumed somewhere at the bulkhead (behind the last disk)
  → z ~ 3m and r > 20cm
- A distance of 5-10m is not feasible due to voltage drops (details later)

Radiation Tolerance: TID

- FEAST was tested with X-rays at CERN up to ~ 500Mrad
  (results presented by Stefano at Power WG meeting, 27. 8. 2013)
- FEAST seems to work well up to a TID of ~ 100Mrad = 1MGy
- For higher dose, bandgap voltage decreases → output voltage drops

Required: ~1MGy → looks roughly ok, but not much safety margin



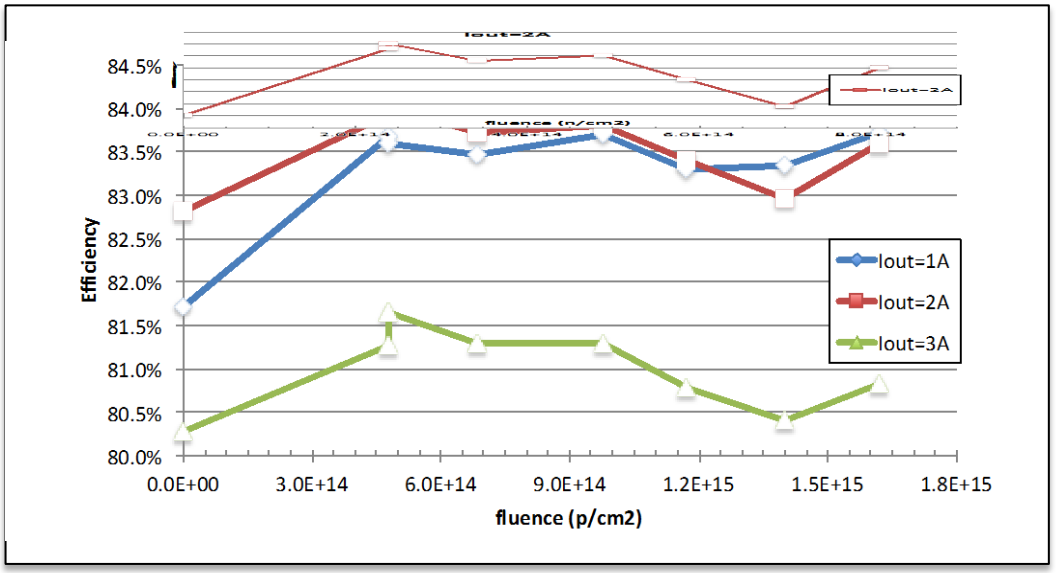


Radiation Tolerance: Fluence

- AMIS5 was tested with protons at CERN
  (results presented by Stefano at Power WG meeting, 5. 2. 2013)
- AMIS5 works up to 1.4 x 10^{15} p/cm^2 (corresponds to 7 x 10^{14} n_{eq}/cm^2)
  - Large band gap drift: +180mV
- For 1.6 x 10^{15} p/cm^2 only 1 out of 2 tested converters worked
- No converter survived > 1.6 x 10^{15} p/cm^2

Required ~ 2 x 10^{15} n_{eq} /cm^2

→ Insufficient



Radiation Tolerance: Fluence

- Problem is considered to be caused by displacement damage in HVPMOS transistors used in regulators
- On-Semi provides different technologies which differ only in HVPMOS (same LV transistors and HVNMOS)
- Investigation of another semiconductor technology: AMS H18
- Tests with neutrons up to 5 x 10^{15} n/cm^2
  - Transistors, diodes, linear regulators in both technologies
  - Small converter in AMS H18

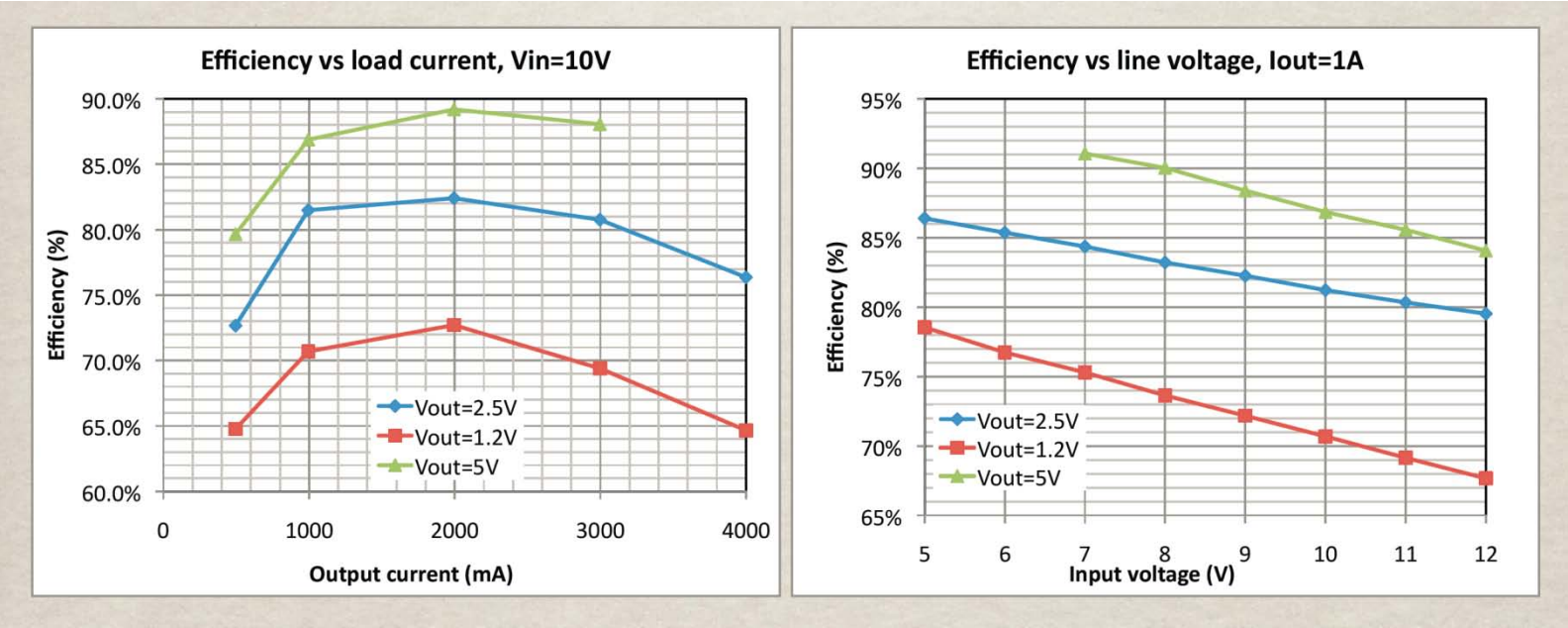
→ Regulator still working, efficiency reduced by few %, drift of bandgap

→ **More work needed**

Work is done by CERN PH-ESE.

Conversion Ratio

- ASICs (e.g. FEAST) can receive 12V at the input and deliver 1.2V at the output
  → r = 10
  → losses are reduced by a factor of 100
- Efficiency for r = 10 is not great (but acceptable): ~ 60% for 4A output current
  (measurements with FEAST presented by Stefano in Aug. Power WG meeting)



Converter Output Current

- FEAST ASIC specified for 3-4A output current

- Successfull tests with AMIS4 pixel converters
  - up to 4A for cooling temperatures up to +25°C
  - up to 5A for cooling temperatures up to +5°C

- Electro migration* simulated by Federico for AMIS5
  margin in the current density is
  - 10 for 5A at chip temperature of +20C
  - 4 / 3 / 2.5 for 3A, 4A, 5A at chip temperature of +50C
  - At +80C chip temperature, the 5A case starts to be critical (failure rate exceeding 1% failures in 10 years of operation)

* From Wikipedia: Electro migration is the transport of material caused by the gradual movement of the ions in a conductor due to the momentum transfer between conducting electrons and diffusing metal atoms.

Converter Output Current

Module type	Module area [cm^2]	Module power [W]	Module current [A]	Analog and digital current [A]
1 x 2 chips	8	4.8	4	**2**
1 x 4 chips	16	9.6	8	**4**
2 x 2 chips	16	9.6	8	**4**
2 x 4 chips	32	19.2	16	**8**

- Assumptions
  - ASIC size = 4 cm^2
  - Worst case power density = **0.6 W / cm^2**
  - U = 1.2V (for both analog and digital)
  - Digital : analog power = 0.5 : 0.5

→ 2 x 4 chip modules are excluded

→ 1 pair of DC-DC converters (1 for analog part, 1 for digital part) could power 1 pixel module

→ Assuming an active area of 4m^2, and 1 x 4 or 2 x 2 modules, the number of modules is 2 500 and the number of converters 5 000

→ FE current = 20kA

Converter Output Current (II)

Module type	Module area [cm²]	Module current [A]	Analog and digital current [A]
1 x 2 chips	8	2	**1**
1 x 4 chips	16	4	**2**
2 x 2 chips	16	4	**2**
2 x 4 chips	32	8	**4**

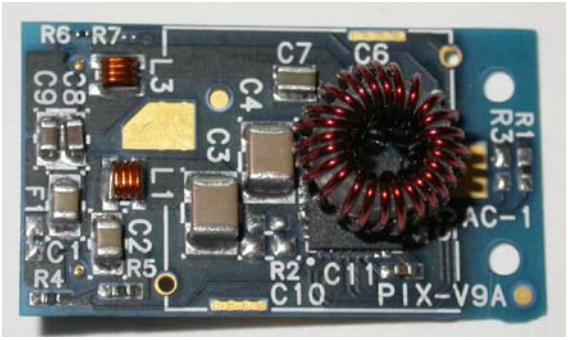
- Assumptions
  - ASIC size = 4 cm^2
  - Best case power density = **0.3 W / cm^2**
  - U = 1.2V (for both analog and digital)
  - Digital : analog power = 0.5 : 0.5

→ Now 2 x 4 chip modules are possible
→ 1 pair of DC-DC converters could power 2 pixel modules
→ much less DC-DC converters required

Space Requirements

- Area of present pixel DC-DC converters: **2.8cm x 1.6cm ≈ 4.5 cm²**
- Height (including connector) = 1.4cm
- Some reduction in size & height can be expected
  (but I think 50% reduction will already be very difficult to achieve!)

→ Area required for 5 000 DC-DC converters: 2.2 m²

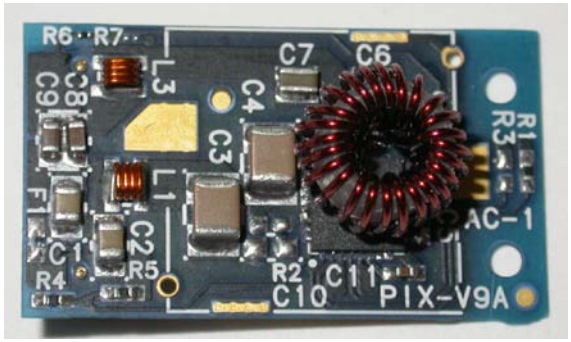


AC_PIX_V9 A: 2.8cm x 1.6cm

Weight of DC-DC converters

- Weight of present pixel DC-DC converters, including shield: **3g**
  - A phase-1 pixel module of layer 1 weighs 1.6g
  - It has never been considered to place the converters inside the pixel volume, and will not be feasible for phase-2 either
- Again, some reduction can be expected
  (e.g. by moving to an aluminium coil, higher switching frequency, smaller caps…)

→ **Weight for 5 000 DC-DC converters: 15kg**



Without shield: 2g

With shield and heat conductive paste: 3g

Voltage Drops & Sensing

- The output voltage of the DC-DC converters is regulated by sensing at the chip output (on the converter PCB)
- Remote sensing, e.g. at the module input, is not “recommended“, as the feedback loop is not designed for it (issue with stability)

→ Voltage drops between DC-DC converter and load (pixel module)

→ Will be sizable, since distances are large and currents also

→ System needs to work for different load conditions (0 – max. current)

For the phase-1 pixel detector, we have calculated the voltage margins, and dimensioned resistances of the PCBs and cables on the supply tube accordingly

Even though boards are pretty heavy, and distance is only ~ 1-2 m, it is a constant source of concern!

Placing the converters 5-10m away is not feasible!

A little calculation: dU = 50mV, I = 4A, L = 10m (+return), copper cables → diameter of cable d = 6mm

Material on the Supply Tube

- Depends on the total current: with 2 times the sensitive area and three times the current density compared to phase-1, we need **a factor of 6 more current**
- Depends also on the allowed voltage drop between module and converter
  - For phase-1, the voltage drops for nominal currents are 100 - 200 mV just for the DC-DC bus board and extension board (1.2m long)
  - For 65nm, the voltage has to be stable on the level of 5% = 60mV (Sandro)
    - this includes line and load variation, radiation induced drift, thermal drift, …
    - Allowing for voltage drops of 30mV over 3m, this leads to **a factor of 5 x 3 = 15 larger copper cross section** wrt phase-1 (for the same current)

- **Total factor in material on supply tube is 6 x 15 = 90 – not really an option**
- DC-DC conversion inside the sensitive volume is required

A Two-Step Scheme

- To profit from the concept of DC-DC conversion also inside the sensitive volume, a 2-step scheme with on-chip DC-DC converters would be required
- Total current required per ROC: ~ 1-2 A
- Switched capacitor DC-DC converters are being developed:
  - CERN PH-ESE: r = 2, output current = 60mA
  - LBNL (Maurice Garcia-Sciveres, ATLAS):
    - 130nm, r = 2, I = 1A (for the FE-I4)
    - 65nm, r = 4, I = ?
      - Info from Maurice: device is under test, some parts have blown, needs to be understood, report within ~ 1 month

A Two-Step Scheme (2)

- Example: Switched cap with Vin = 4V, r = 4 and efficiency = 90%
  Buck converter with Vin = 12V, r = 3 and efficiency = 80%
  Total r = 12

- Switched cap delivers Iout = 1A, Iin = 0.28A (per chip)

→ Module with 4 chips needs 1.12A (0.56A analog and digital)

→ Module with 8 chips needs 2.24A (1.12A analog and digital)

- Buck converter: could now power six 4-chip modules or three 8-chip modules from one converter pair
- Voltage drops are “scaled down“ by r = 4 (→ one gains twice)
- But this is not sufficient: in addition an LDO must be foreseen to have more margin for the voltage drops, closer distance of converters, power density only 0.3 W/cm^2 …
- Feasibility depends on many parameters and would have to be worked out

Conclusions

- A scheme as will be used at Phase-1, with only 1 conversion step, cannot be used for Phase-2
- A placement of DC-DC converters many meters away from the load is not feasible, due to the lack of remote sensing
  → it will lead to more mass than a conventional scheme without converters, where remote sensing close to the modules is possible!
- A two-step scheme with a conversion step of 4 on-chip could perhaps work
  → **we need to understand better the feasibility of such development**
- If on-chip converters with the required current capability and conversion ratio cannot be developed, serial powering must seriously be considered
- The pixel ROCs should have an LDO, a switched cap converter (at least r = 2) and electronics (shunt regulators…) for serial powering
- Could the pixel size in the outer layers be (much) larger, in order to profit from the lower power in 65nm?

Additional Material

Output Current