What needs to be investigated and studied for pixel phase2 electronics (For TP)

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We need a “Baseline”

- TP reference point: What to study in more details and possible options
- Layout:
  - Phase1 pixel with extra disks
  - Location of opto/power services ?
  - (Performance, physics, ,)
- Trigger:
  - 1MHz, 500KHz ?
  - 20us , 10us ?
  - Pixel participation in L1 ?
- Pixel chip
  - RD53: Technology, Basic pixel architecture, tools, IPs, ,
  - CMS specific: Sensor, Pixel size/aspect, Trigger rate/latency, L1 trigger contribution
- System:
  - Readout/links
  - Powering
  - Module design
  - Cooling/mechanics
  - ?

Menu of what has to be done and find/assign groups/people to this:

This gets urgent for TP but so far very few groups/people ! (phase 1 in parallel)

For many of these aspects it only makes sense to work closely with ATLAS but for the TP we (CMS) will have to propose a viable system

Pixel chip “menu”.

- Investigate trigger latency – pixel size issue
- (L1 trigger contribution: option)
- Rest is general RD53
  - Where CMS contributions are also vital

Readout “menu”

- Readout data rates
  - Trigger rate
  - Hit rate confirmations
    - Despite uncertainties on layout and sensor
  - Data formatting/compression
  - Track/cluster position extraction
- Readout links
  - Option of Opto on module
    - Dedicated link chip/built-in versus LPGBT
  - Use and requirements to LPGTB (local/remote)
    - Specification group will soon start work.
  - Electrical links: speed, low mass cable, distance, Cable driver, Cable receiver
  - Location and configuration of remote opto module

Powering "menu"

- Power
  - Pixel chip: On-chip: DC/DC, shunt, LDO, etc. ?
  - Optical link: Link interface chip + laser
  - HV
  - Safety/protection aspects
  - Power cabling
  - Bulk power supplies
- Powering options
  - DC/DC: Dynamic variations ("low" power)
    - A. As for phase 1: Remote DC/DC (1-2m)
    - B. Fully on pixel module DC/DC
    - C. Combined remote and on module (and on-chip)
  - Serial powering: Constant module power ("higher" power)
    - A. With-in pixel module (4 – 8 pixel chips)
    - B. Between pixel modules
    - C. On-chip versus on-module shunt regulator
    - D. Intermediate remote DC/DC feeding serial power loops

Pixel module "menu"

- Module integration/assembly
  - Hybrid technology
  - Interconnect:
    - Chip wire bonding / flip chip / TSV
    - Sensor – pixel chip bump-bonding
- Cooling
  - Power density: ¼ – 1W/cm^2 ?
  - Impact on material budget
- System integration:
  - Individual modules
  - Stave (barrel – disks)

Not urgent

- All the off-detector pixel electronics
  - COTS based

TP

- Urgent (6 months) to converge to realistic baseline pixel detector/electronics
  - Phase 1 like does NOT work:
    - Completely new pixel chip/architecture/technology
    - 100x higher readout rates
    - Power requirements very different
      - DC/DC -> serial powering ?
    - Not “allowed” to have “heavy” service cylinder ?
  - We do not have time to set up extensive collaboration/studies with ATLAS on system aspects for our TP.
    - But we should make such collaboration independently of urgency of TP.
- The writing of the few pixel TP pages is the easy part when/if we have a viable implementation worked out.
- We urgently need people to start working on systems aspects (“clash” with pixel phase 1 upgrade)