Fermilab Electronics Development Plans

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Fermilab

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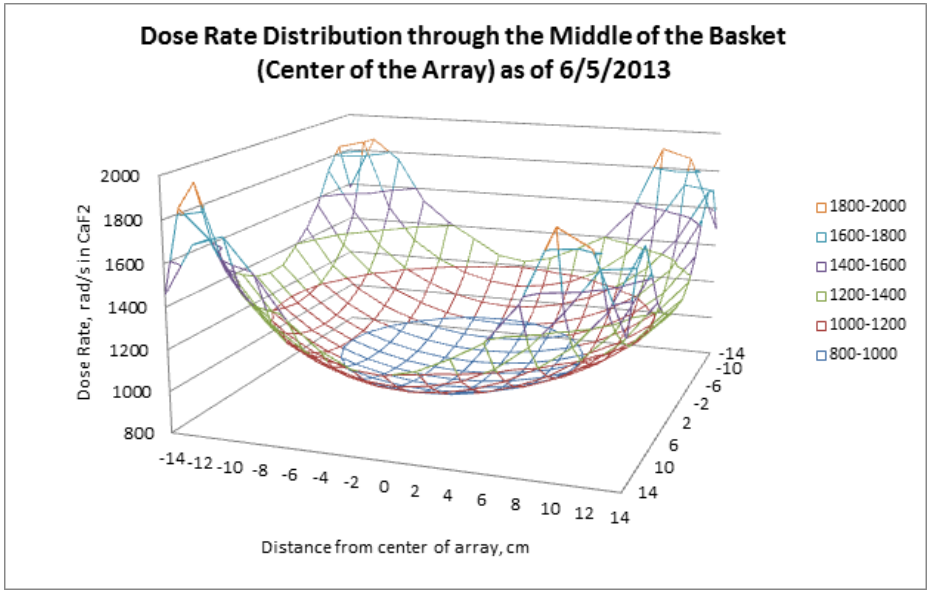
Primary Activities 2013-2014

- Radiation tolerance studies (RD53)
  - 130 and 65nm ICs (mostly transistors) designed at FNAL, fabricated by Global Foundries & TSMC
    - 130nm results will validate our methods
    - 65nm results will extend comprehensive tests to ~1 Grad
  - Gamma irradiation – Sandia National Lab
    - Coordinated by Steve Wagner (Colorado)
    - Major contribution from Michael Krohn (Colorado graduate student)
    - 1st irradiations will be of room temperature devices, but we plan to irradiate cold devices (-20C?) if possible
- Readout chip for array of 30μx100μ pixels
  - 130nm CMOS (GF)
  - Goals:
    - Explore how small a pixel is possible.
    - Demonstrate low threshold ($\leq$ 1000 e^-) operation.
    - Provide a device for sensor R&D.

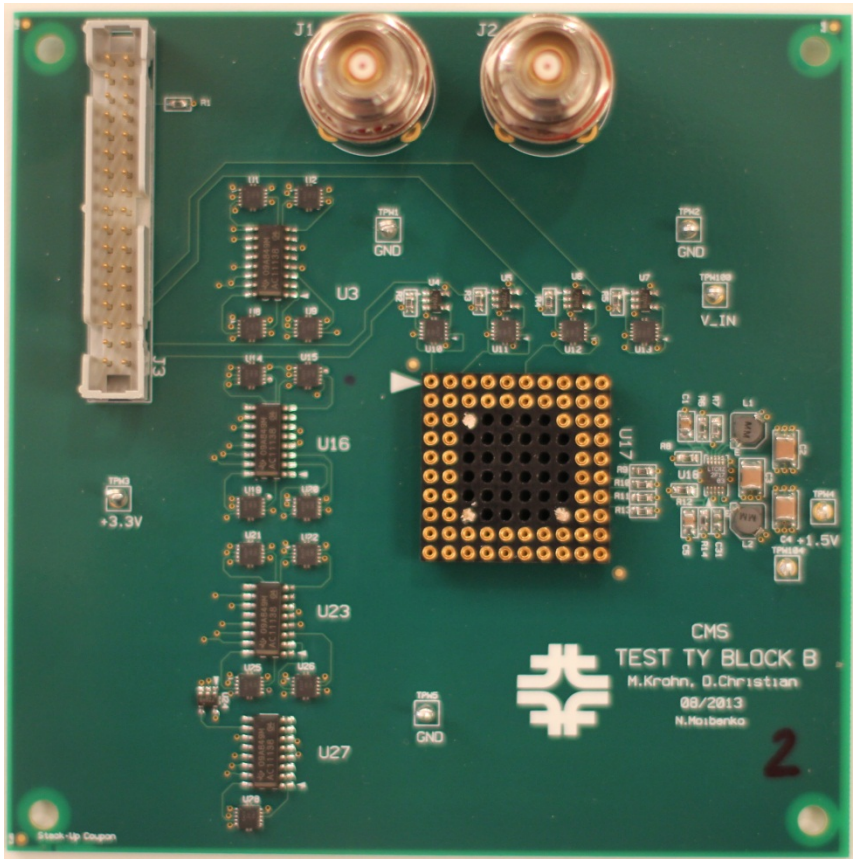
Sandia Gamma Irradiation Facility

- http://www.sandia.gov/research/facilities/gamma_irradiation_facility.html
- Three test cells with arrays of ^{60}Co sources (1 MeV gammas)
  - Sources shielded in pool of water; raised above water for irradiation
  - Sample held in basket above pool.
  - High dose rate possible
    - 1krad/sec typical (3.6Mrad/hr)
  - Large area with approx equal dose rate.



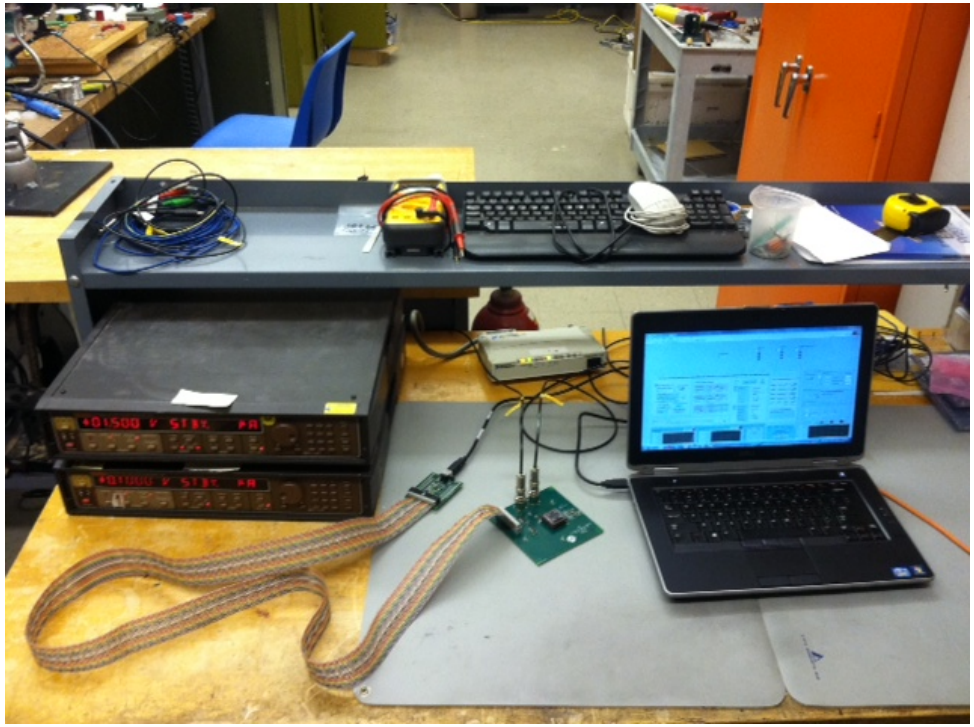
Measurement PCBs

- Test ICs bonded in pin grid arrays.
  - ~20 transistors bonded per package
- PCB provides power for protection diodes and connects SMUs to one transistor at a time
- Labview program selects which current switches are active – connects one SMU to transistor source/drain & the other to transistor gate.

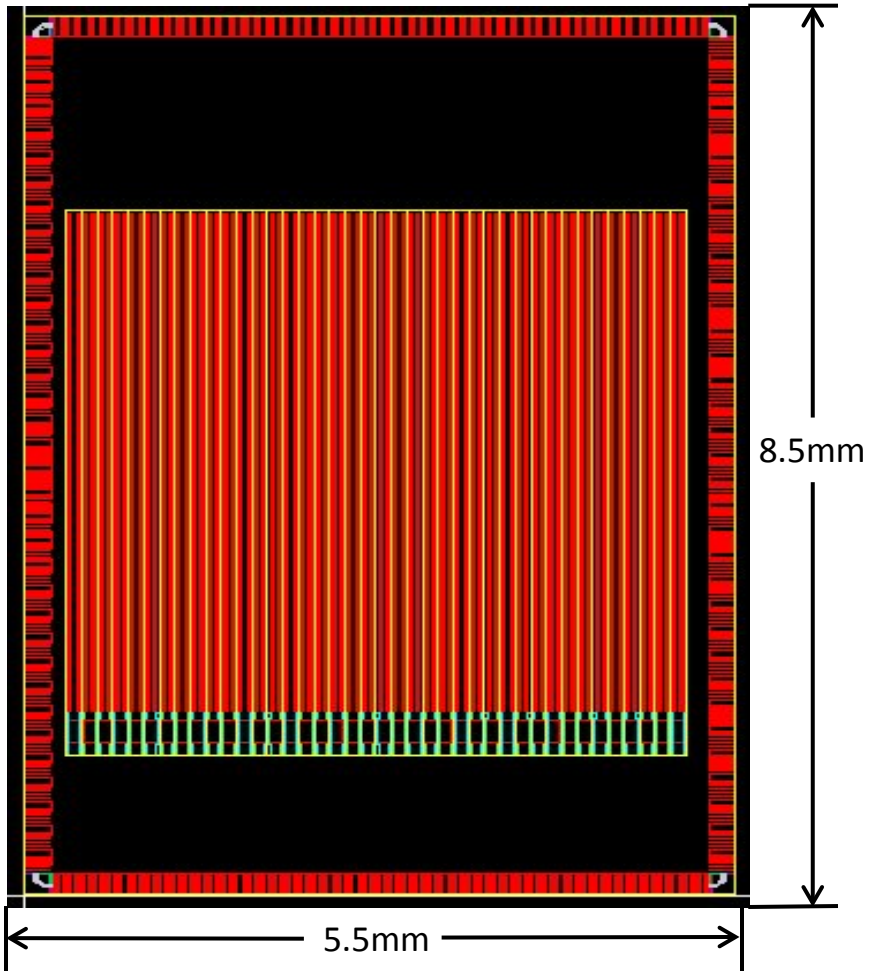


Simple “Portable” Measurement Apparatus

- For each transistor:
  - Set $|V_{ds}| = V_{dd}$
  - Sweep Vg ($0 – V_{dd}$)
  - Measure I_{ds} & I_g
- Extract
  - Leakage current (off state)
  - Transconductance g_m(max)
  - Threshold voltage V_T

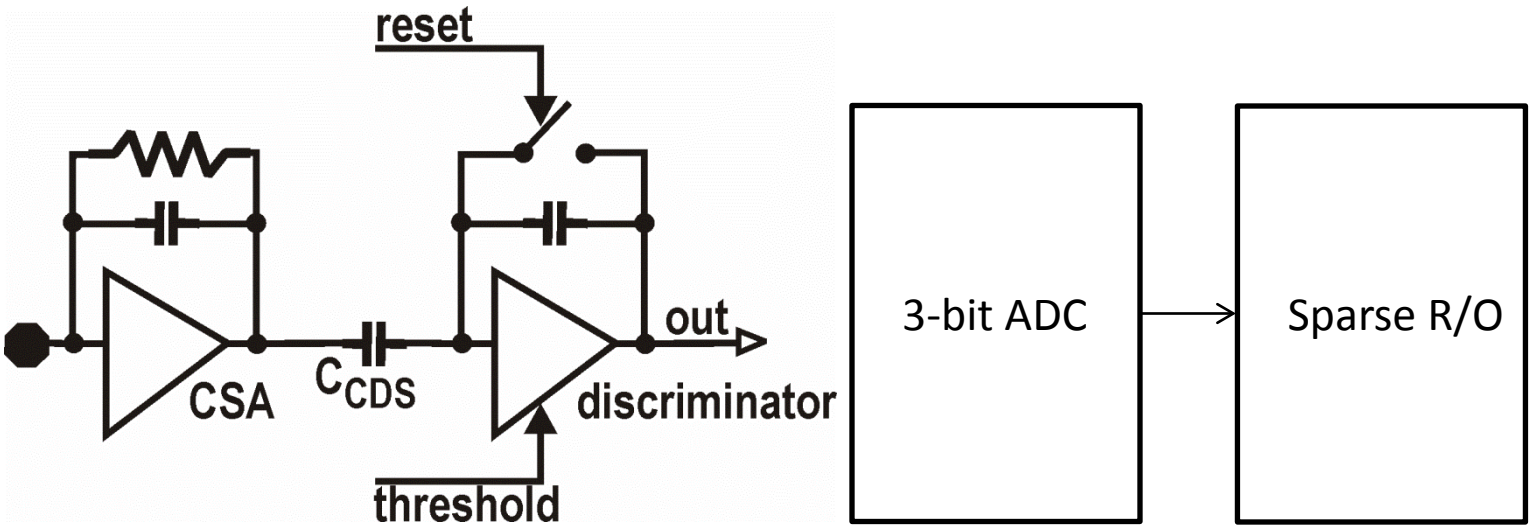


Small-Pixel Readout Chip



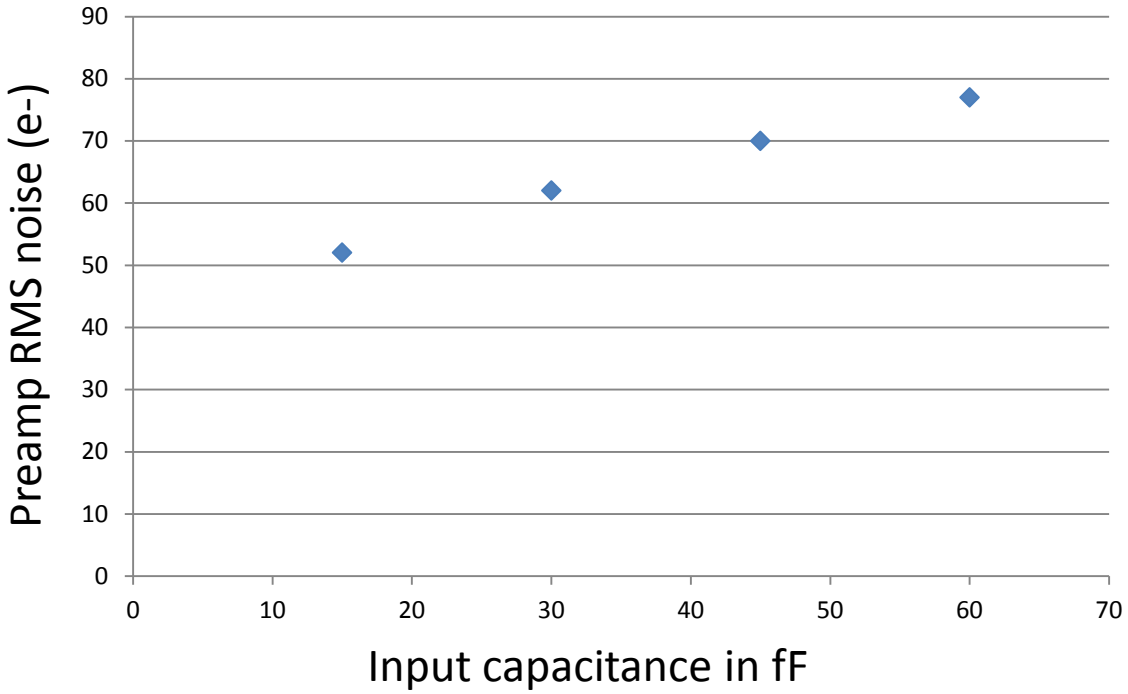
- Pixel unit cell = 30μx100μ
  - Amplifier ~ 20x20
  - ADC ~ 20x80
  - Digital logic = 10x100
- Two types of amplifier/ADC
  - ½ of array each
  - (Different) 3-bit ADCs in each
- Uses digital logic from other FNAL projects
- Zero-suppressed readout using priority encoder
- Normal readout at bottom; debug at top (including analog from selected cells); side pads accessible only when not bonded to a sensor.

Pixel Unit Cell



- Both FE cells use a synchronous front end, reset @40MHz:
  - Correlated double sampling with Δt=25ns removes low frequency noise.
  - Greatly reduces sensitivity to pile-up.
  - Designed so that current draw does not change during reset.

Simulation of Preamp#1 Yields Noise < 100 e^-



- Correlated double sampling adds a small amount of noise (total noise = 62 e- at C_{in} = 30 fF)
- Power Consumption: 5μA (preamp) + 8μA (all comparators)
  - 433 mA/cm^2 = .65W/cm^2 (1.5V)

Test ROC timeline

- Fabricate test ROC in Global Foundries 130nm CMOS
  - Submission expected in January 2014
- Test bare dice
  - March – April 2014
- If OK
  - Bond to sensors included on Phase-1 prototype sensor wafer
  - Bond to diamond sensors (Colorado)
  - Bench test with sources
  - Beam test
- Translate (at least analog circuits) to 65nm (as part of RD53)
  - Fabricate either small blocks or ROC
  - Compare circuit performance w/130nm version