VeloPix ASIC

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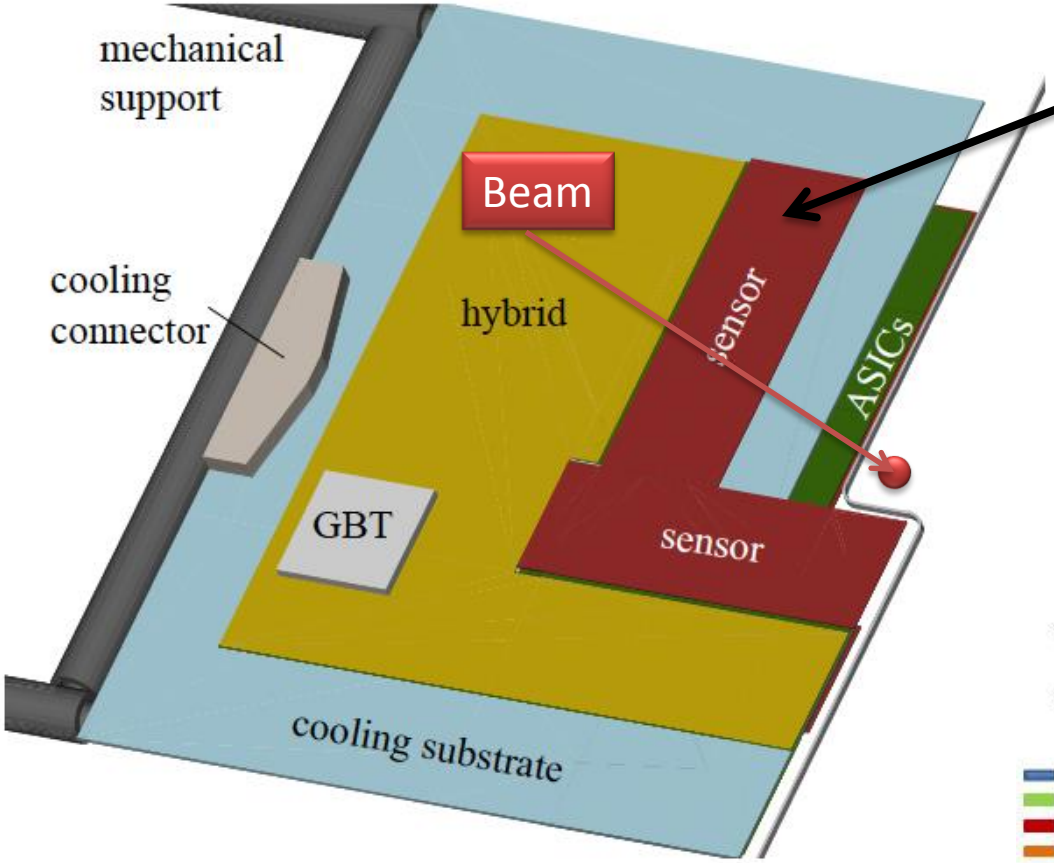
and others

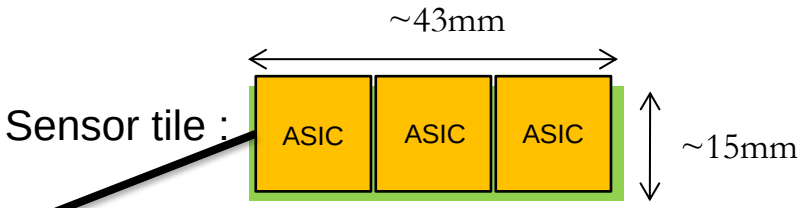
outline

Note that the architecture of the VeloPix ASIC is not part of this review
However, since the VeloPix produces all data that has to be handled by the DAQ it is presented here in some detail

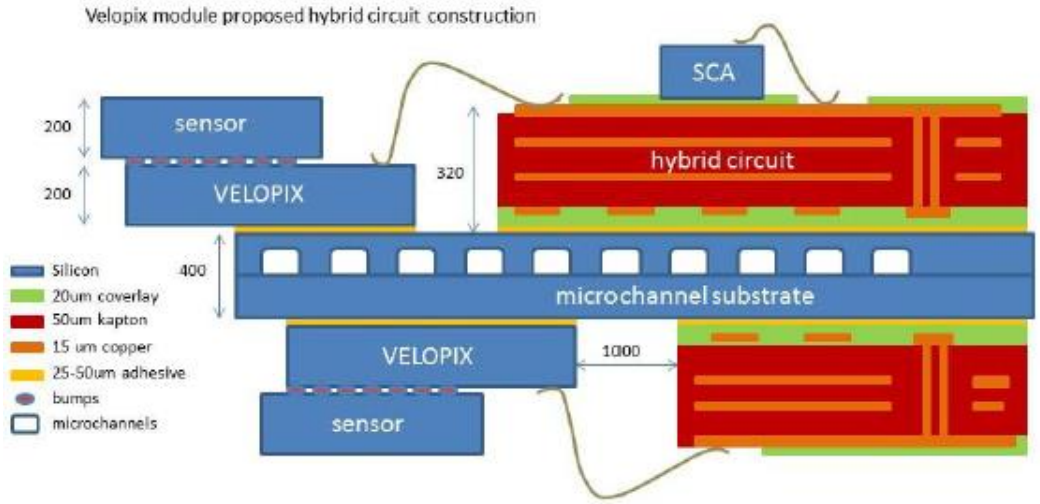
- Introduction
- Data rates from physics simulation
- VeloPix architecture / features
- Data format
- Slow / fast control

VeloPix module overview





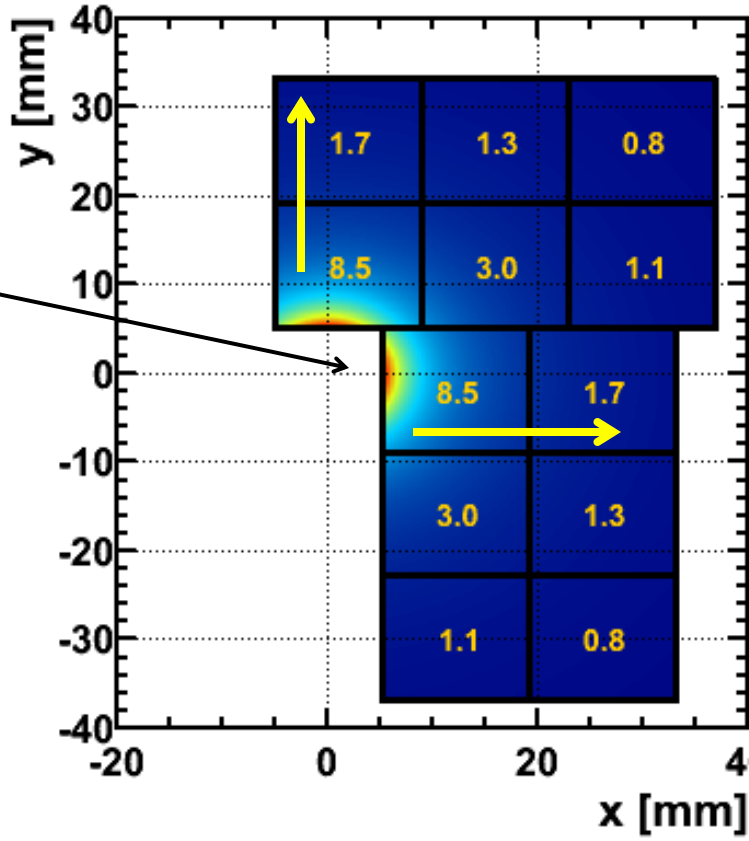
- 4 sensors per module
- One sensor = 3 ASICs
- VeloPix ASIC based on Timepix3
- Each ASIC has 256x256 pixels
- 55 x 55 μm^2



Track rates & radiation

for L = 2x10^{33} and R_{min} = 5.1 mm, 2400 bunches, ν = 7.6

- **Non-uniform occupancy, large variation in average rate from chip to chip**
- **Average # particles / chip / event**
  - **event = colliding bunch**
  - **average (peak) rate: multiply by 26.8 (40) MHz**
- **Hottest chip 8.5*26.8 (40) = 230 (320) Mtrack/s**
- **=> ~ 600 (890) Mhits/s per chip**



Radiation levels:

- **Order of 400 MRad in 10 year life time**
- **and about 8.10^{15} 1 MeV n_{eq}**
- **rad. tolerance demonstrated for this 130 nm technology**

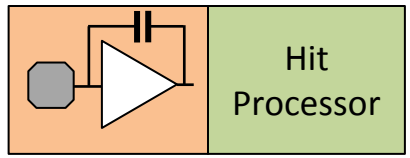
VeloPix

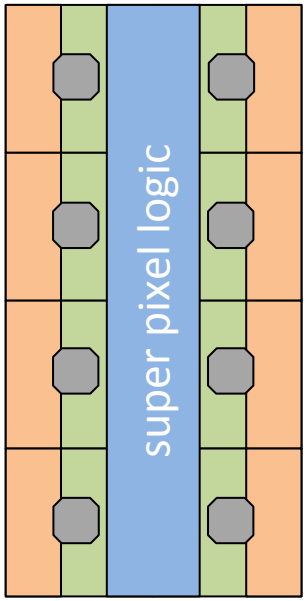
- VeloPix is based on Timepix3
- But has to cope with ~10x higher pixel hit rate
- 65k pixels, 55x55 um^2 each
- 130 nm technology
- Chip dimension 14.1 x ~17 mm
- Both TPX3 and VeloPix have a data driven readout

- VeloPix is a binary pixel chip
  - When a hit is registered
  - It is combined with other simultaneous hits in the same super-pixel
  - A 9-bit timestamp (BCID) is added
  - And the packet is sent off-chip immediately
- Advantages of binary readout: fixed pixel format, smaller data volume

Super pixel

- Typical cluster size of 2 .. 4 pixels
- -> beneficial to combine 2x4 pixels in a so-called super-pixel
- Removes duplicate address and timestamp information compared to single pixel data packets
- Bandwidth gain of 30-40%
- Super-pixel (SP) has fixed boundaries
- Share logic in centre of SP
  - requires less area for routing

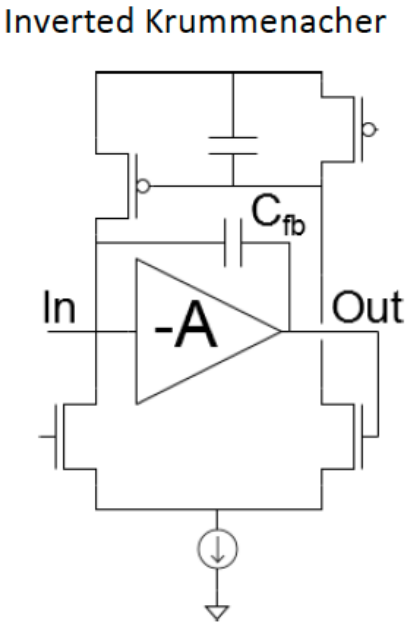


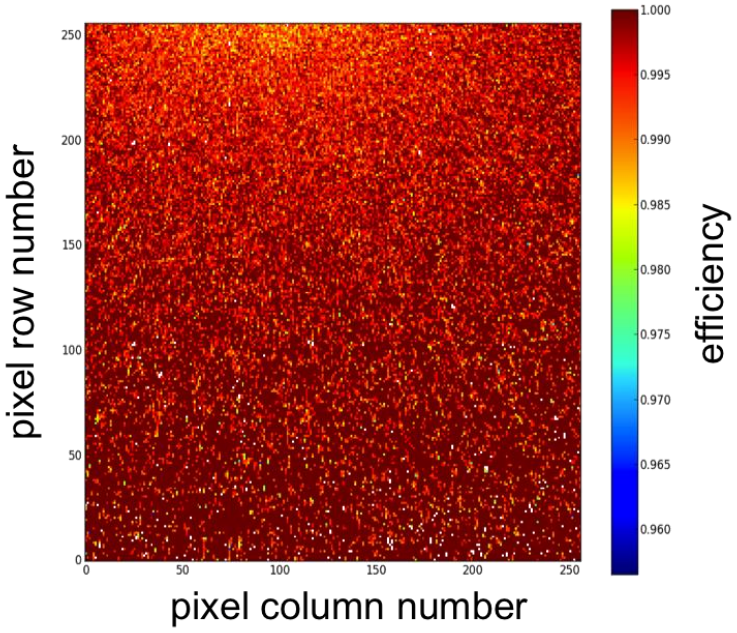


Massimiliano de Gaspari

Analog Front-end

- **Inverted Krummenacher scheme**
  - decouples discharge current from leakage current compensation current
- **Large discharge current reduces dead time and hence pile-up**
- **Considering to add a fast clear for large signals**
- **About 1% loss of hits for an average dead time of 200 ns**





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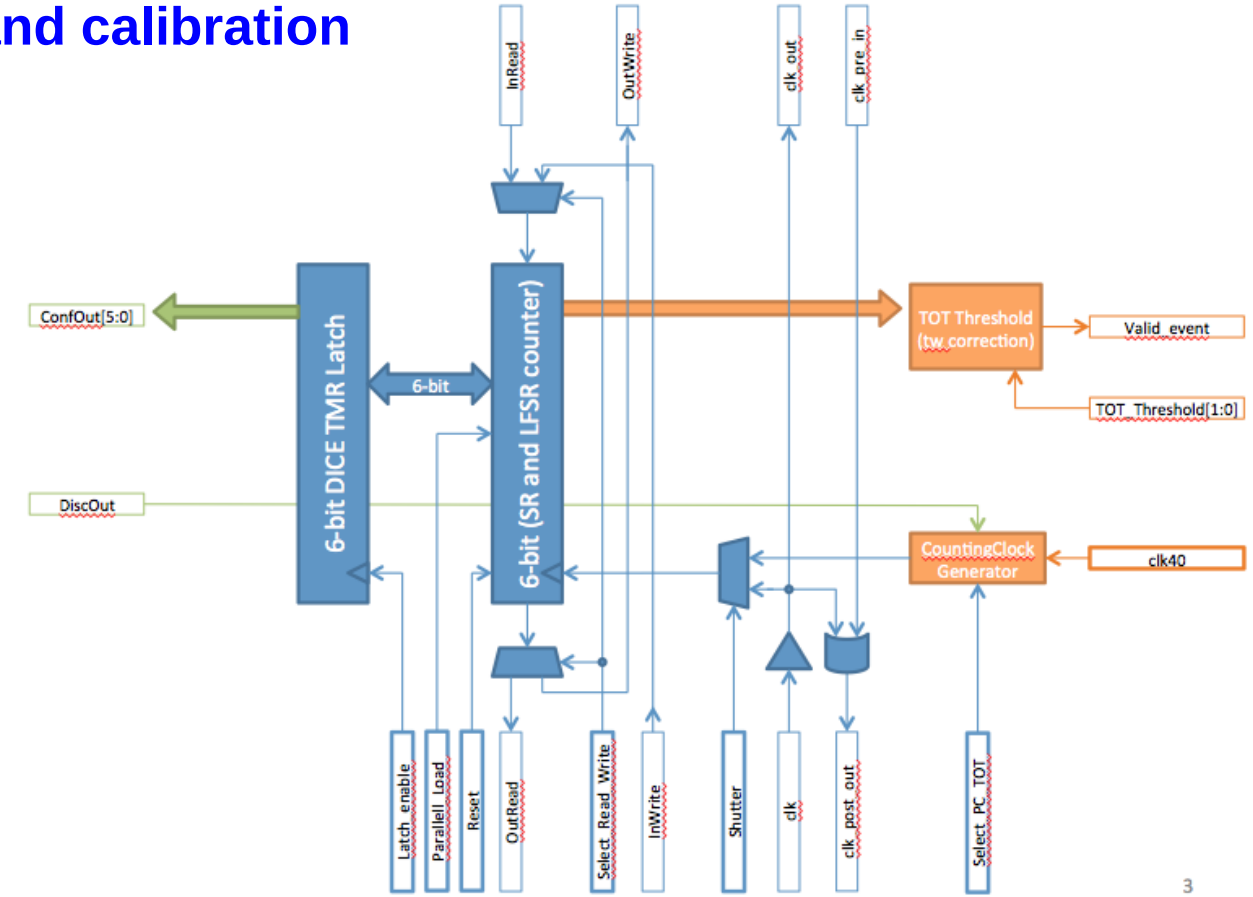
Xavi Llopart

Pixel digital

- Normal operation mode: binary
- Front-end can do Time-over-Threshold (ToT) measurement
- Readout of ToT in special mode, and readout via (slow) ECS interface
- Only for monitoring and calibration



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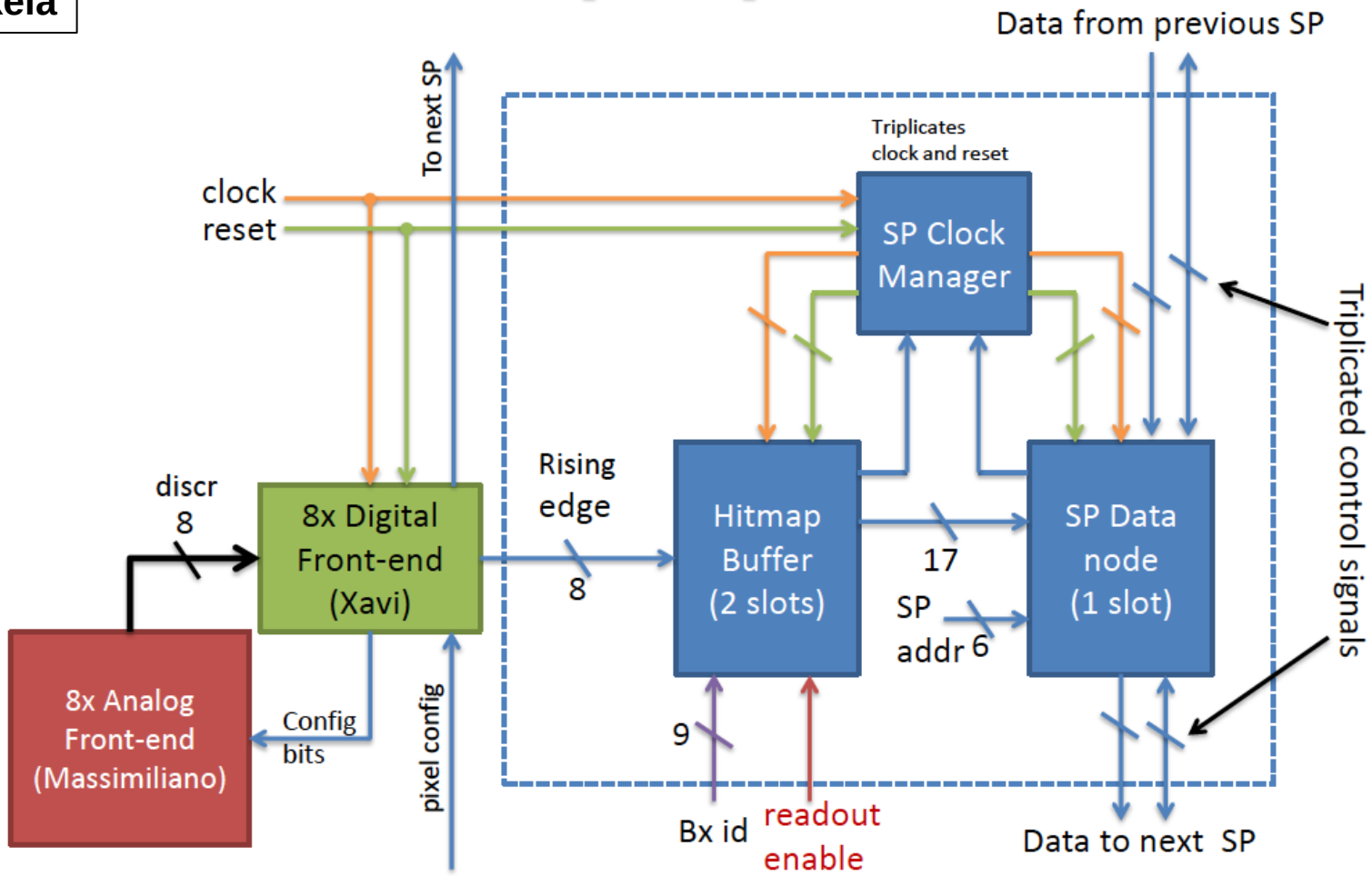
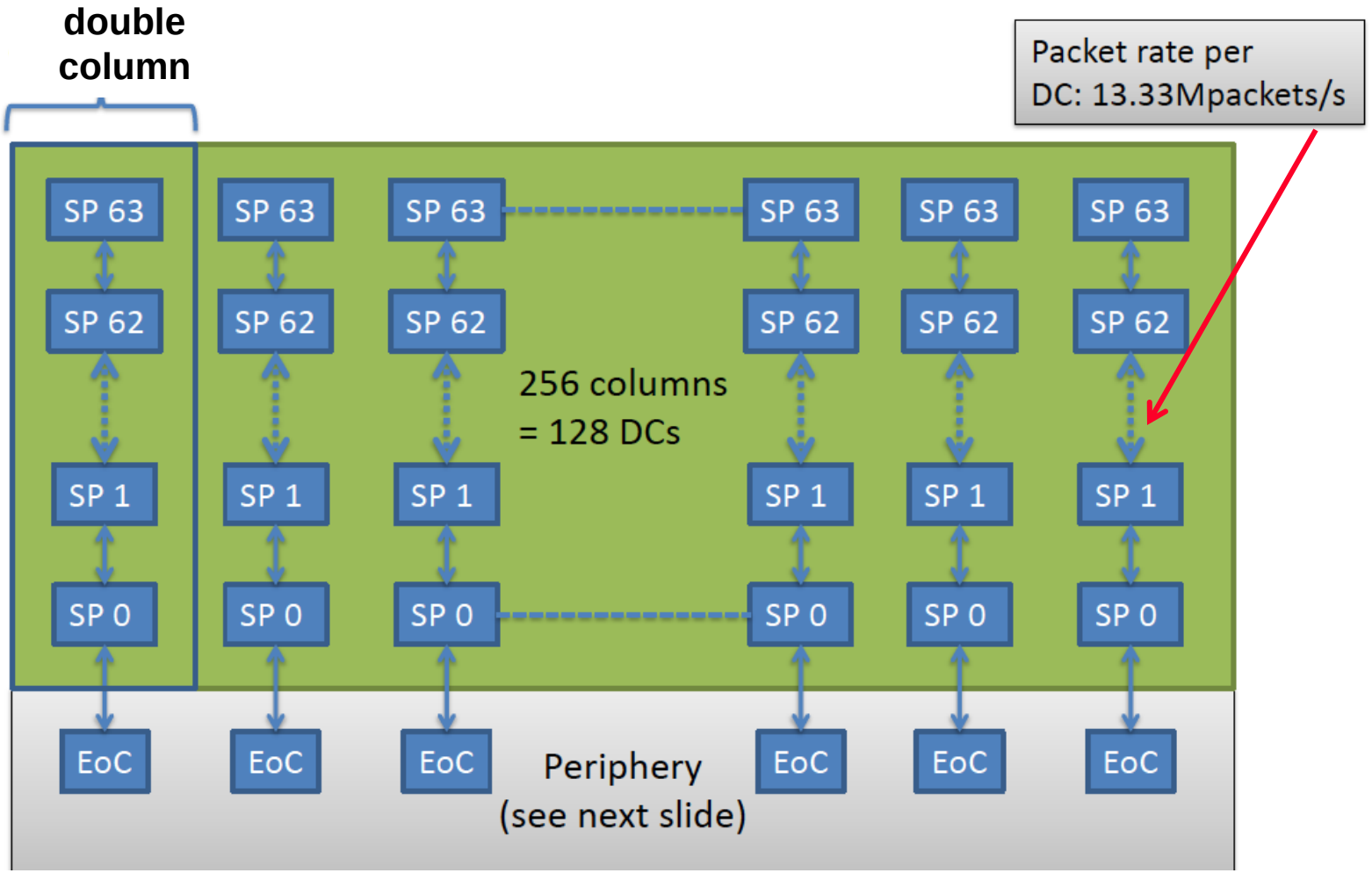
Super pixel



- **2 common buffers per super pixel**

Tuomas Poikela

Double column readout



- Packets ‘trickling’ down
- More latency, but also more buffering
- 23 bits bus, 3 cycles per transfer -> 13.3 Mpacket/s

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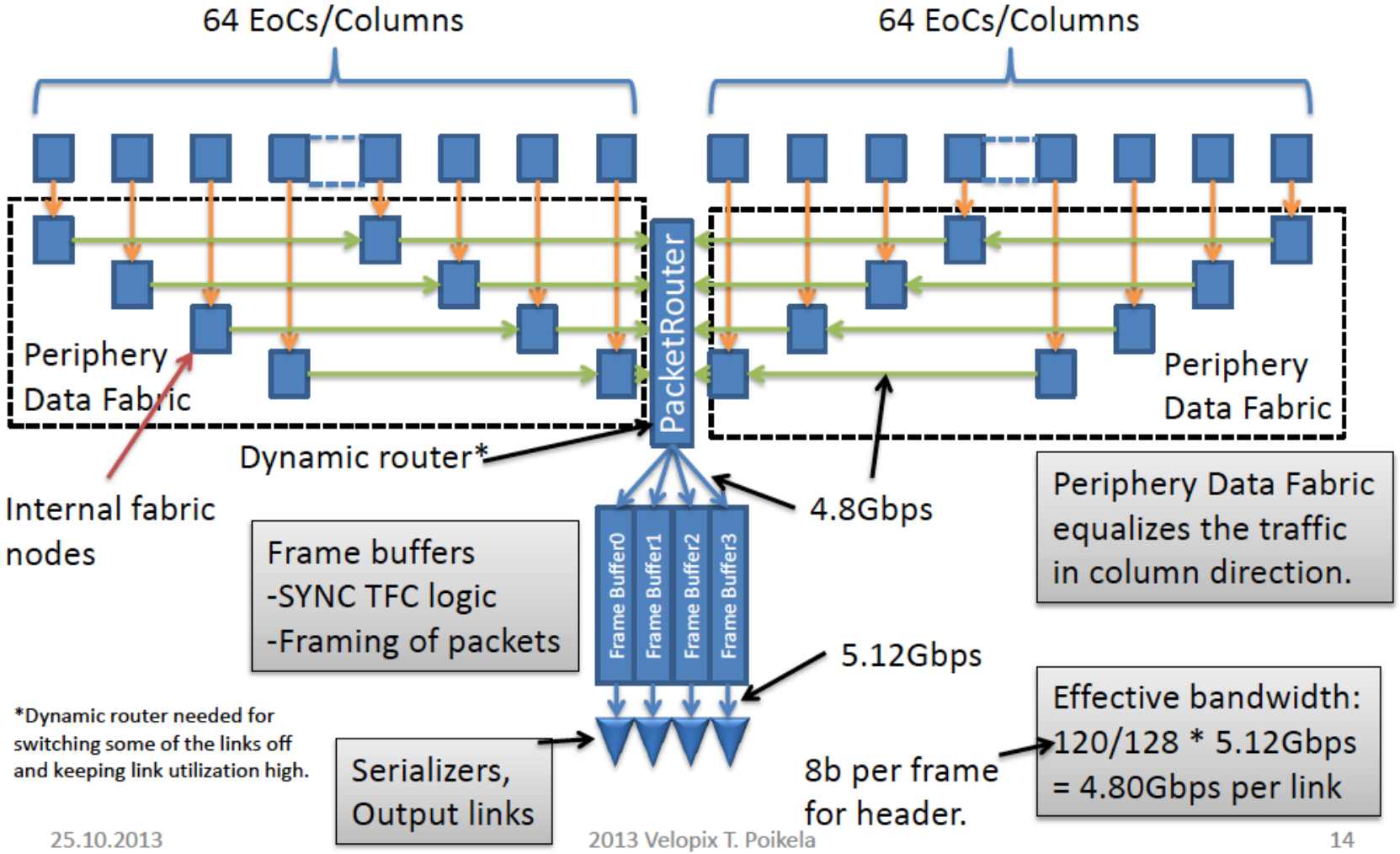
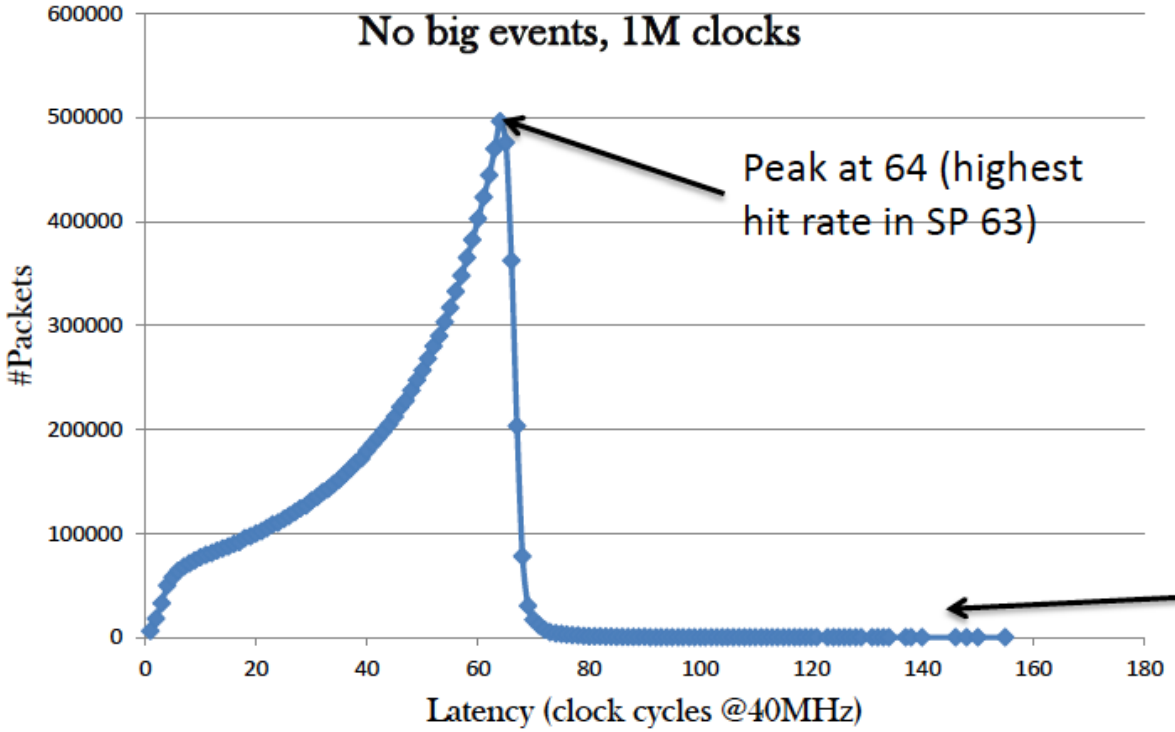
Tuomas Poikela

End of Column



data-packet latency

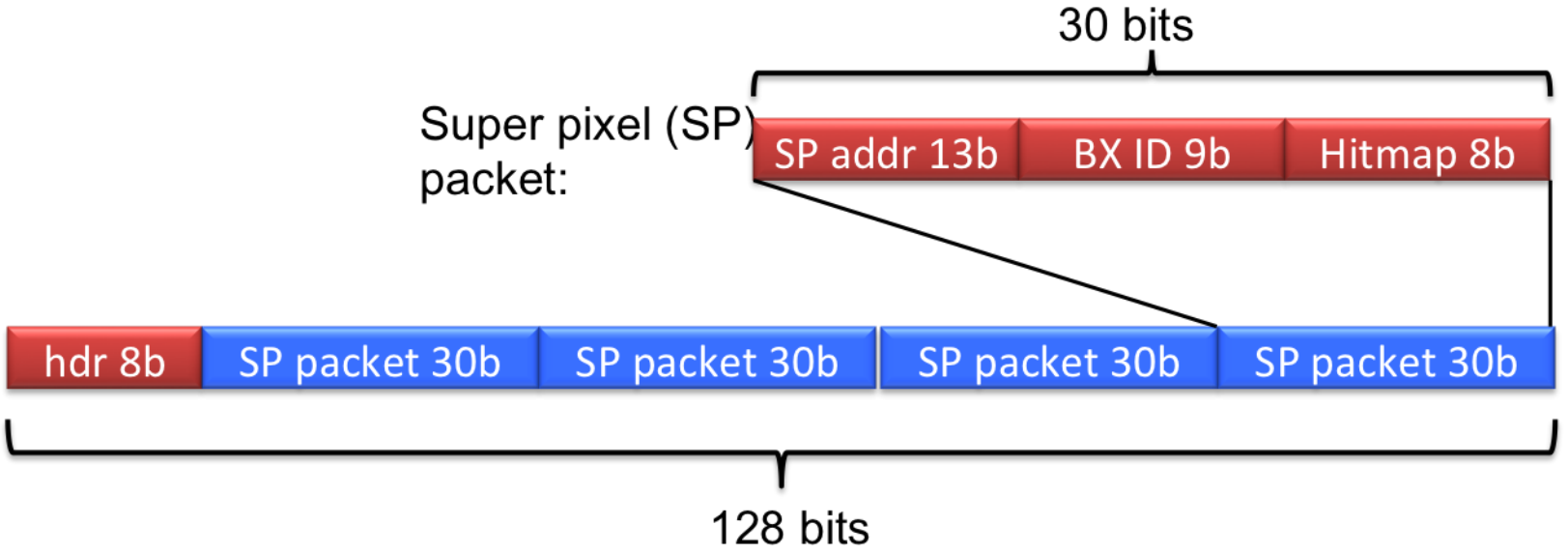


Efficiency: 99.99%
Hit rate: 840 Mhits/s
Packet rate: 505 M/s
Data rate: 16.2 Gbps
Hits per packet: 1.66

- Packet latency peaks at 64 due to pipelined Double Column readout
- Drawback is that data packets are not ordered in time
- Reordering required before other processing steps like clustering can be done
- Must done by off-detector electronics (TELL40)

Data format

- ~900 Mhits/s for hottest ASIC
- Packed into super-pixel packets: 2x4 pixels
- ~520 Mpackets/s, 30 bits each
- -> required effective bandwidth ~16 Gbit/s
- 4 SP packets in 128 bit frame
- 8 bit header: 4 bit fixed (0x5) and 4 parity bits
- SP packets are scrambled to reduce probability of long 0/1 sequences



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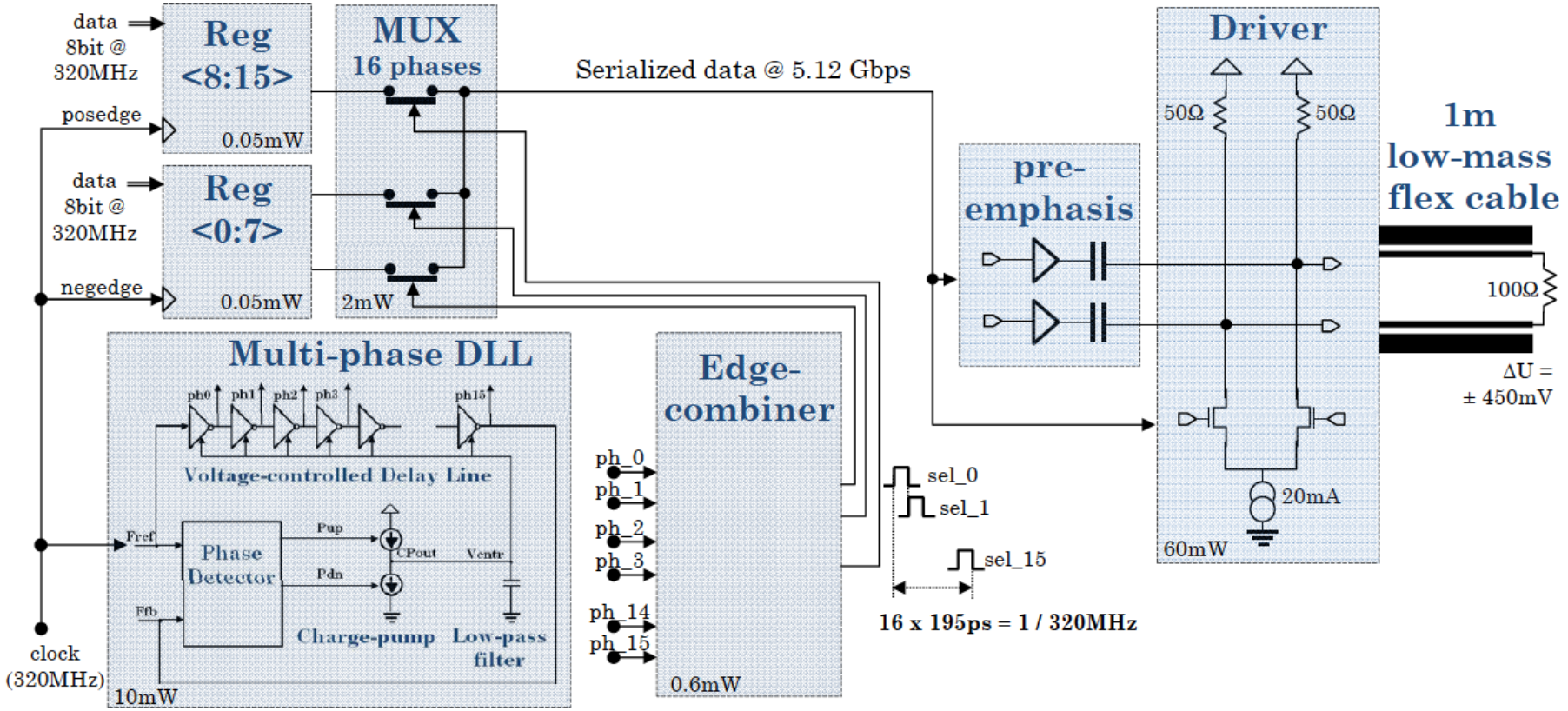
Vladimir Gromov

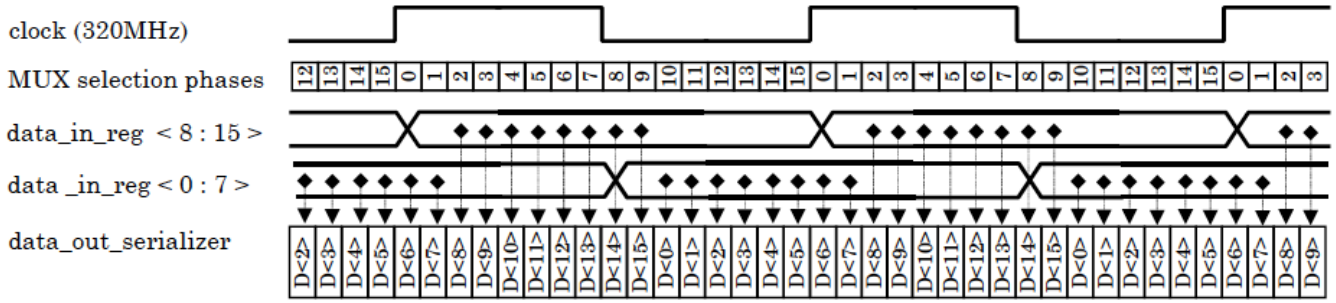
High speed serialiser

- 2 options
- GBT-serialiser (back-up)
  - 120 bits frame of which 112 are available for pixel data
  - Input format 120 bits @ 40 MHz
  - effective 4.48 Gbps per GBT-serialers
  - total bandwidth 17.92 Gbps
  - not plug and play from GBT, because of different metal stack (LM vs DM)
- GWT: lower power, better matches the VELO data format, line driver with pre-emphasis
  - 128 bits frame of which 120 are available for pixel data
  - Input format 8 bit @ 320 MHz DDR
  - effective 4.8 Gbps per GWT-serialiser
  - total bandwidth 19.6 Gbps
- Technical review of GWT testchip last Monday
  - will submit testchip in February 2014

Gigabit Wireline Transmitter (GWT)

Vladimir Gromov





Pre-emphasis GWT line driver

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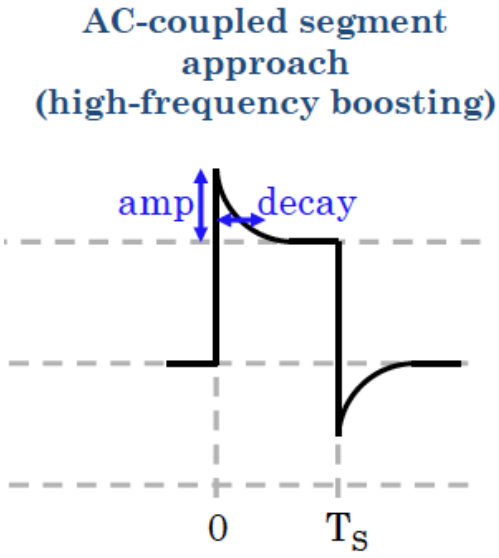
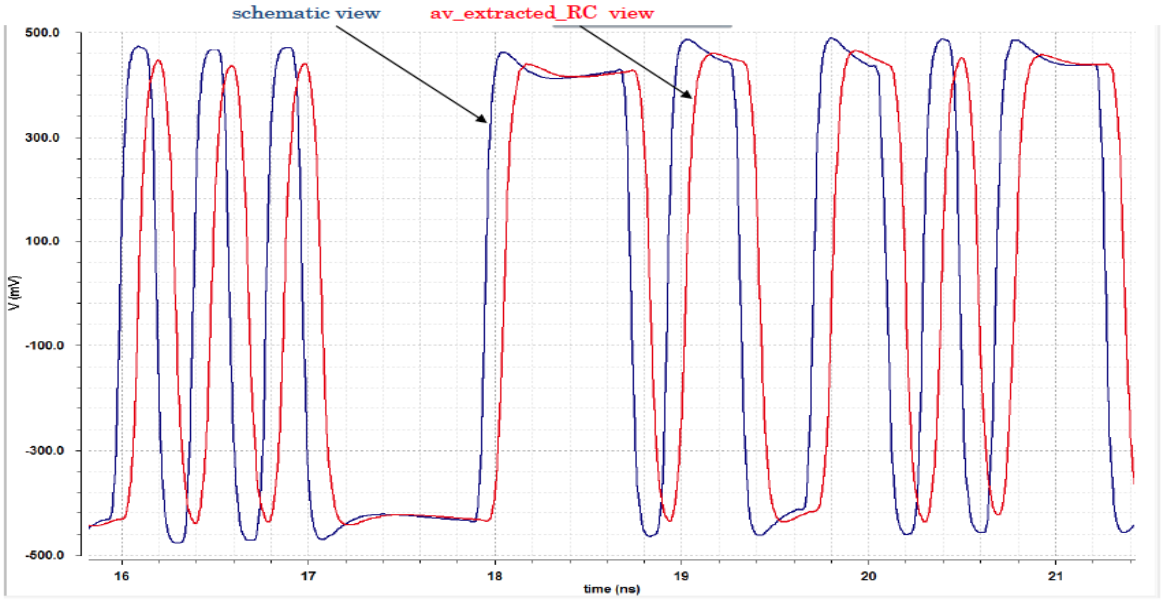


- Pre-emphasis via AC coupling
- Simulation of extracted circuit
- Includes (tuned) model of proto-type flex cable



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Fast control

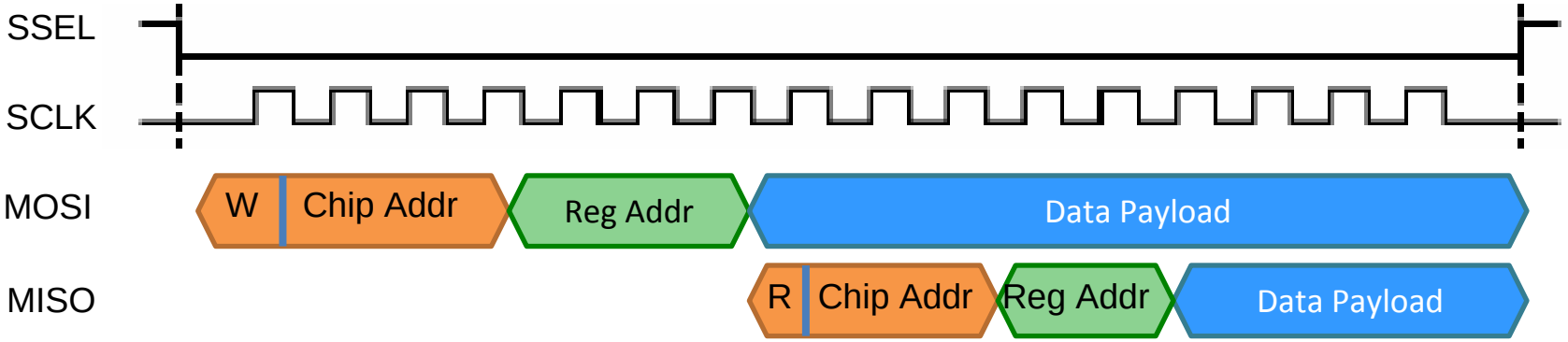
- 5 TFC signals will be provided via the GBTx on the hybrid
- Decision on point-to-point or multi-drop bus to be taken
  - either single PtP line at 320 Mbps
  - or 5 parallel lines (multi-drop) at 40 Mbps
- The VeloPix will respond to the following TFC signals
- Front-end reset
  - Clears all data from all buffers, but will not reset the configuration settings.
  - Requires up to 64 clock cycles
- Bunch count reset
  - Checks and preload its internal 12-bit BCID counter with a configurable offset value.
  - Reset should arrive at expected count, if not latch current value and increment error count
- Sync
  - Sends a predefined (configurable) pattern on its serialisers.
- Snapshot
  - The ASIC instantaneously captures the values of all internal counters. Readout via ECS
- Calibration (testpulse)
  - Timing signal for testpulse
- The VeloPix can not provide non zero-suppressed data
- Nor can it respond to the BxVeto

Vladimir Zivkovic

Slow control

- Slow control data is set/read via GBT e-ports
- Point to point connection between VeloPix and GBTx
- Data rate 80 Mbps
- All registers can be read back (non-destructive read)

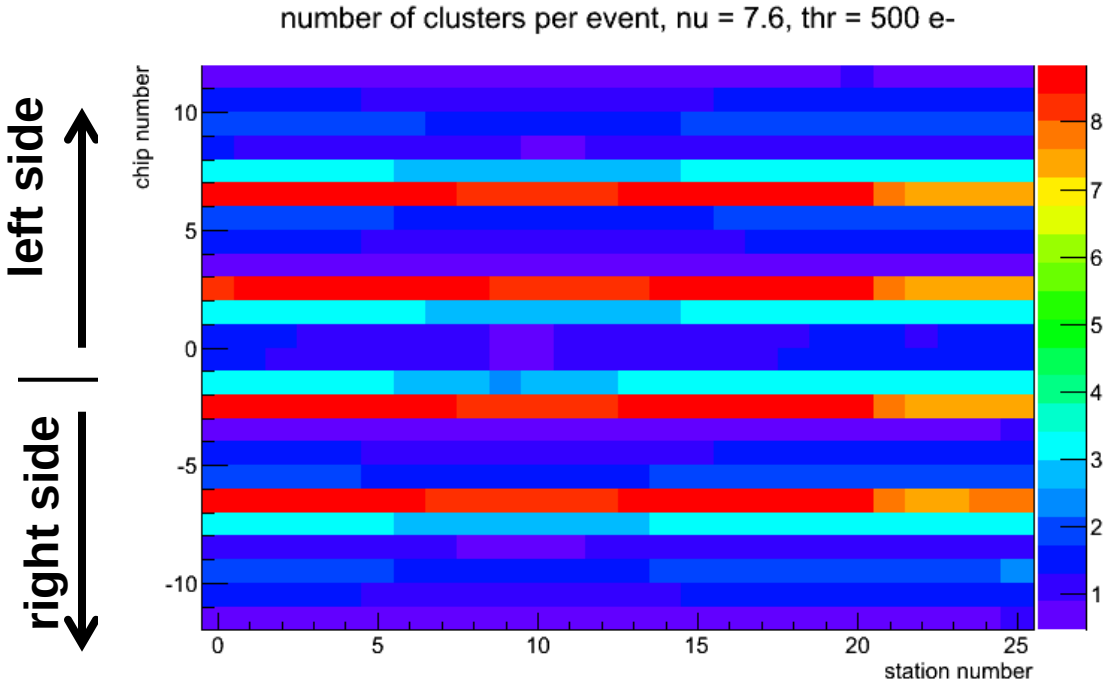
- To be decided whether we use an SPI like protocol using SSEL
- Or whether we use a single e-port and a sync-header

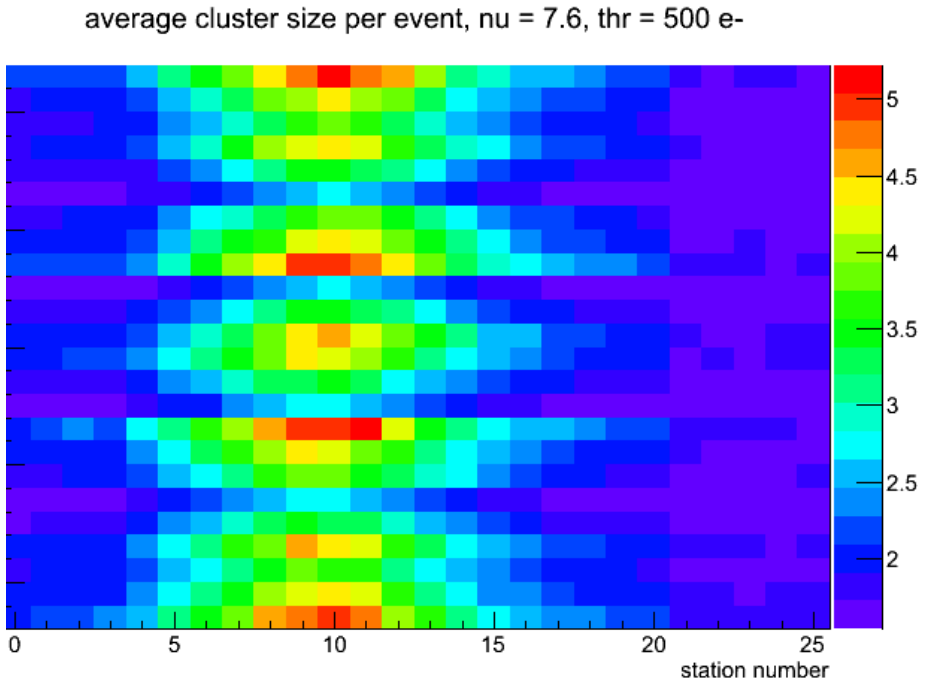


Backup slides

Cluster rate/size versus position

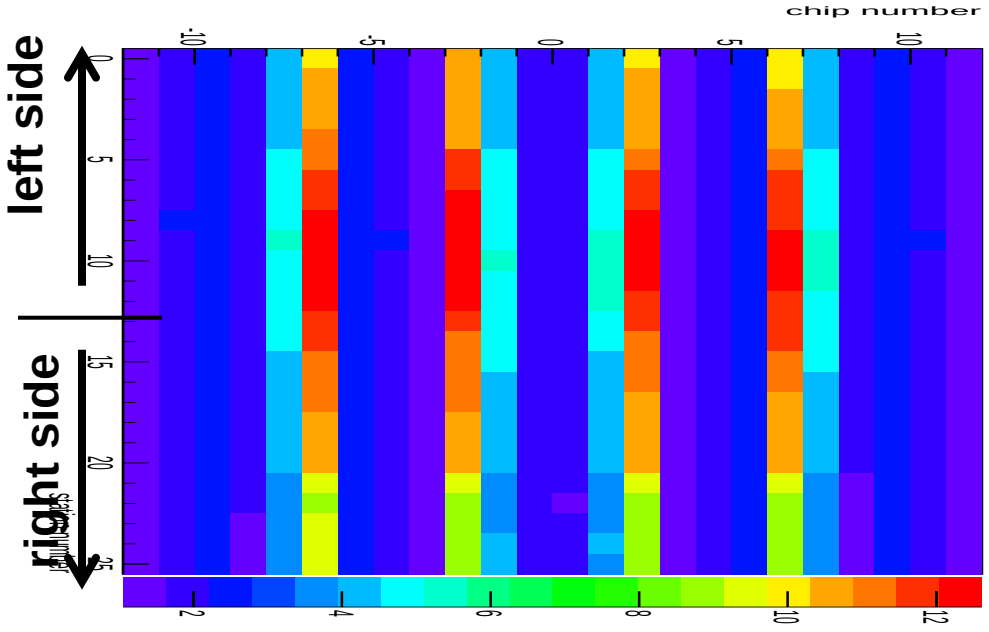
- peak value of 8.83 clusters/event for hottest chip
- Average clustersize is ~2.2
- Regions with a high track density have an (almost) average clustersize
- Large clusters in low occupancy region

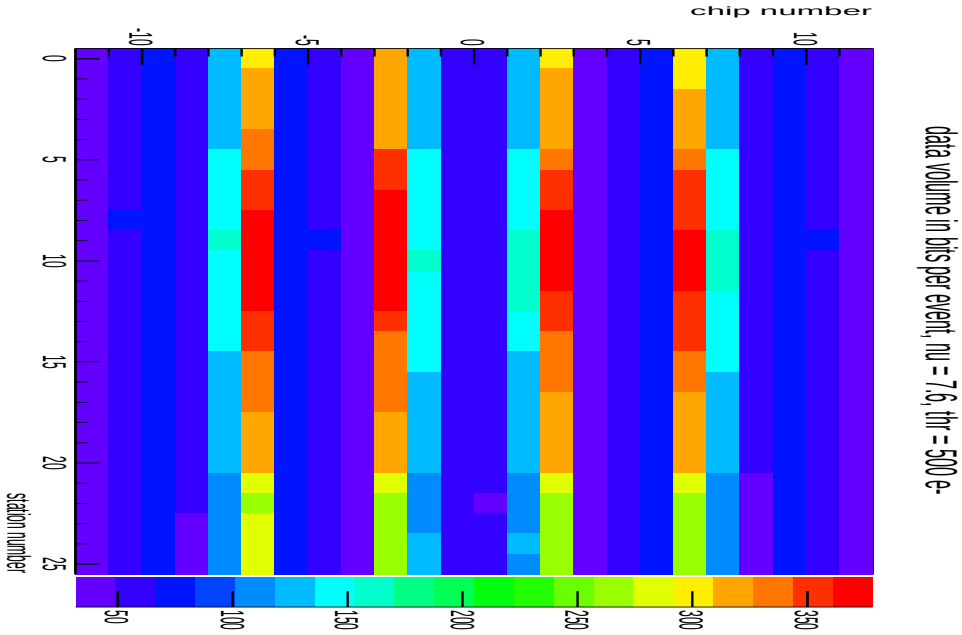




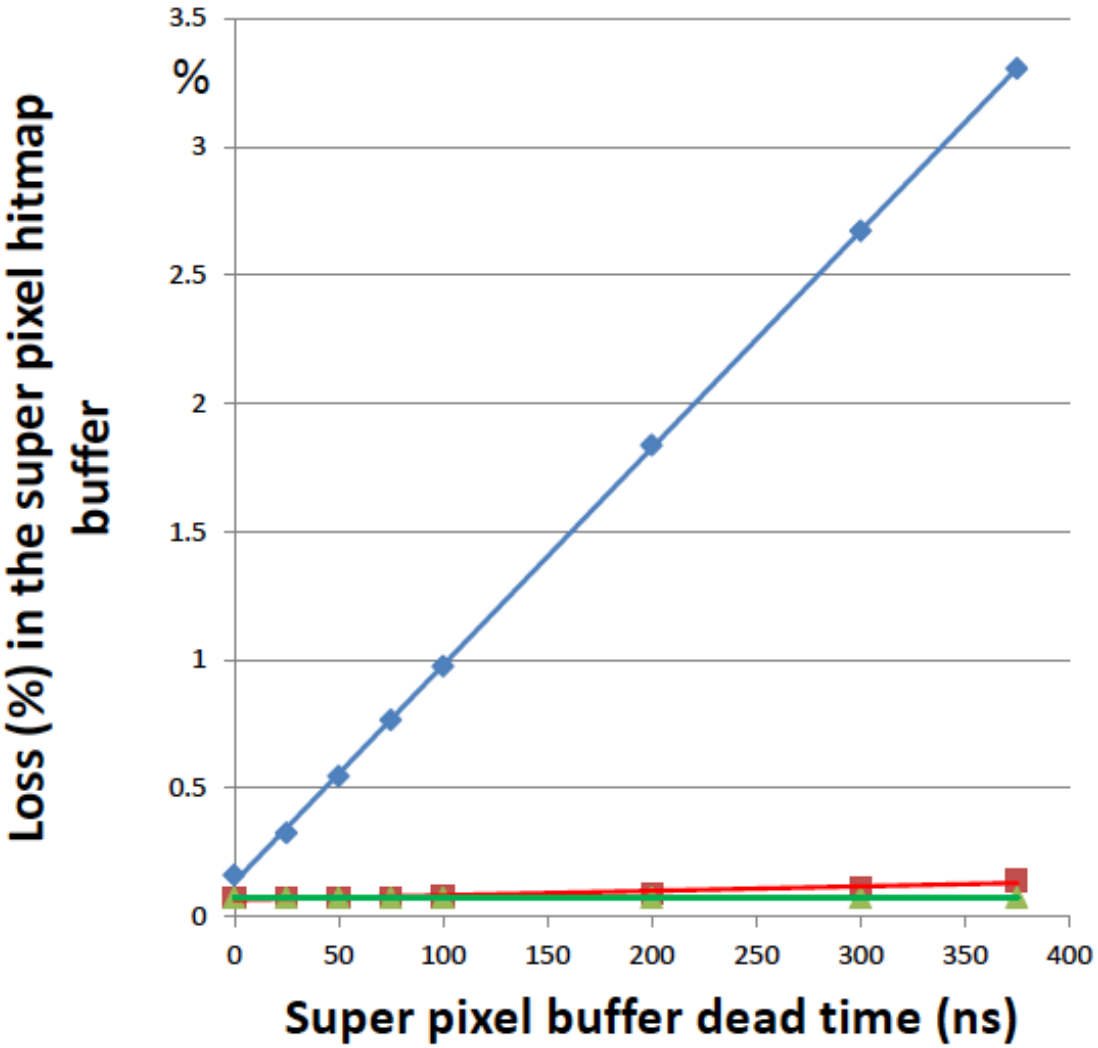
SPP rate versus position

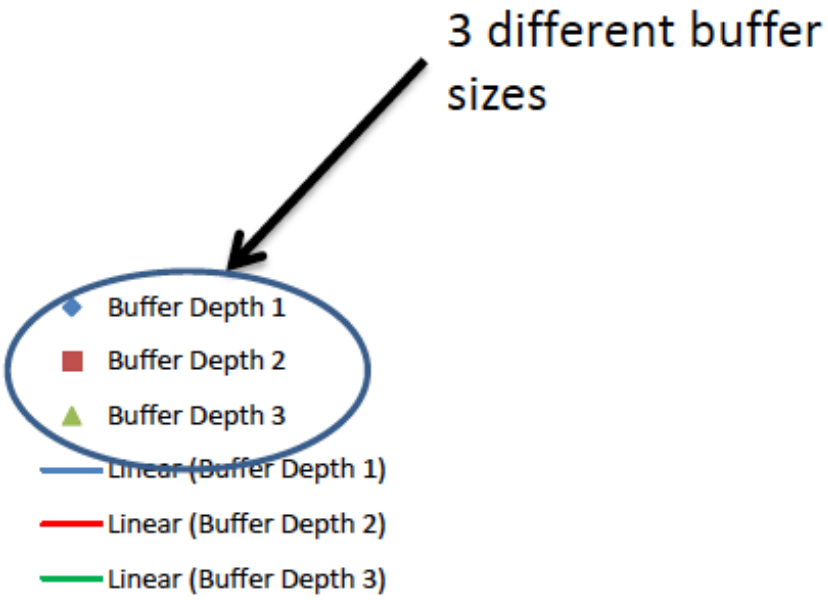
- average value of 12.6 clusters/event for hottest chip
  - -> ~520 Mpackets/s without large events
- Average # pixel hits in SPP = 1.6
- Regions with a high track density have an (almost) average clustersize
- Large clusters in low occupancy region





Buffer depth





Super pixel must be able to store at least 2 SP packets!

VeloPix specifications

VeloPix Features ($L=2x10^{33}$ $cm^{-2}s^{-1}$)	
Pixel size	55 µm x 55 µm
Pixel matrix array	256 x 256
Super pixel size	2 x 4 pixels
Dynamic range	50 ke^-
Timewalk	< 25 ns (@ 1ke^-)
Time stamp (Bunch ID)	40 MHz (25 ns resolution)
Operation modes of pixel	Binary, ToT via ECS only
Timestamp	9 bit
Readout mode	data driven (data push), superpixel packets
Sustainable hit rate	average 600 MHits/s, peak 900 MHits/s
Power consumption	< 3 Watts per chip @ 1.5V (1.5 W/cm^2)
Output bandwidth	~ 16 Gbit/s peak
Radiation tolerance	> 400 MRad