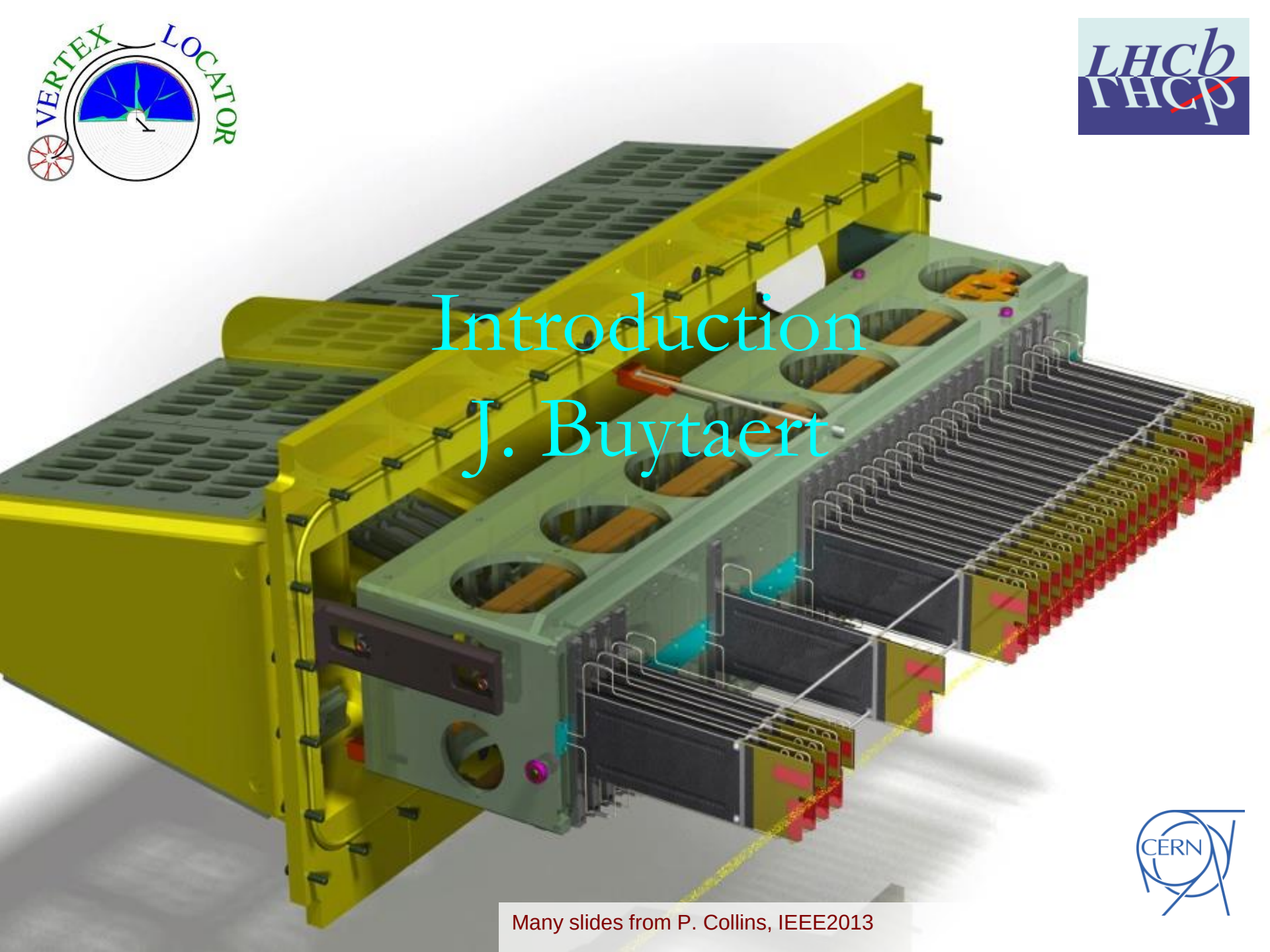


Introduction

J. Buytaert

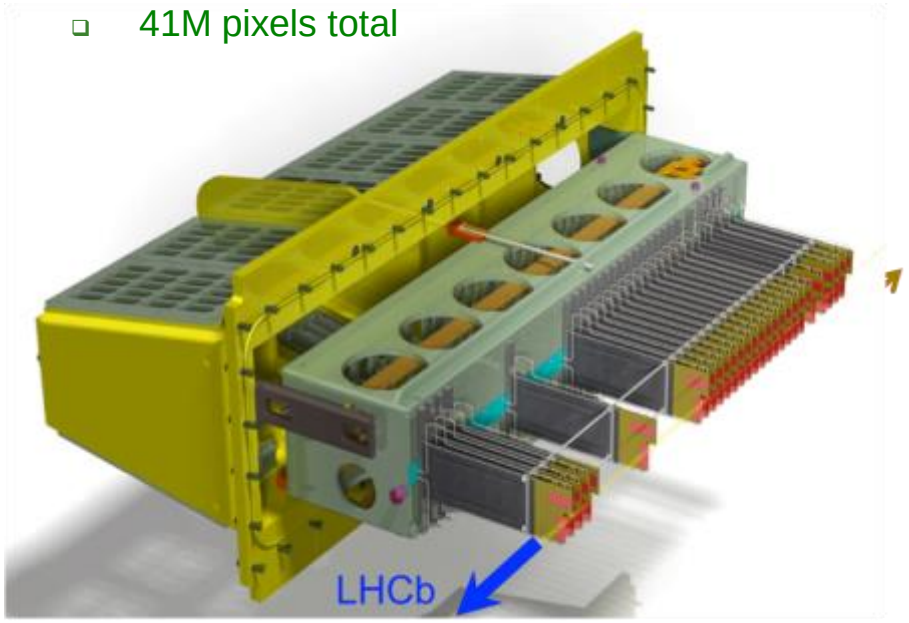
Many slides from P. Collins, IEEE2013

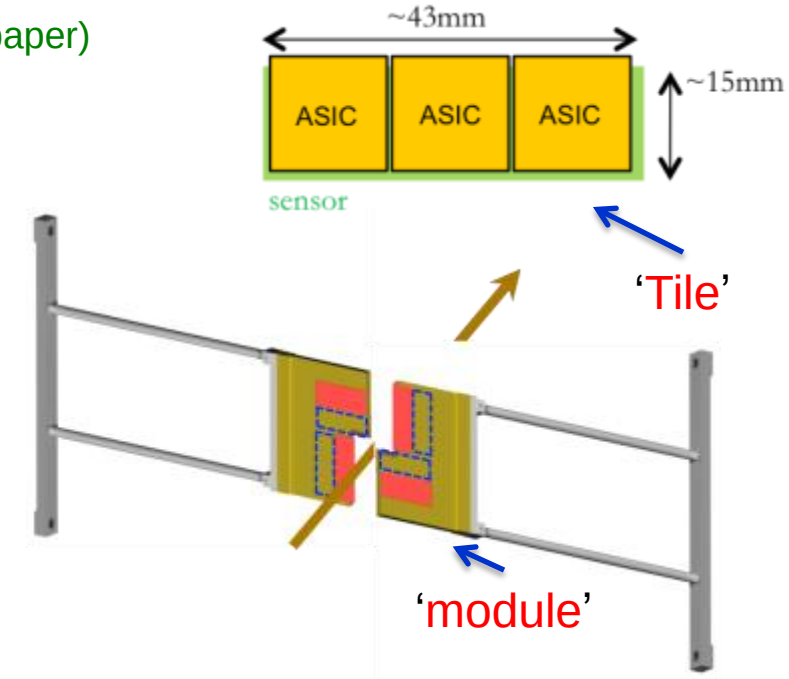
Upgraded VELO (VErtex LOcator)

Function of VELO remains: provide precise tracking and trigger on displaced vertices

Conditions more challenging: increased occupancies, data rates and radiation damage

- Choice for pixels vs strips was made on 17th July 2013
- L shape modules face each other to form stations
- 4 sensor tiles per module. Each sensor has 3 ASICS with 55 x 55 μm^2 pixels
- 26 stations arranged perpendicularly along beam direction
  - total active area 1237 cm^2 (= size of A3 sheet of paper)
  - 41M pixels total



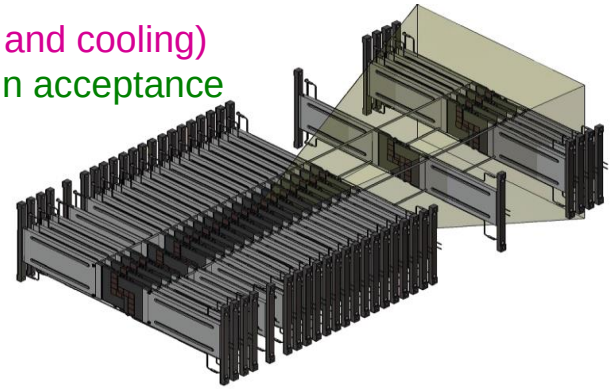


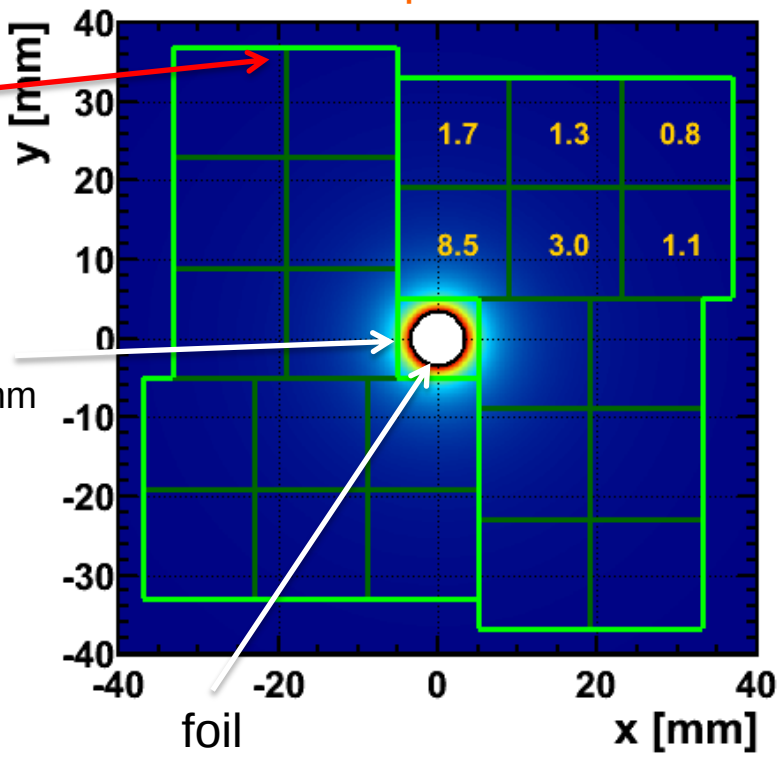
Challenges for upgraded VELO

Sensor Radiation Damage
- Highly non-uniform radiation damage of up to 8 x 10^{15} n_{eq}/cm^2 for 50 fb^{-1} (= full lifetime super LHC)
- Factor 40 less at sensor outer corner
- Expect up to 7nA per pixel and 130 mW per tile
- ASICS must tolerate 400 MRad

Enormous Data Rates
- ~8.5 tracks/collision for hottest ASIC
- Hottest chip 230-320 Mtrack/s
- 600-900 Mhits/s/ chip
- Data volume of whole VELO: 2.5 Tbit/s

Material Budget (thinning and cooling)
- Modules are partially in acceptance
- Thin foil essential





Pixel module layout superposed above anticipated flux (arbitary scale)

Micro-channel cooling

The challenge:

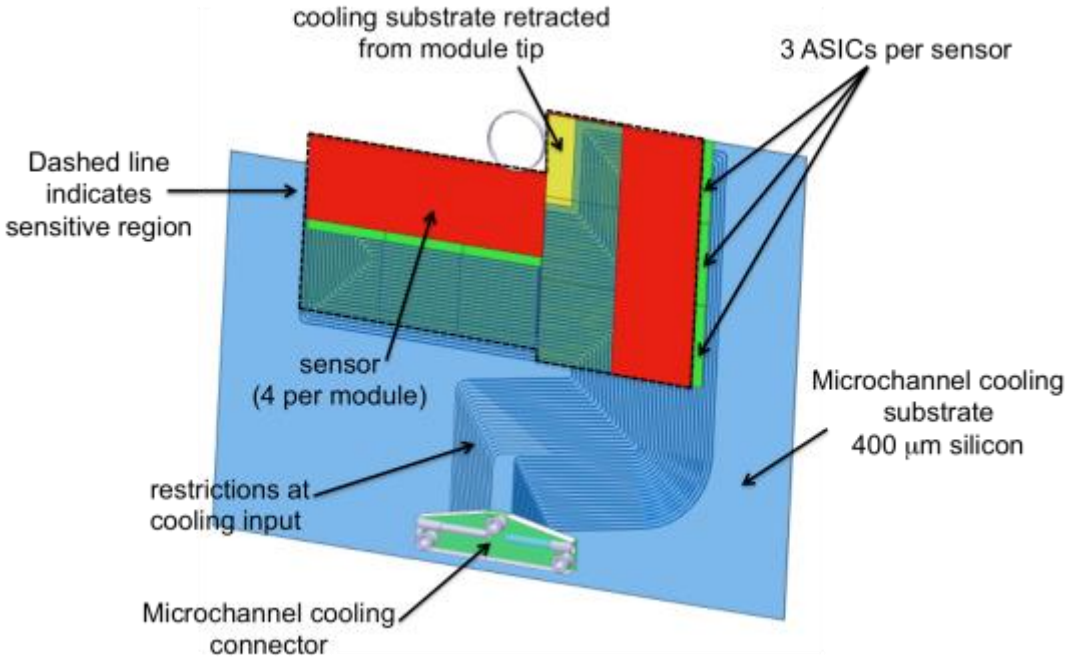
High speed pixel readout chips produce a lot of heat (~ 1.5 W/cm^2)

Necessary to keep the sensors at < -20 °C to minimize the effects of radiation damage, and to avoid thermal runaway

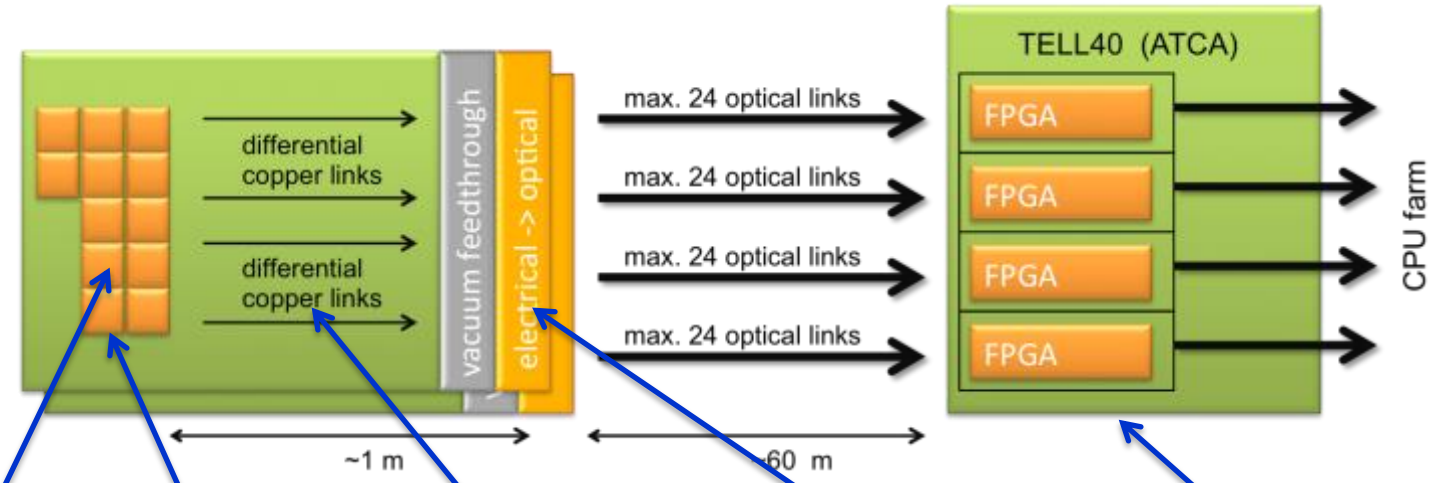
Should avoid material, especially at the tip of the module (where radiation damage is highest)

Novel solution: evaporate CO_2 via micro-channels etched in Si substrate

- High heat transfer coefficients
- no CTE difference (Si on Si)
- excellent uniformity of material in sensitive region
- Method developed with CERN PH-DT group
- Pressure tolerance of module very important



Electronics review topics



VeloPix ASIC

Front-end Hybrid circuit

Electrical high speed links

Optical & power board "OPB"

Tell40 data processing

+ power supplies

+ planning ressources

Some remarks

- Progress in the various areas is very different:
  - Design is quite well advanced for
    - 'VeloPix'
    - 'Electrical high speed links'.
  - At conceptual stage for
    - 'front-end hybrid',
    - 'Optical & power board'
    - 'Tell40 Data processing'
- Velopix ASIC is not 'fully' part of this review
  - Review only its interface with the rest of the system:
    - Data in/outputs, Fast & slow control, powering, …
  - Not 'Internally' : very complex ASIC and requires a separate review (early 2014 ?)
  - Nevertheless , an extensive presentation is provided for full understanding of the system.
- Documentation:
  - We benefit somewhat from the writing of the Technical Design Report…