VELO upgrade electronics – HYBRIDS

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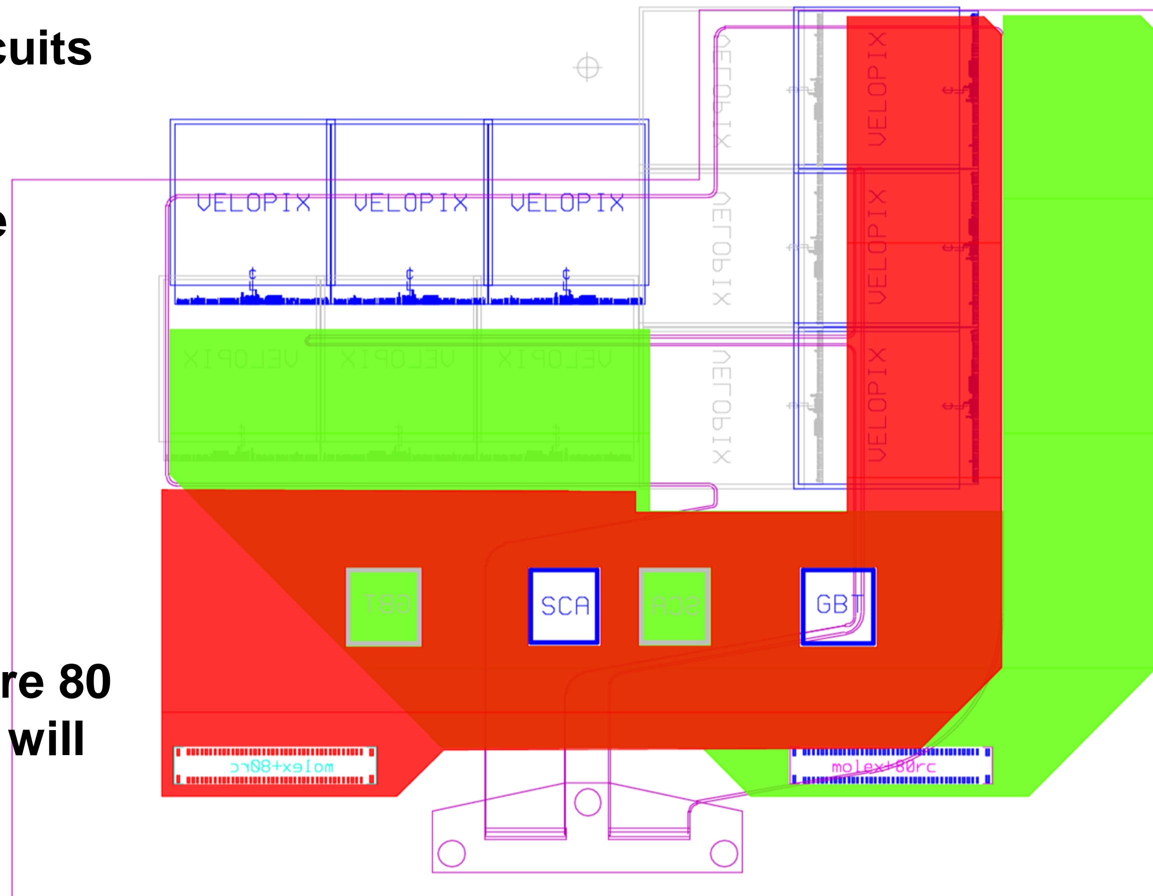
General layout

2 electrically identical circuits but
with different layouts attached either side of the cooling substrate

These circuit outlines are representative and will change when full design details are finalised.

Connectors shown here are 80 pin Molex – a final design will likely require 2 per side

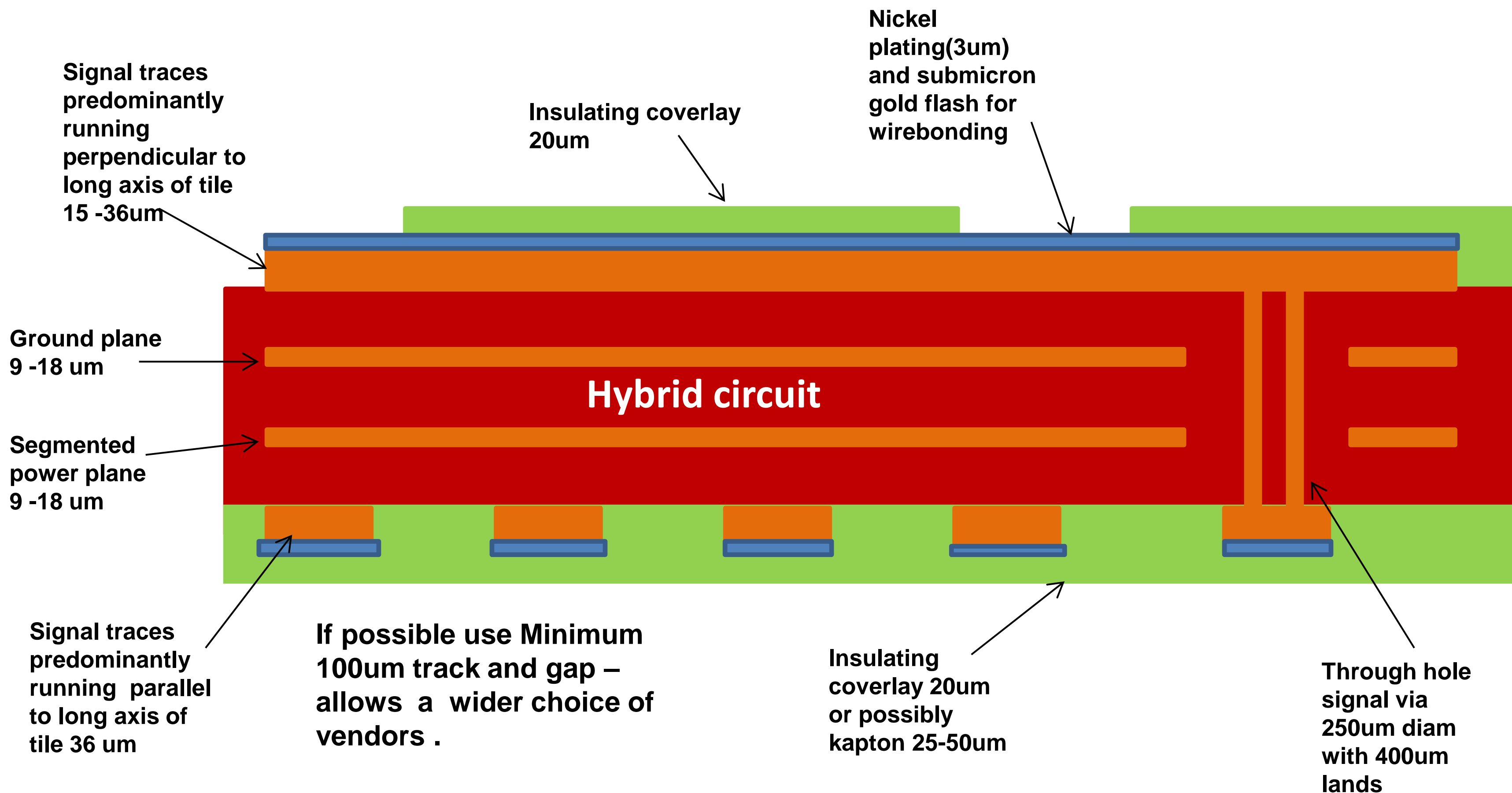


Velopix module proposed hybrid circuit footprints

Top side circuit

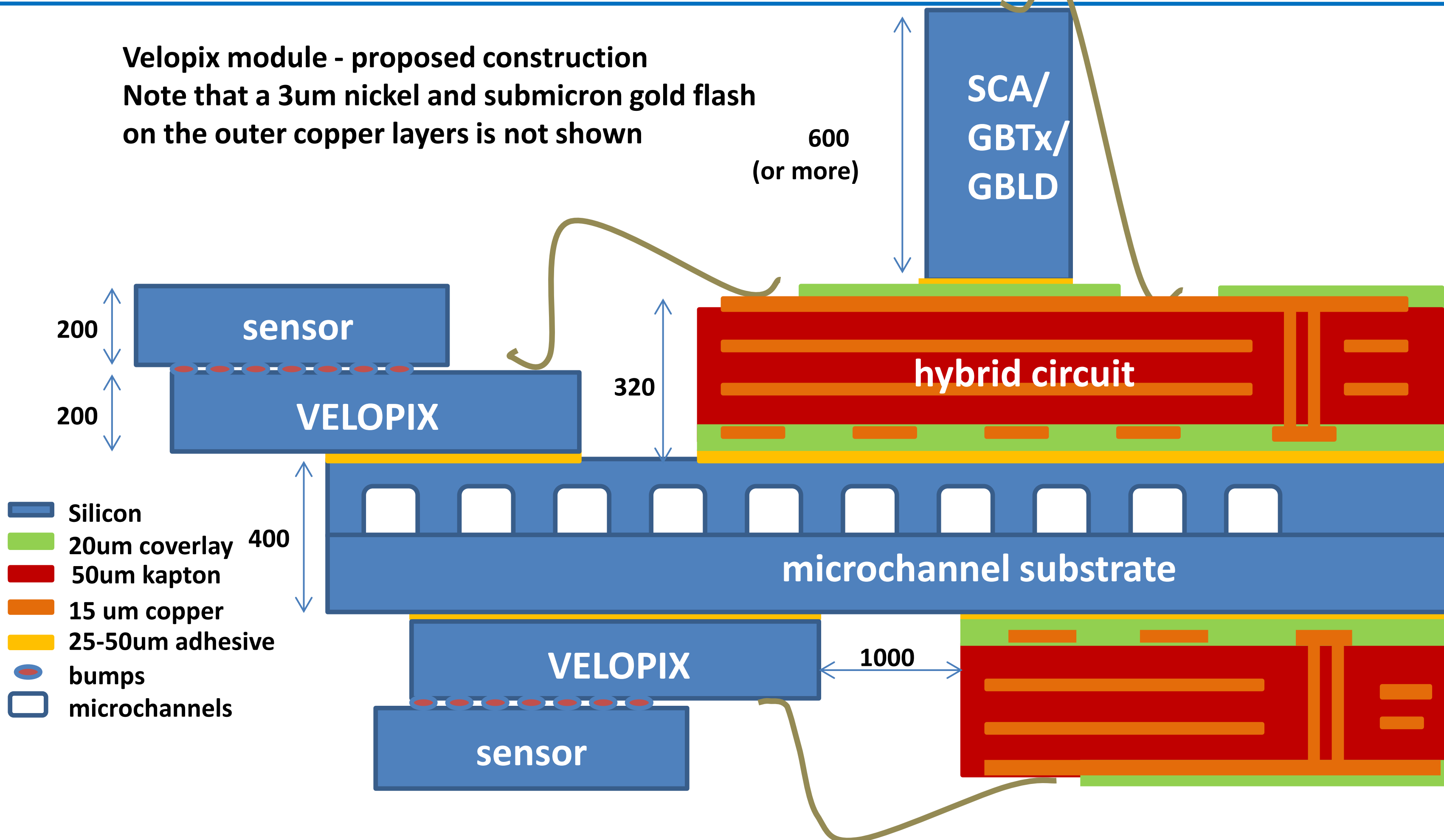
Bottom side circuit

Construction



Baseline hybrid - This has 4 copper layers but additional signal layers may be needed depending on final complexity and chip padring layout. This would add little copper as the traces would be narrow and sparse.

Module assembly



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Power distribution and decoupling

The ground plane will be continuous except where pierced by vias and common to all power supplies on the hybrid. This will be the second layer down in the pcb directly under the high speed traces on the top layer.

The power planes will be partitioned into analog and digital supplies to each tile. Multiple connector pins will be used for each supply and return.

It has been assumed for radiation length calculations that the power and ground planes would have an equivalent thickness of 15um of copper on each layer to account for less than complete coverage. It is possible that either or both these planes can be reduced to 9um copper in a final design.

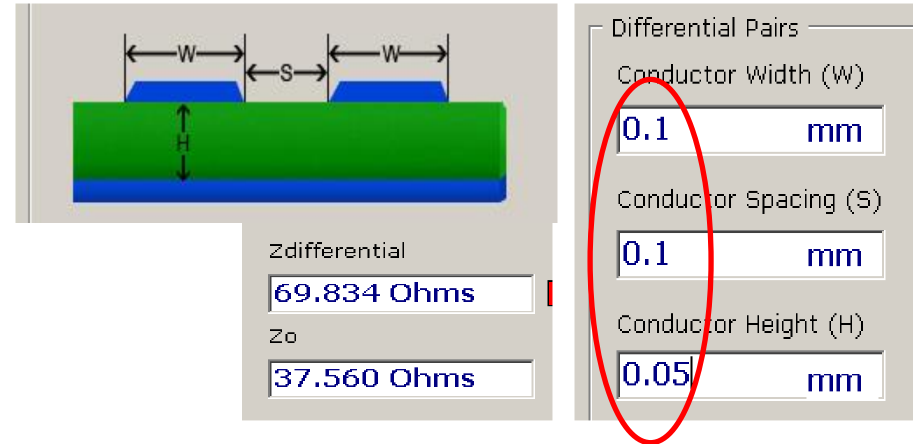
Low ESR ceramic decoupling capacitors will be placed as close as possible to each of the chips as necessary. Note that larger value capacitors could be placed on the cables. Some experimentation may be required here.

High frequency differential pairs

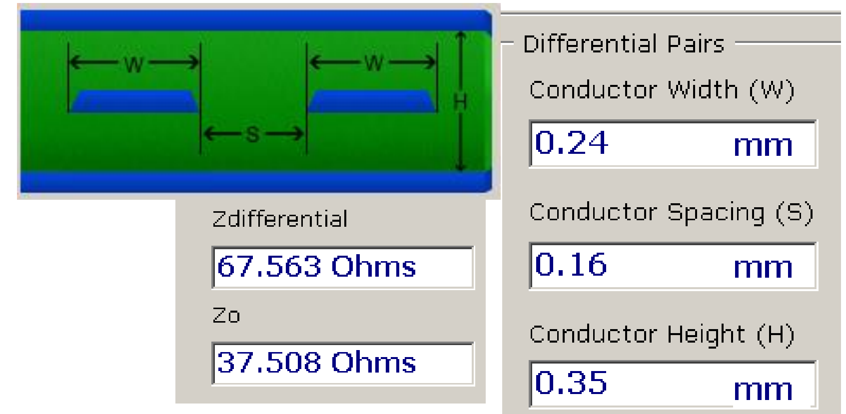
Hybrid traces carrying high frequency GHz signals need to match the characteristic impedance of the cable traces, direction changes should be minimised and vias avoided if possible .

This is achieved by keeping the 100um T&G traces on the top layer of the circuit and plating up to a thickness of 36 microns with a 50um kapton dielectric (Er=3.4) over a continuous ground plane.

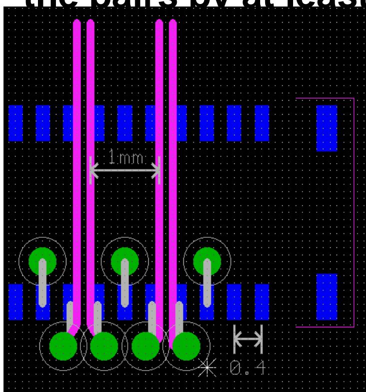
Crosstalk will be minimised by spacing the pairs by at least 300um.



Hybrid traces surface – 36um



Cable traces embedded -18um



Trial layout of 100um T&G pairs connecting from a lower layer to a Molex connector

In some instances it may be necessary to route high frequency traces for a short distance on the lower layer.

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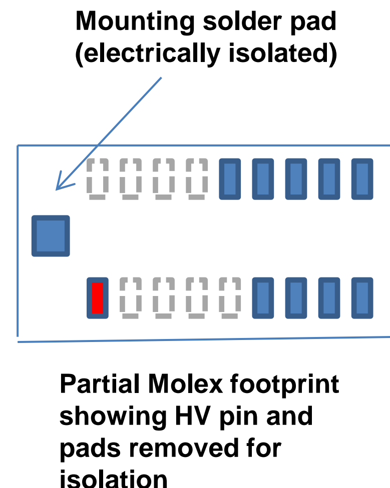
High voltage considerations

Separate high voltage bias up to 1KVwill be supplied to each sensor tile via a suitably rated one or two stage RC filter.

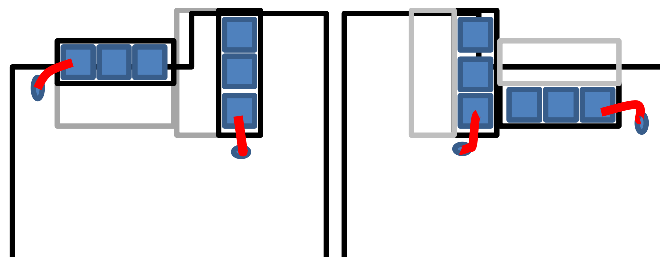
Isolation to avoid tracking at the connector will be achieved by removal of Molex connector pins and solder pads to give a minimum distance equal to that between the two end pins of the 1Kv rated RC filter capacitors.

Traces will be isolated by the same or greater distance from other traces where exposed and a minimum of 1mm when covered by the top coverlay.

To connect to the backplane of the detector a long wirebond will be made from the hybrid. Fortunately the positioning of the sensors allows this bond to be made at the short edge of the tile in all cases so it will not need to pass over any of the velopix bonds.



Partial Molex footprint showing HV pin and pads removed for isolation



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Component attach and test

BARE CIRCUIT TEST

It is normally the case that manufacturers can bare board test their PCBs but flying probe machines do not generally have the precision to probe 100um bond pad fingers. For VELO open and short tests were only made between accessible component pads and of over 200 circuits only one open and one short circuit were found after this limited test.

→ suggest use the same strategy

ATTACH DISCRETE COMPONENTS

Discrete components will be reflow soldered to the hybrids before the hybrids are attached to the module. Tin/lead solder will be used to avoid tin whisker problems and will be applied using a stencil.

To facilitate handling and to keep the circuits planar they will be manufactured on an FR4 carrier PCB and cut from this after solder reflow.

ATTACH AND BOND SUPPORT CHIPS?

In principle at this stage it would be possible to now mount the GBTx ,SCA and GBLD asics and wirebond them and, with suitable design of the carrier PCB, to then test the assembly before attachment to the substrate. ** The benefit would be to guarantee functioning hybrids and modules before attaching expensive chip and sensor tile assemblies. The caveat is that this makes the hybrid more fragile and difficult to handle.

(N.B. This is a proven technique developed by the Atlas group at Liverpool.)**

ATTACH HYBRIDS TO SUBSTRATE

ATTACH AND BOND SUPPORT CHIPS NOW?

TEST BEFORE MOUNTING SENSOR AND CHIP TILES?

is this test as good as what could have been made if support chips mounted on hybrid before attach to substrate

Conclusion

Ready to start design when chip padrings are finalised