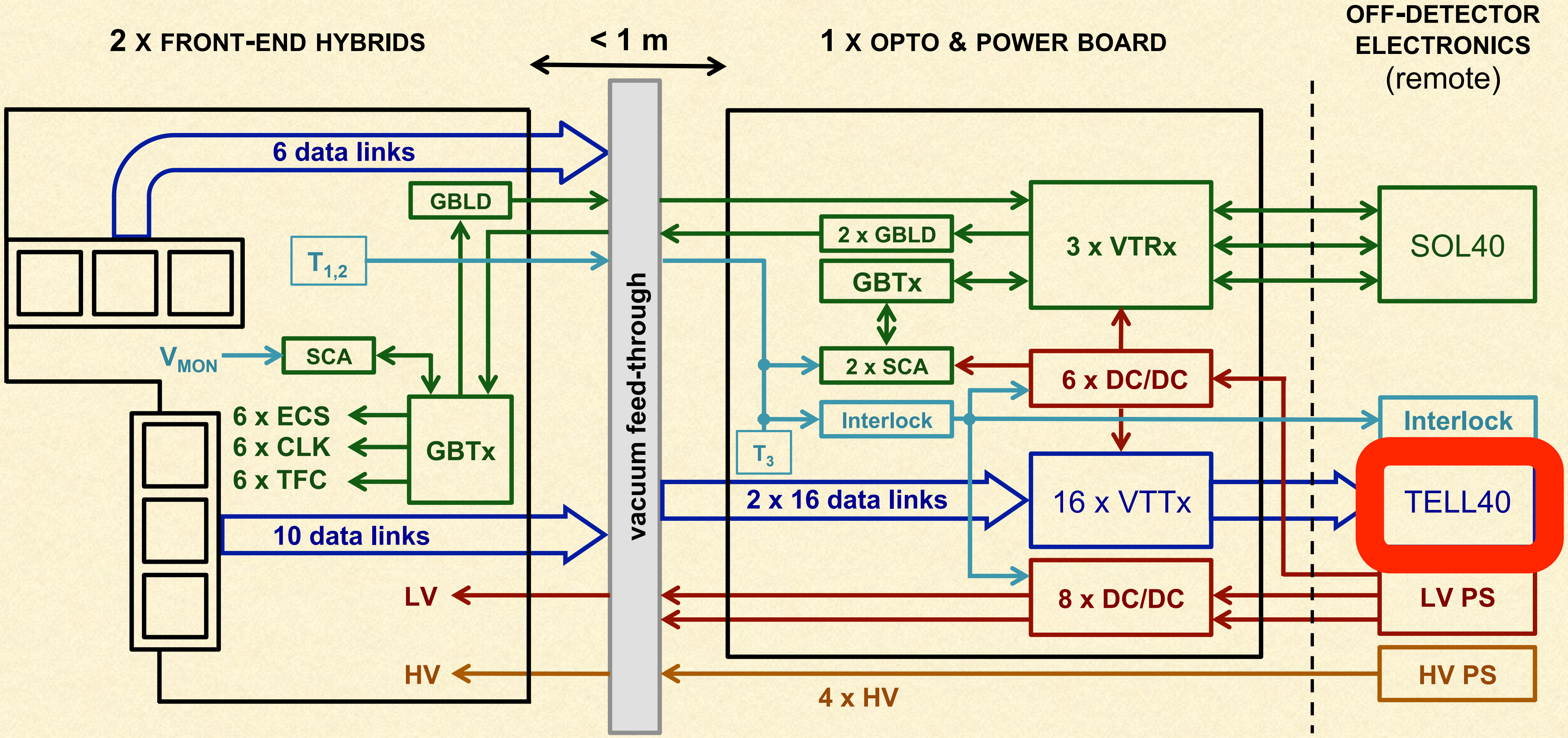
VELO UPGRADE DAQ

Karol Hennessy, Jan Buytaert

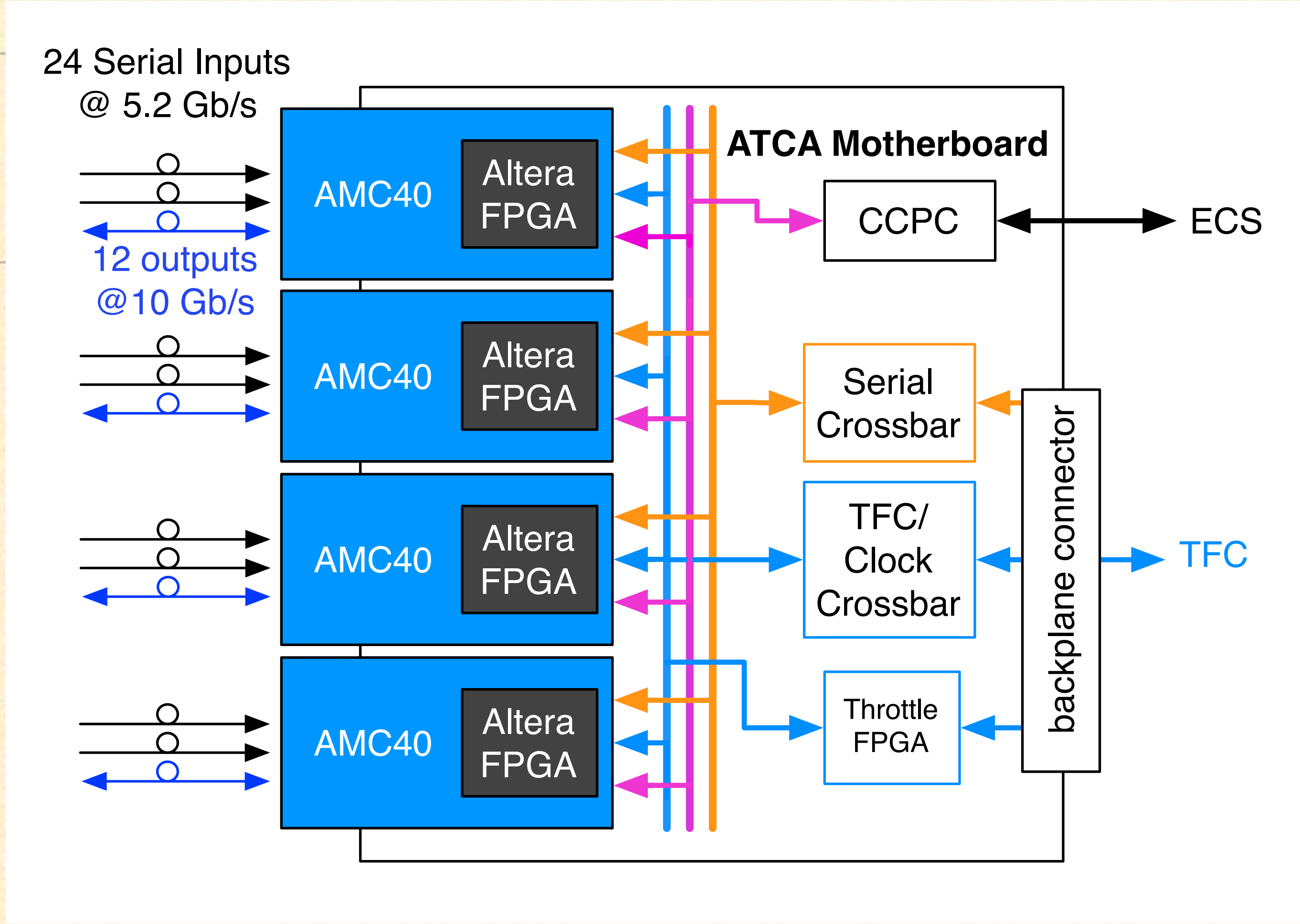
DAQ


2 X FRONT-END HYBRIDS
< 1 m
1 X OPTO & POWER BOARD
OFF-DETECTOR
ELECTRONICS
(remote)
6 data links
GBLD
T1,2
VMON
SCA
6 x ECS
6 x CLK
6 x TFC
GBTx
10 data links
LV
HV
vacuum feed-through
2 x GBLD
GBTx
2 x SCA
Interlock
T3
2 x 16 data links
3 x VTRx
6 x DC/DC
16 x VTTx
8 x DC/DC
4 x HV
SOL40
Interlock
TELL40
LV PS
HV PS

“TELL40”

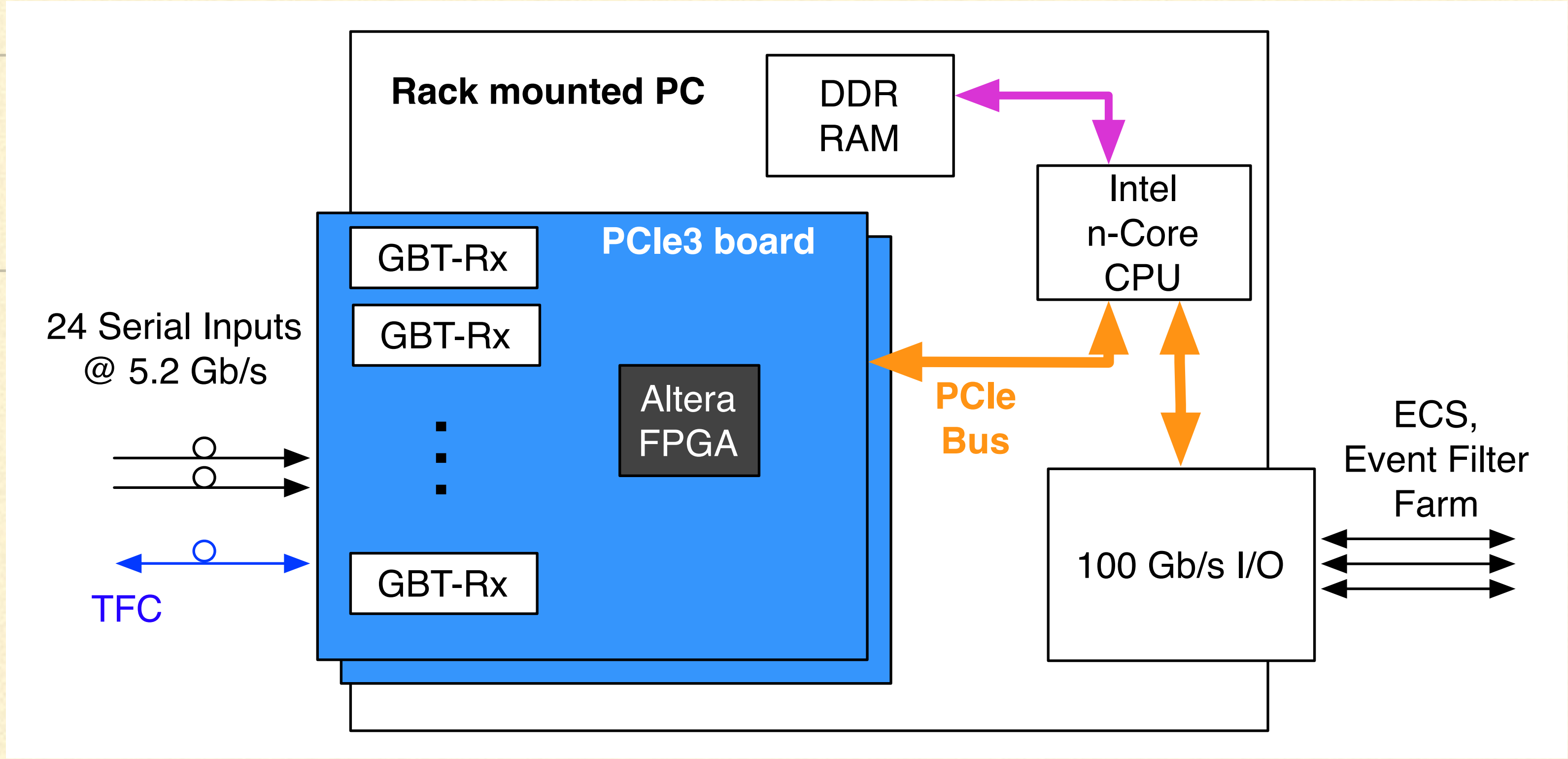
- TELL40 is used as an umbrella term for the LHCb upgrade DAQ Readout Board.
- Two options:
  - AMC40 (Traditional - rack with dedicated cards)
  - PCIe40 (New - PC based)
  - Similar to end user/programmer - FPGA based

AMC40



- Similar in form-factor to current TELL1 with CCPC
- Based on ATCA standard - dedicated crate with 14 slots
- AMC40 FPGA does most of the work.
  - Up to 24 GBT inputs on each AMC40 card
  - 12 outputs to event builder farm @ 10Gbits/s each

PCIE40



- New design from LHCb Online group
- Place FPGAs on PCIe3 cards inside rack-mounted PCs
- No need for special motherboards/crates
- No need for CCPC
- PCIe3 bus rate ~120 Gb/s => 100 Gb/s links

TELL40 FIRMWARE

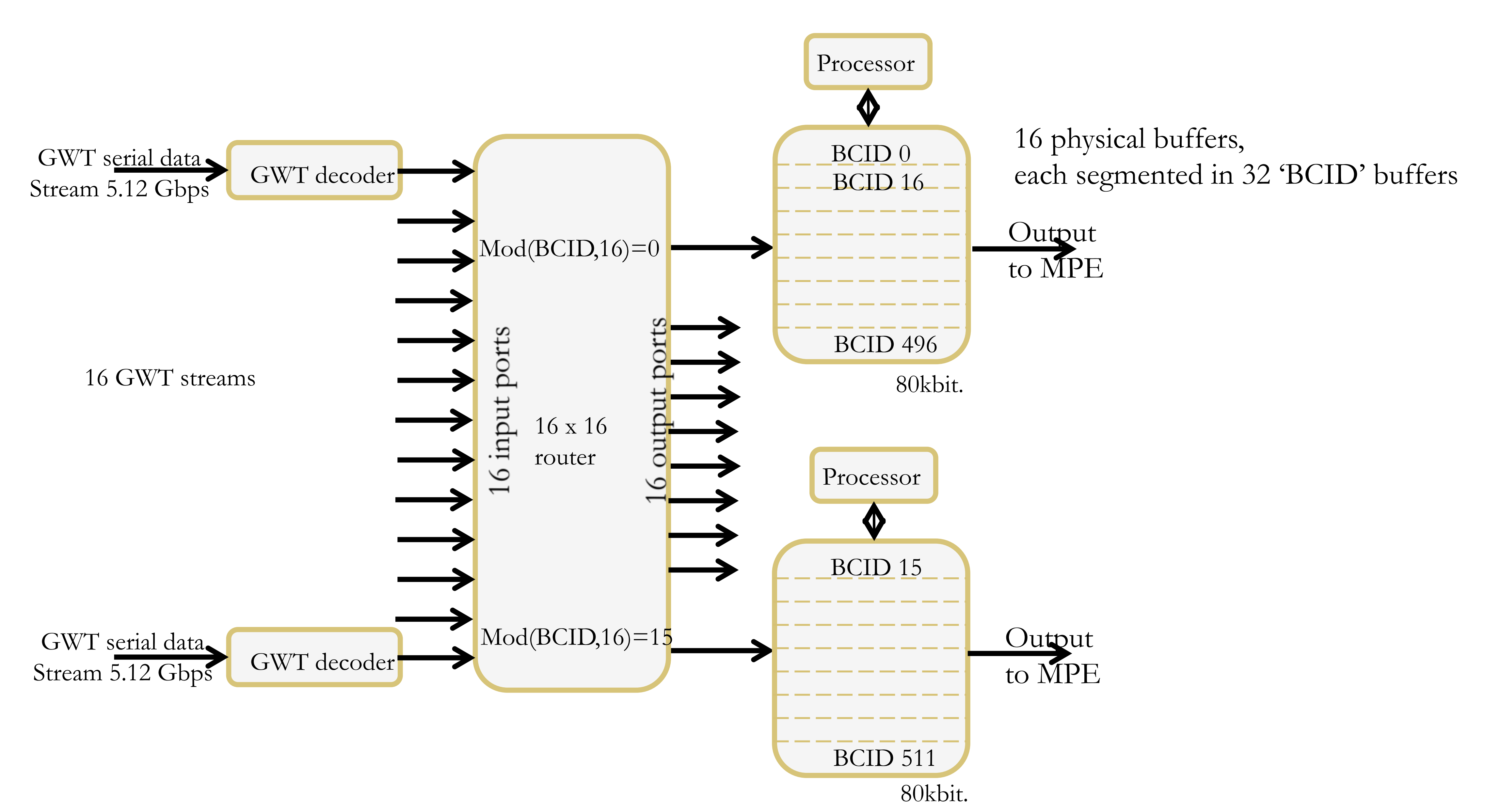
- Firmware will be much the same in either case since FPGA will be identical/very similar
  - Development done now is not wasted!
- Common firmware elements such as GBT decoding and packing data for the farm will be developed centrally
  - LLI - Low Level Interface
- VELO specific parts must be developed by the group.

VELO FIRMWARE

- Main challenge - time ordering data whilst coping with high input rate from hottest chips.
  - If possible, perform clustering
- Two critical items to ascertain the firmware resource utilisation
  - GWT decoding - similar to GBT decoding?
  - Time Re-alignment
- Can independently develop VELO elements

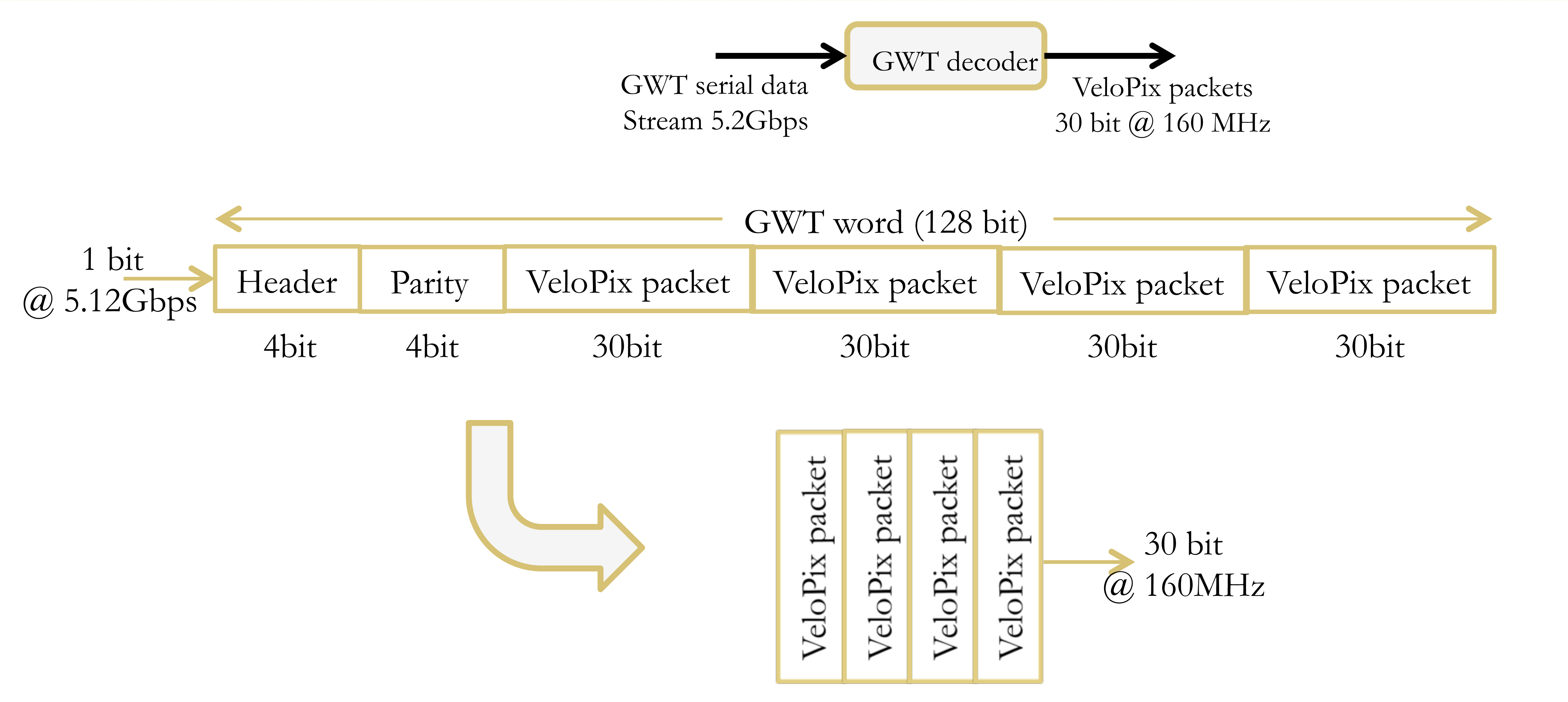
TIME REORDERING

- Based on a packet router. All VeloPix packets with the same BCID are collected in one BCID buffer. The routing destination is based on 9 bit BCID contained in the packet.



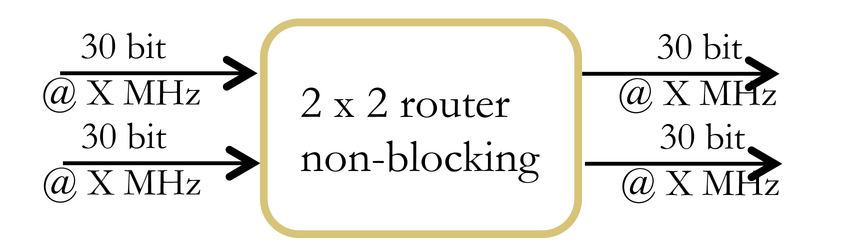
GWT DECODER

- Extract fixed length (30 bit) and fixed position VeloPix packets from 128 bit GWT words

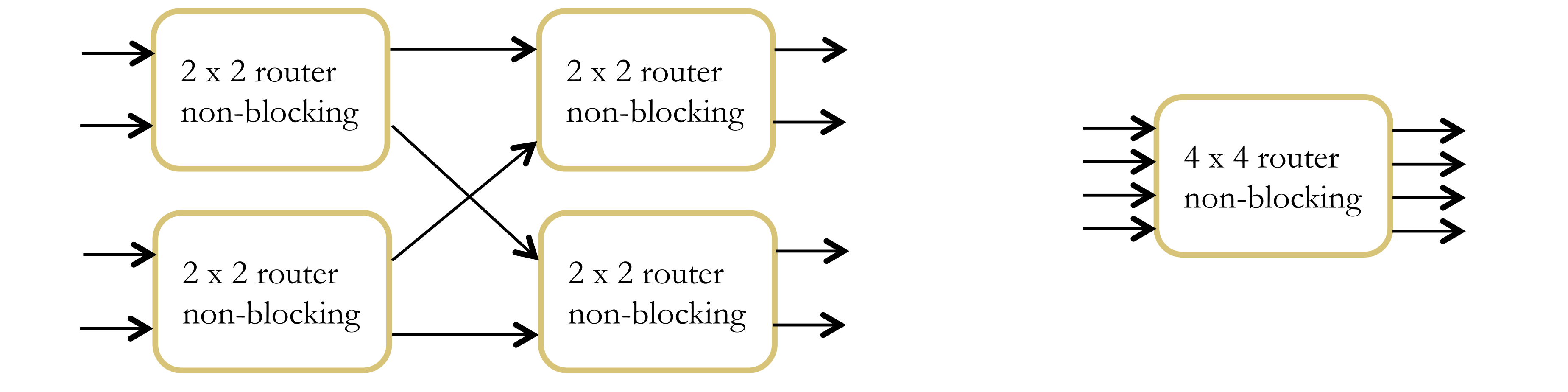


ROUTER CORE

- 'Building block': 2 x 2 non-blocking router. Routing based on MSB of BCID.

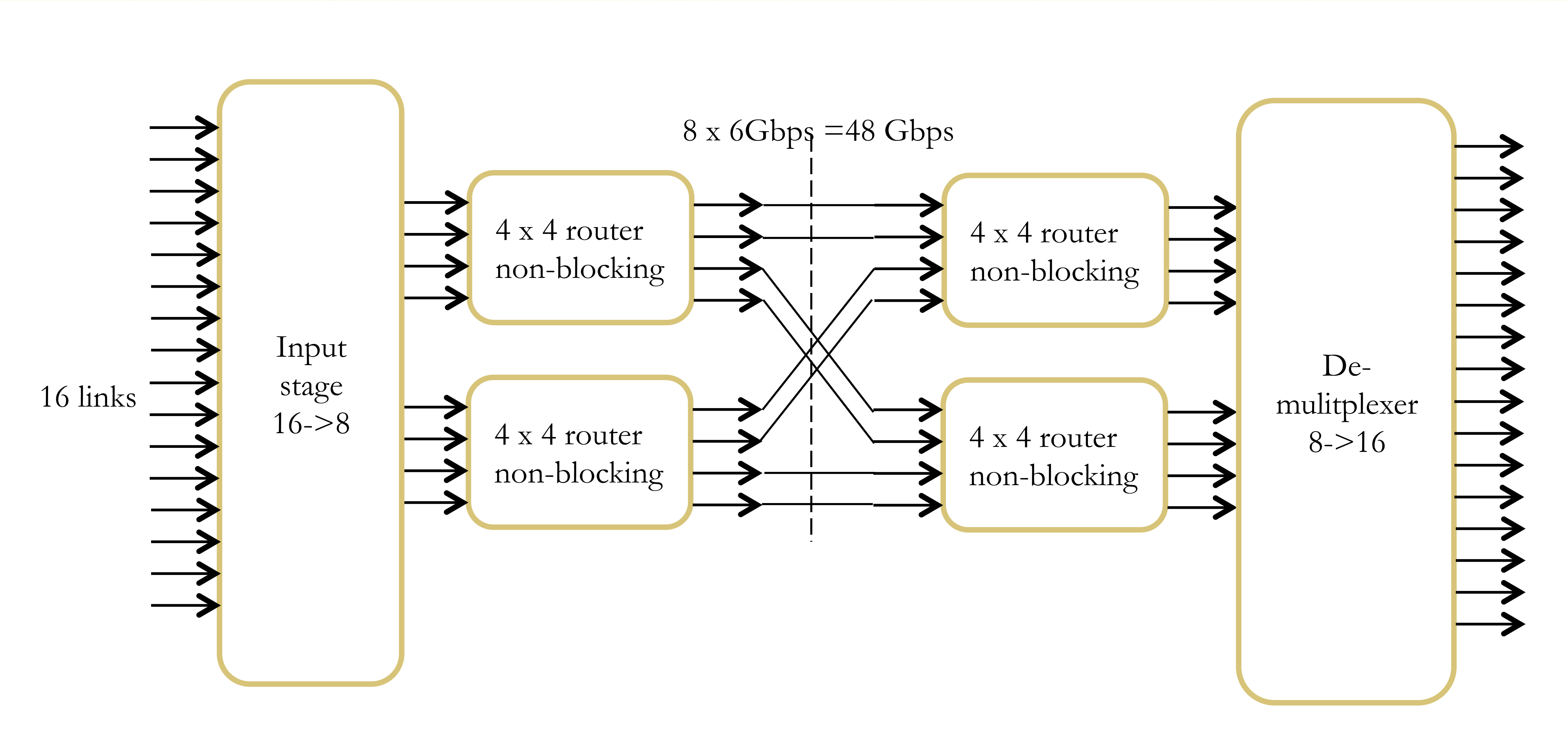


- Need the highest possible clock speed !
  - X = 200MHz? => 6 Gbps port data rate
- Cascade to 4 x 4 non-blocking.



FULL ROUTER

- 8x8 ? Cross sectional bandwidth = 48 Gbps.


16 links
Input stage 16->8
4 x 4 router non-blocking
4 x 4 router non-blocking
8 x 6Gbps =48 Gbps
4 x 4 router non-blocking
4 x 4 router non-blocking
De-mulitplexer 8->16

ROUTER INPUT STAGE

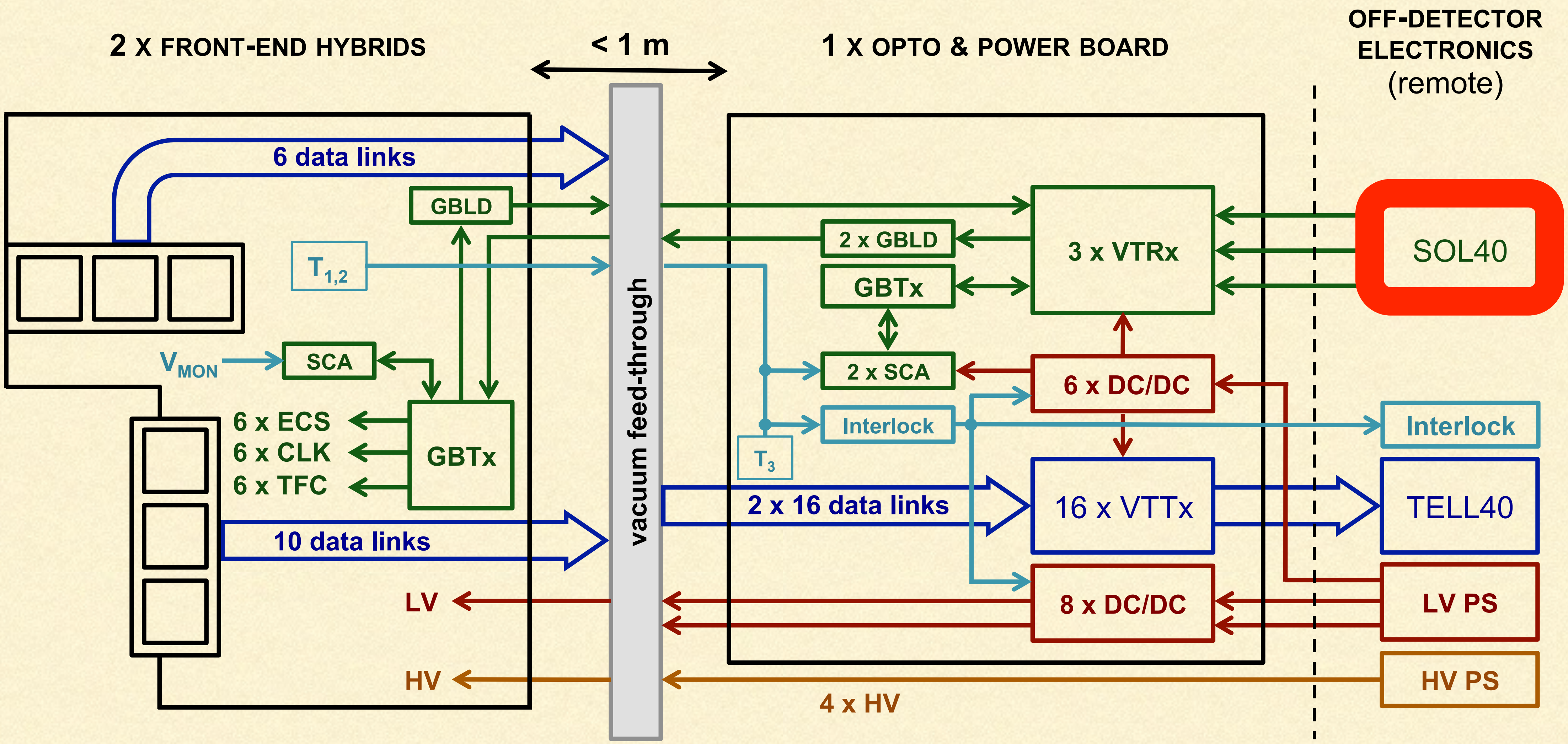
- Not all 16 input links use 100% of the available link data rate (4.8Gbps):

- Estimates : 4 x 4.8 Gbps, 6 x 2.3Gbps, 4 x 1.8 Gbps, 2 x 1.1 Gbps. Total= 42.4 Gbps.

- Need to equalise the load at the 8 input ports of the router. Goal for data rate at one input port of the router is 6 Gbps (= fully loaded 30bit bus @200MHz). Available input rate capacity is 48 Gbps.

- Redistribute the packets on the input links to the 8 outputs.

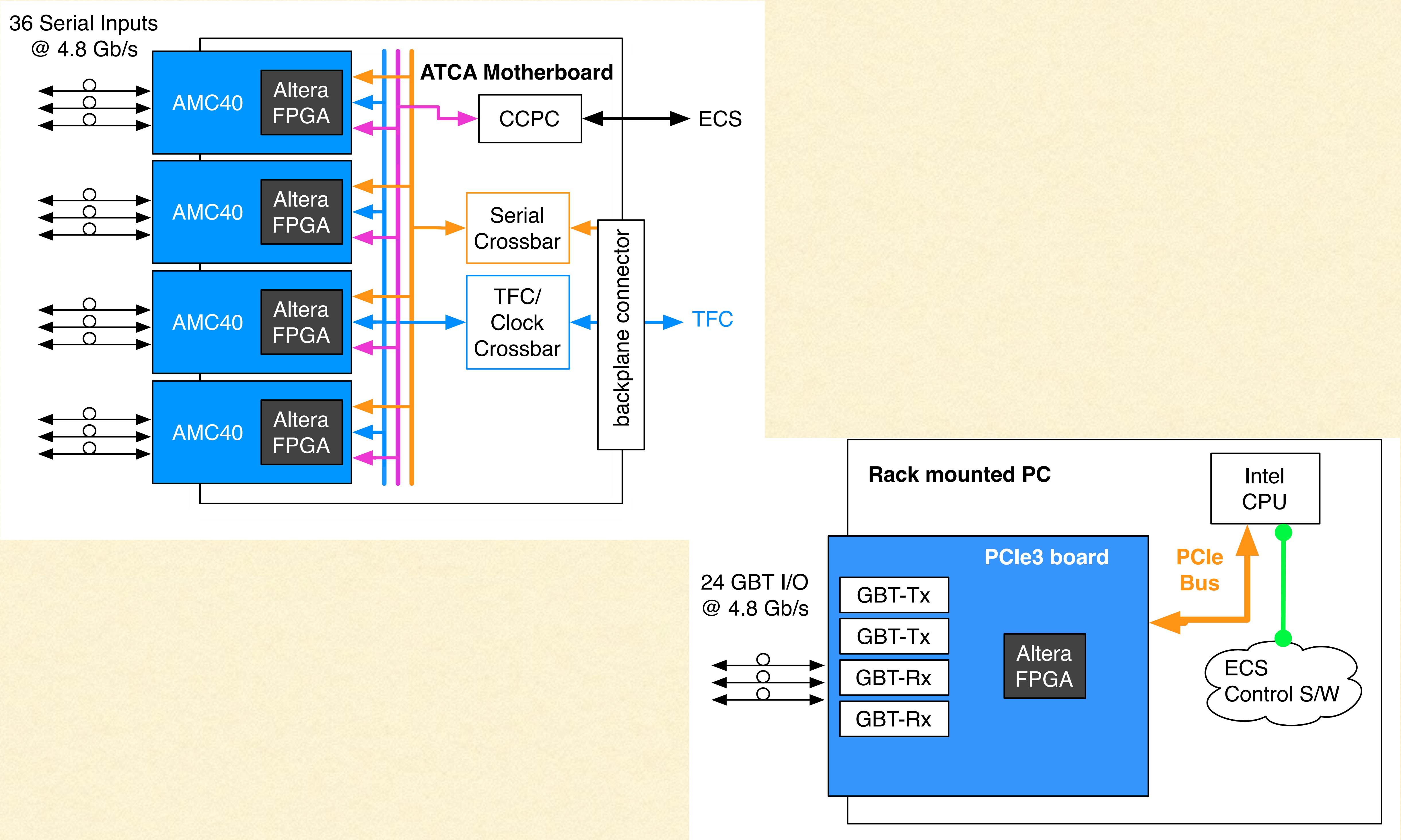
CONTROL/ECS


2 X FRONT-END HYBRIDS
< 1 m
1 X OPTO & POWER BOARD
OFF-DETECTOR ELECTRONICS
(remote)
6 data links
GBLD
T1,2
VMON
SCA
6 x ECS
6 x CLK
6 x TFC
GBTx
10 data links
LV
HV
vacuum feed-through
2 x GBLD
GBTx
2 x SCA
Interlock
T3
3 x VTRx
6 x DC/DC
16 x VTTx
2 x 16 data links
8 x DC/DC
4 x HV
SOL40
Interlock
TELL40
LV PS
HV PS

SOL40 - CONTROL & MONITORING

- Analogous to the TELL40
- Will have the same form-factor AMC40 or PCIe40, communicating over GBT
- No custom firmware!
  - Firmware will be general and developed by the Online group
  - Sub-detectors will add definitions for communications spec.
    - E.g., SPI, I2C, ELMB etc.

SOL40 - OPTIONS



FROM THE (UPCOMING) TDR

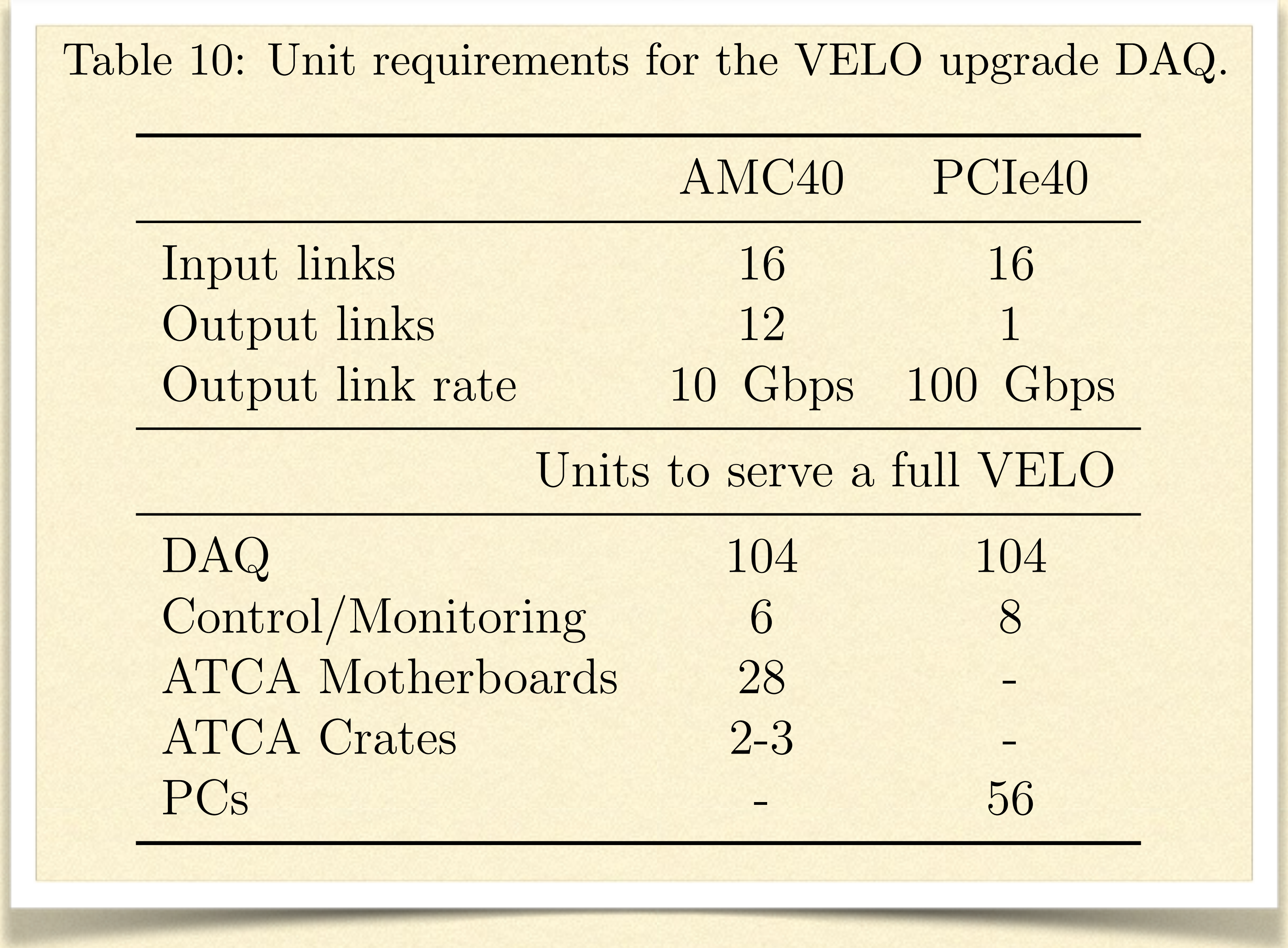


Table 10: Unit requirements for the VELO upgrade DAQ.

	AMC40	PCIe40
Input links	16	16
Output links	12	1
Output link rate	10 Gbps	100 Gbps
	Units to serve a full VELO	
DAQ	104	104
Control/Monitoring	6	8
ATCA Motherboards	28	-
ATCA Crates	2-3	-
PCs	-	56

- But these numbers make the assumption that we can support at least 16 links per FPGA

PROTOTYPING PLAN

- Stage 0
  - Can “do it all” in simulation before any final decisions are made.
  - Realisitically, prepare a first version of VELO-only firmware and examine resource utilisation
- Stage 1
  - First prototype board should run first version of firmware integrated with LLI
  - find bugs not found by simulation
  - Develop a front-end emulator that runs on a similar/same chip
- Stage 2
  - Approach a final version of firmware
  - Add SOL40 to system, create definitions and test.

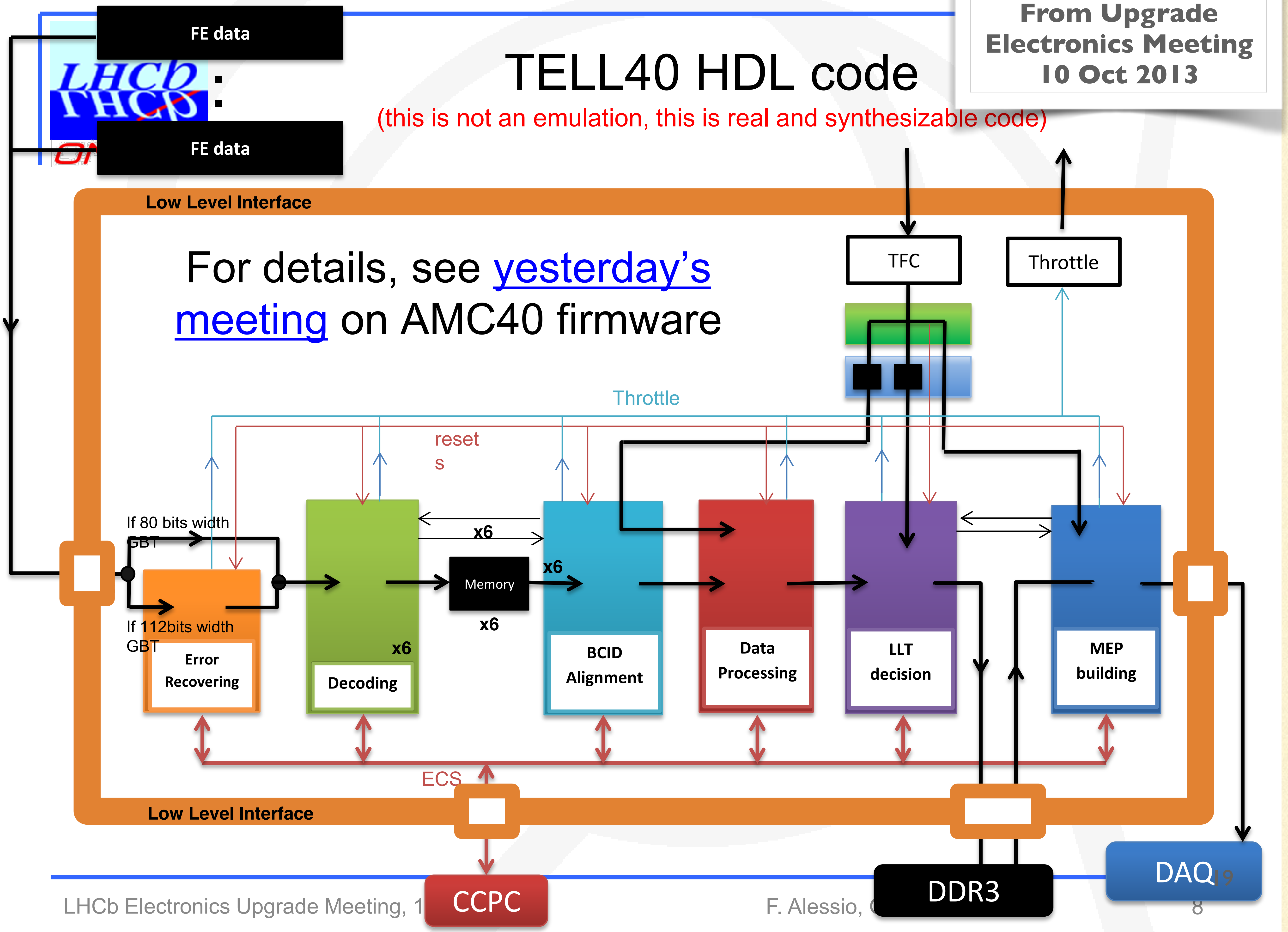
BACKUP

From Upgrade Electronics Meeting 10 Oct 2013

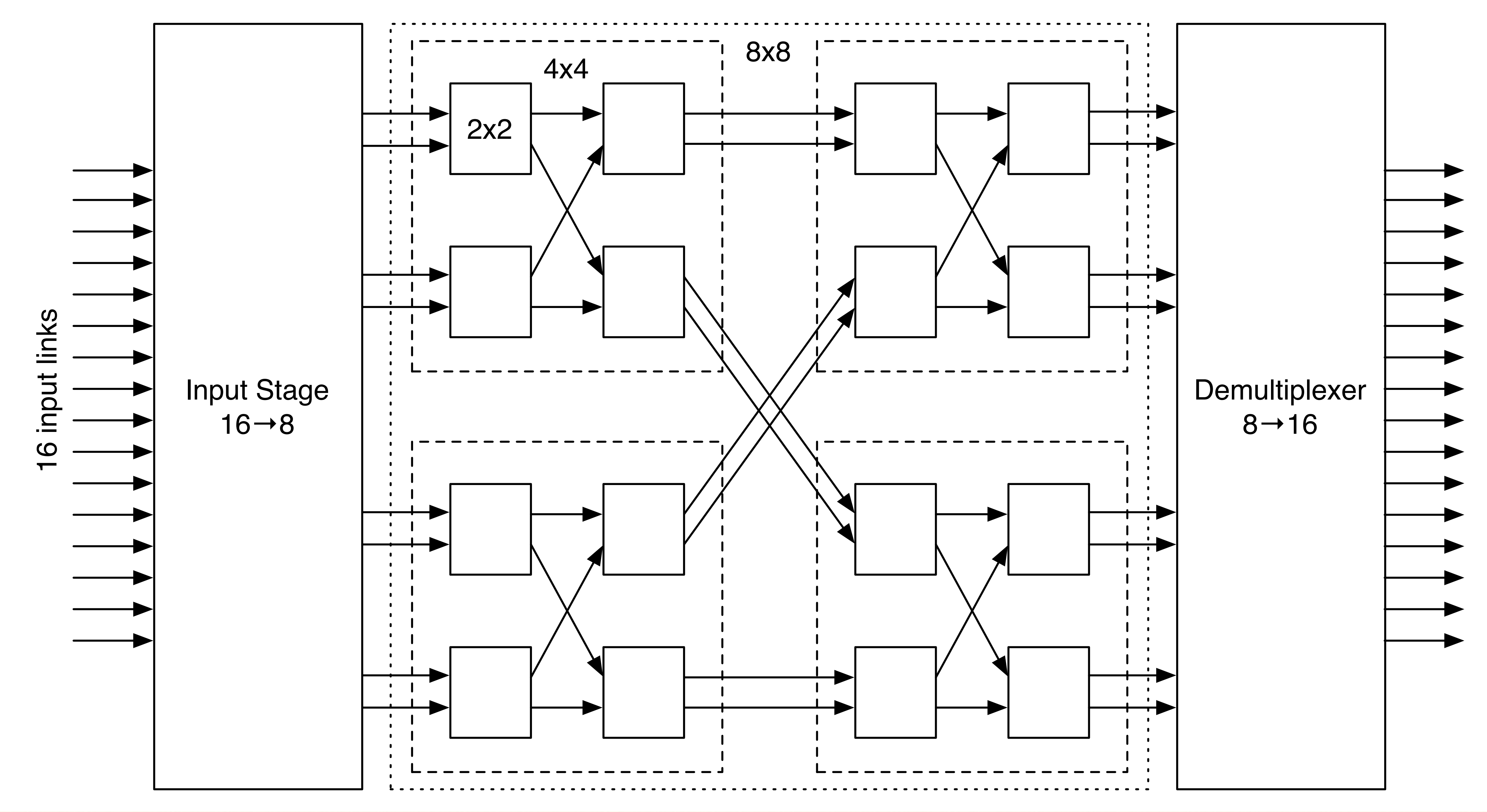
TELL40 HDL code

(this is not an emulation, this is real and synthesizable code)

For details, see yesterday's meeting on AMC40 firmware



16X16 ROUTER


16 input links
Input Stage
16→8
8x8
4x4
2x2
Demultiplexer
8→16