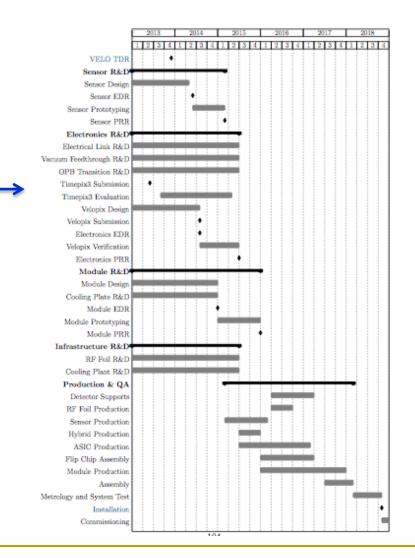
# VELO Upgrade Timeline

### VELO Upgrade schedule almost finalised for TDR

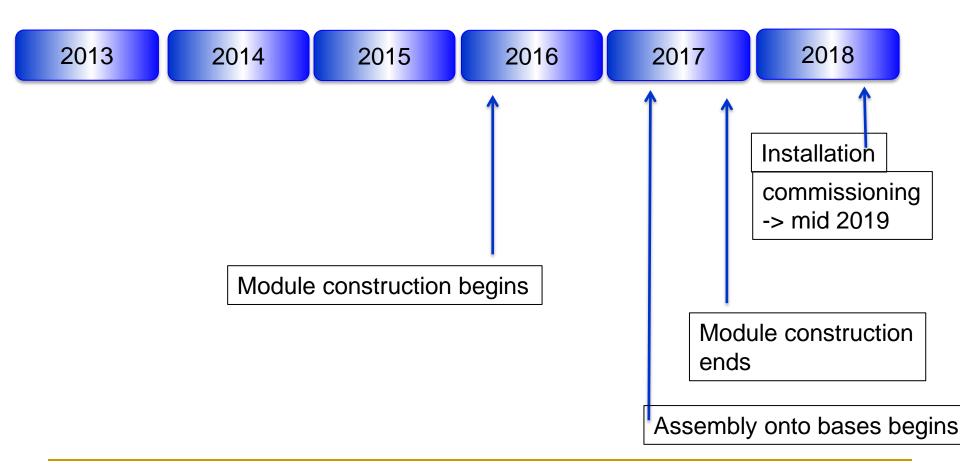
Today we discuss suggested timelines for the electronics part

Many thanks for input to Martin, Eddy, Jan, Lars, Karol, Tony +++

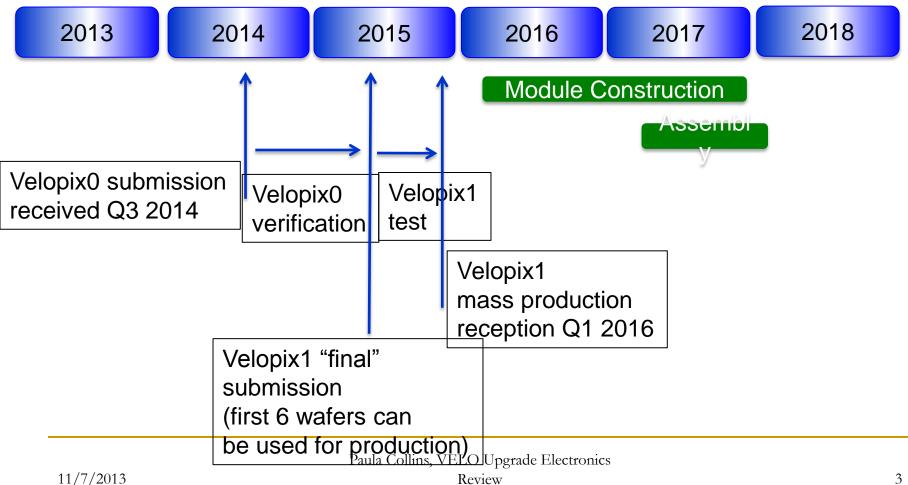


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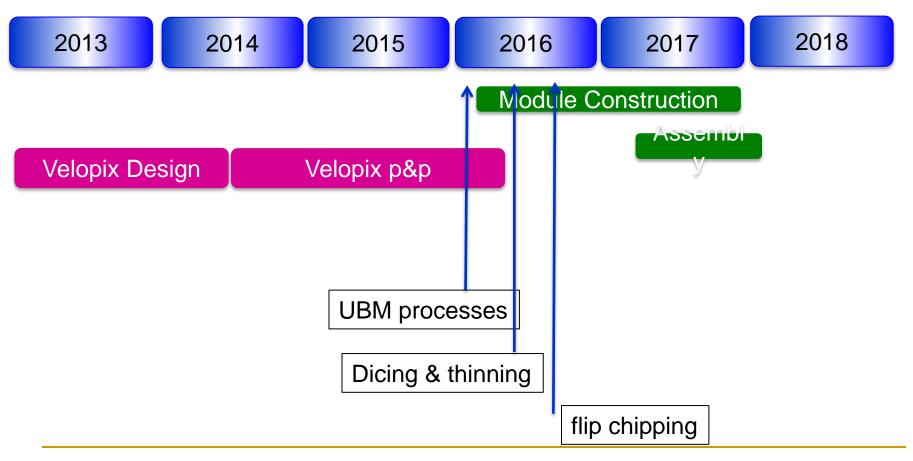
# Module Construction & Assembly



# Velopix Schedule

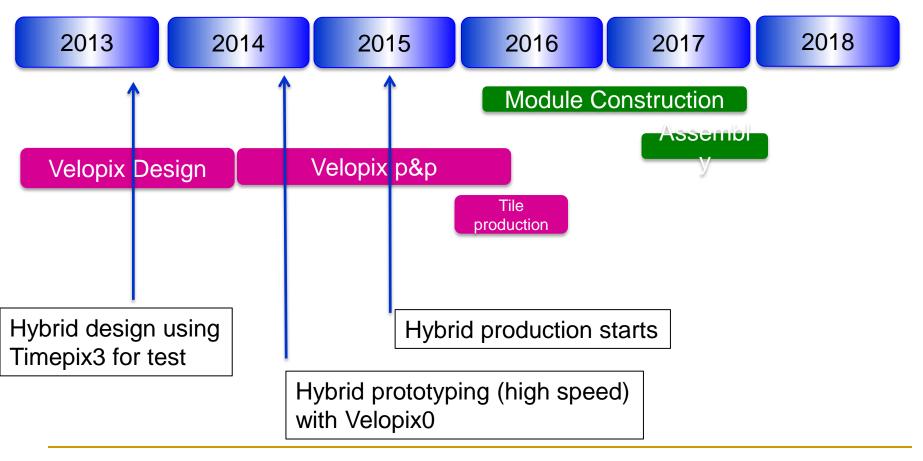


### Tile Production Schedule

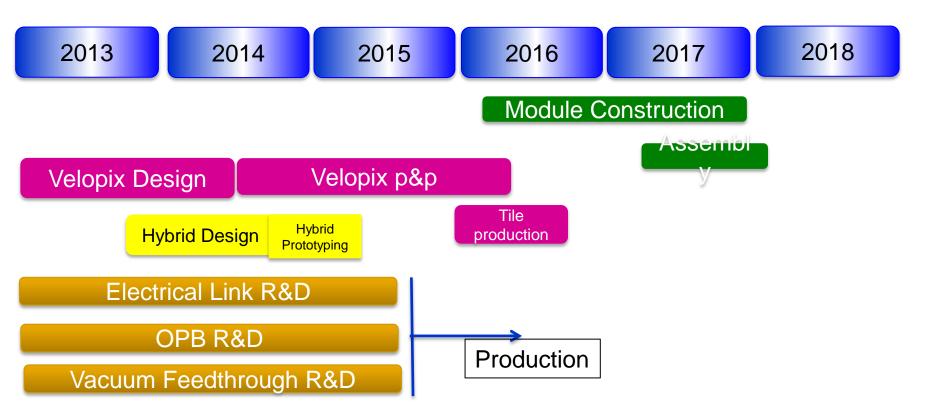


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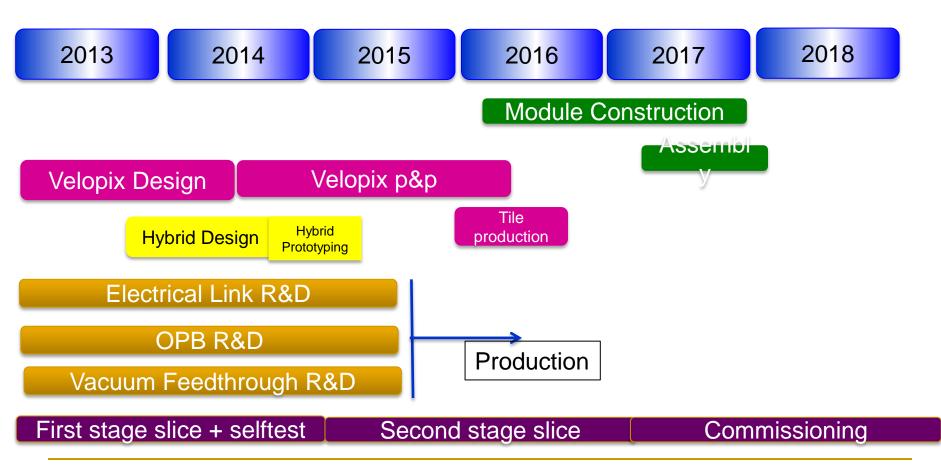
## Hybrid Schedule



# Link, OPB, Feedthroughs

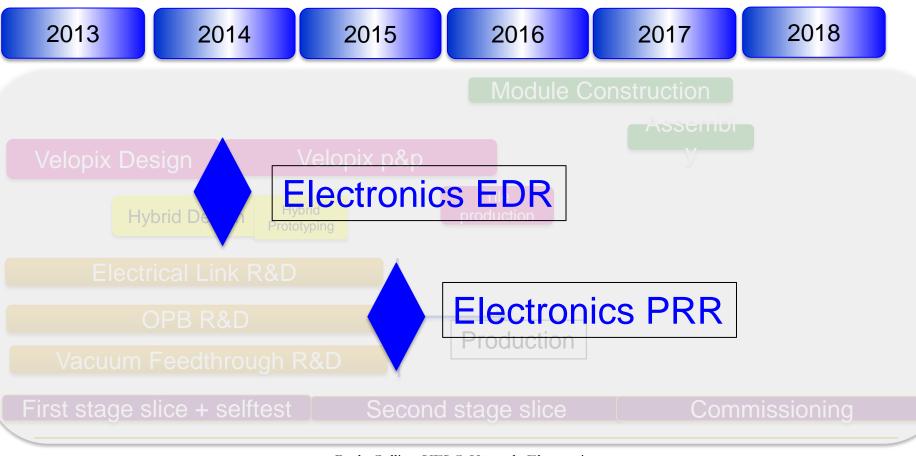


# Firmware and ECS Development



# Proposed Dates for EDR and PRR

p&p = production & prototyping



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### Resources

Production stage	Host Country
Electrical Link	UK, Spain
Vacuum Feedthrough	UK, Russia
ОРВ	UK
HV + LV	UK
General Electronics	UK, Brazil
Hybrid	UK, Spain
DAQ Integration + ECS	UK, Brazil
FE ASIC	The Netherlands, Switzerland
R&D, Design, Optimisation, QA, Testbeam	UK, The Netherlands, Spain, Brazil, China, Russia, Switzerland

Official production tables leave many tasks open. e.g. ASIC wafer testing, bench and testbeam activities, production database etc. may be led by an institute but contributions are possible