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Developments on 3D detectors at FBK-irst

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outline

- tecnological strategy

- first 3D - DDTC batch
  - Layout
  - Electrical characterization

- Next Steps (with in-house DRIE)

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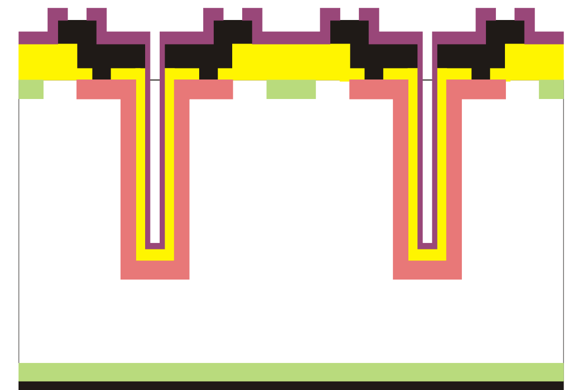
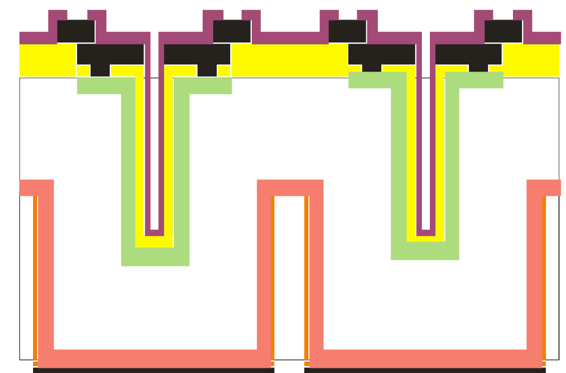
Introduction

FBK is developing the technology for the production of 3D detectors in a three phases program:

1. First device produced: **3D-S**ingle **T**ype **C**olumns
   "simple" fabrication process, high yield;
   collection mechanism not very efficient.

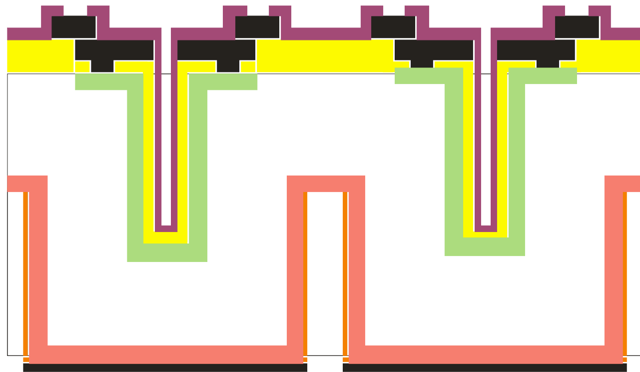


2. Performance enhancement with acceptable process complication:
   3D-Double **T**ype **C**olumns



3. Full 3D detectors.

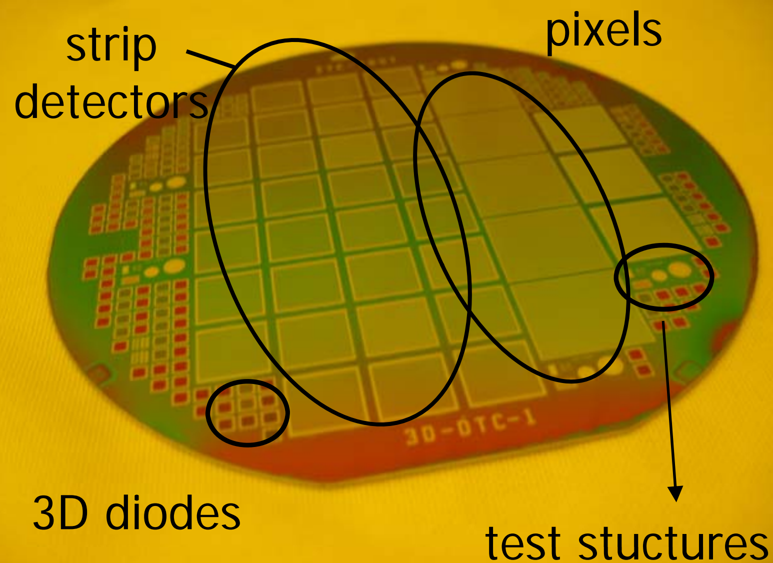
3D DDTC: process and wafer layout



Double sided process

P-type columns on n-type substrate

no hole filling



Planar test structures

3D diodes: single and double columns

30 strip detectors, cell size 1cmx1cm, biased by Punch–through structure with AC and DC pads

ALICE (5 detectors)
MEDIPIX (3 detectors) pixel

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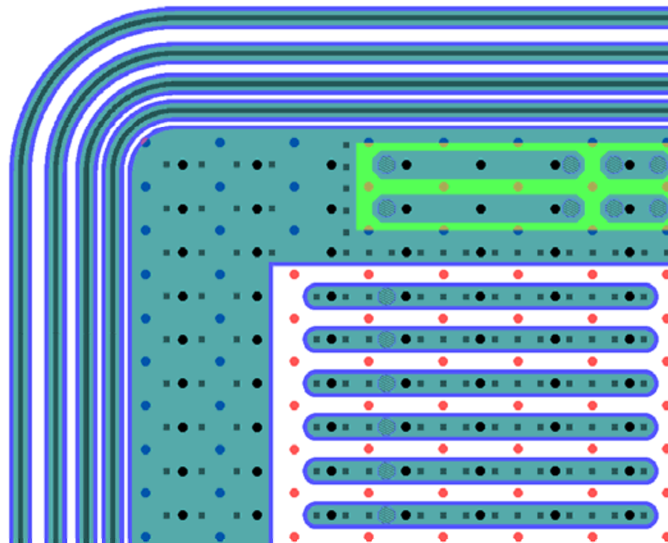
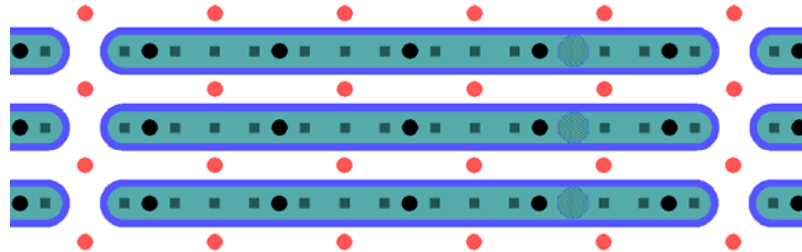
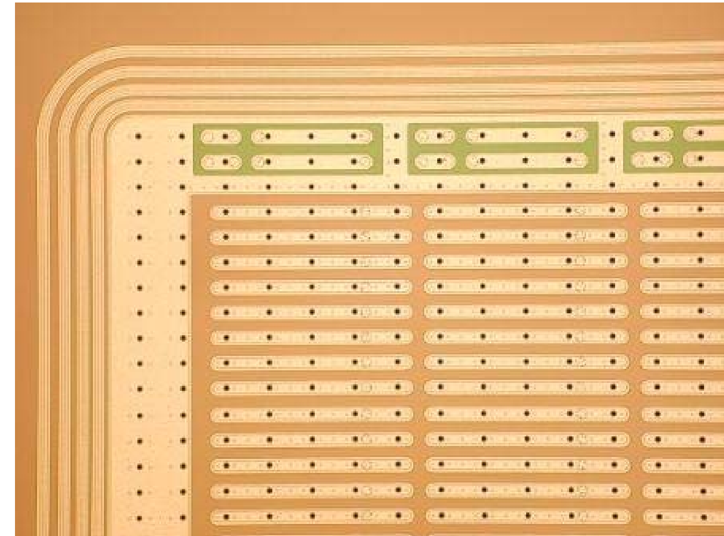
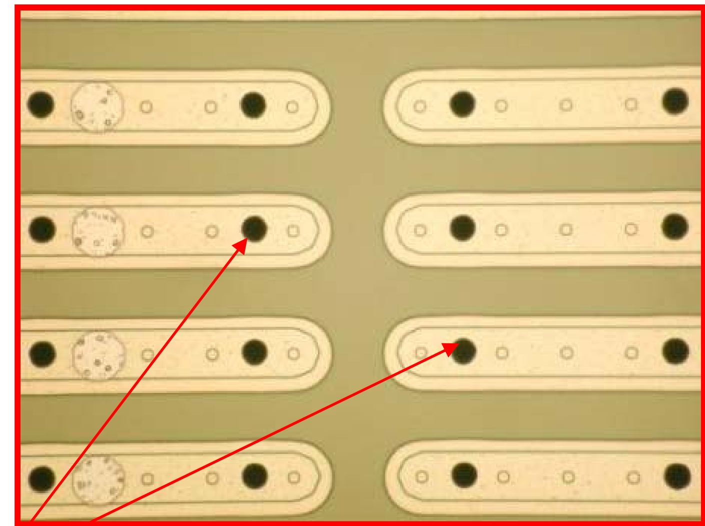
ALICE pixel detectors

5 devices/wafer
(3 with metal on backside)









p-type columns

Planar test structures

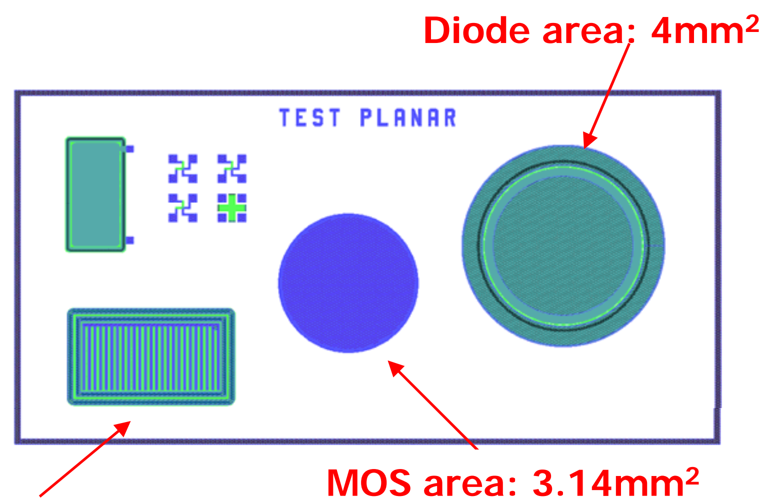
Very low depletion voltage (10V) for 300µm thickness

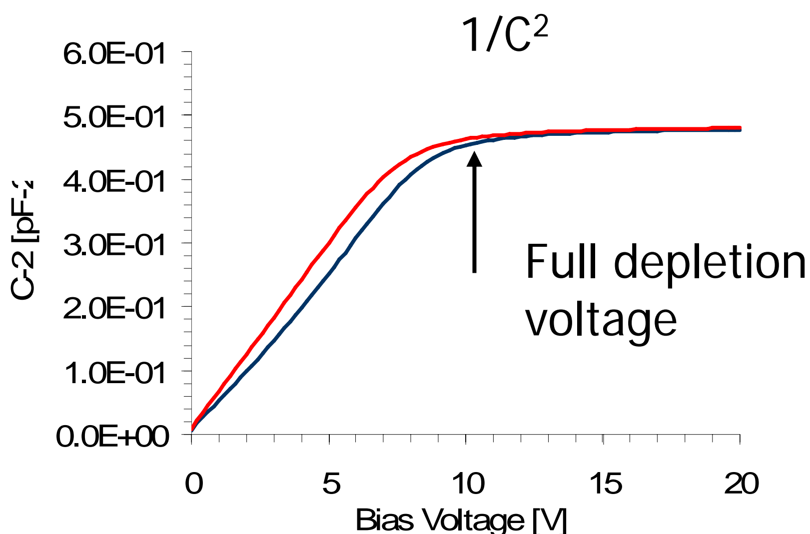
From $1/C^2$ a substrate concentration of 1.4×10^{11} cm^{-3}

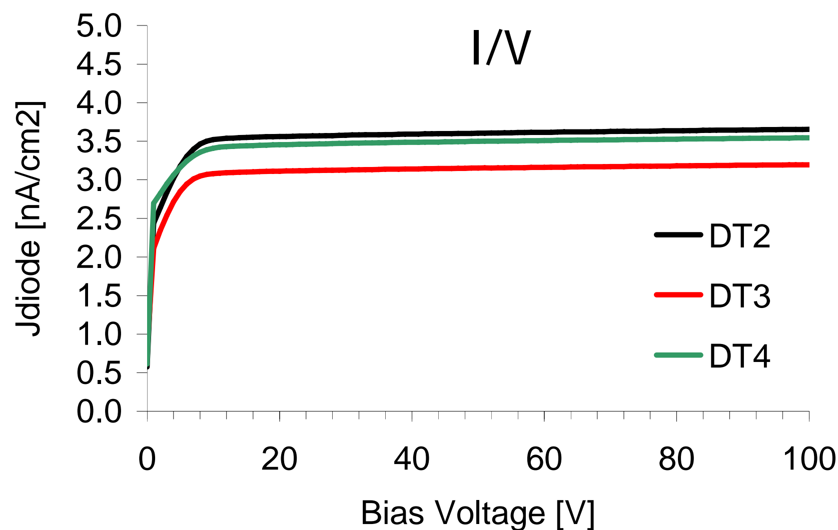
Very low leakage current→ good process

Tox = (570-600) nm
Qox = $(3.6 – 5)\times 10^{11}$ cm^{-2} from CV on MOS structures

So = 1 cm/s from gated diode measurements







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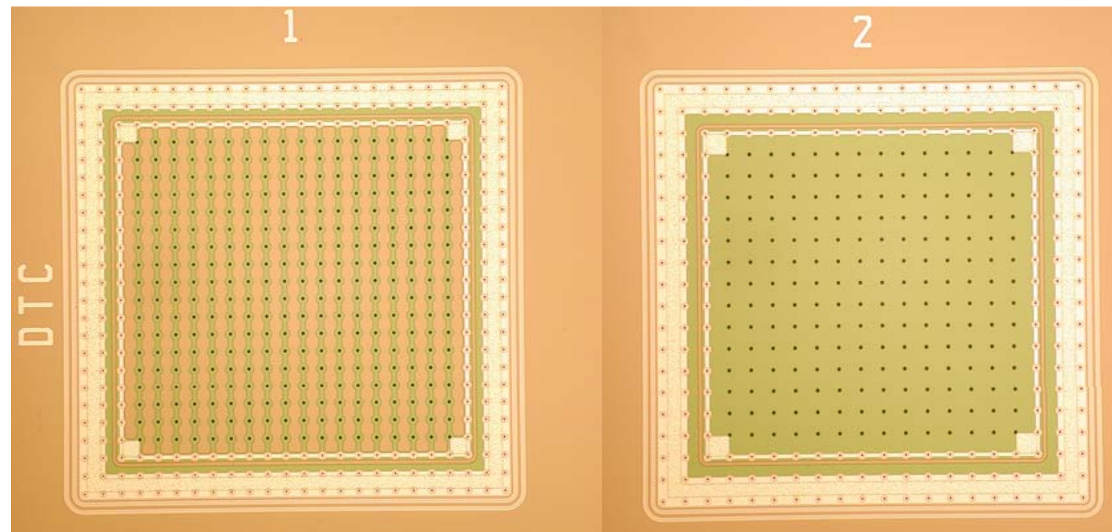
3D-stc & dtc diodes



48 STC & 48 DDTC diodes
Active area 16mm x 16mm

Either with a uniform (2) or strip like (1) surface implant.

Pitch80 have 20 x 20 = 400 columns

Pitch100 have 16 x16 = 256 columns

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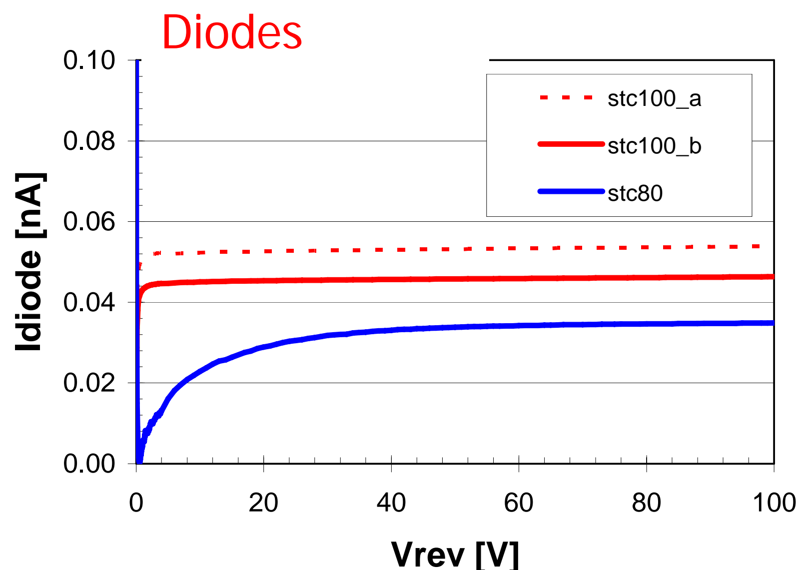
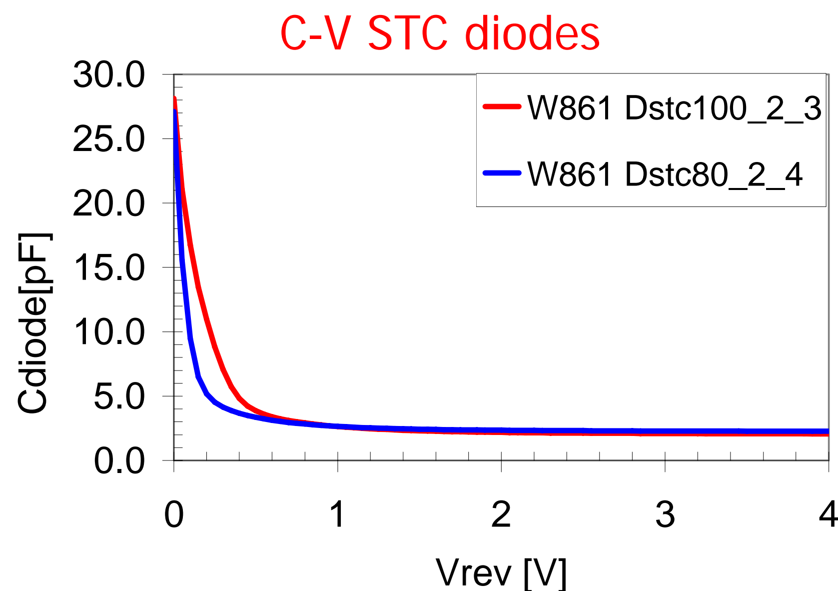
3D-stc diodes

STC diodes exhibit low dark current in agreement with previous batches
Less than 0.1pA/col

Lateral depletion < 0.5V , full depletion < 3V

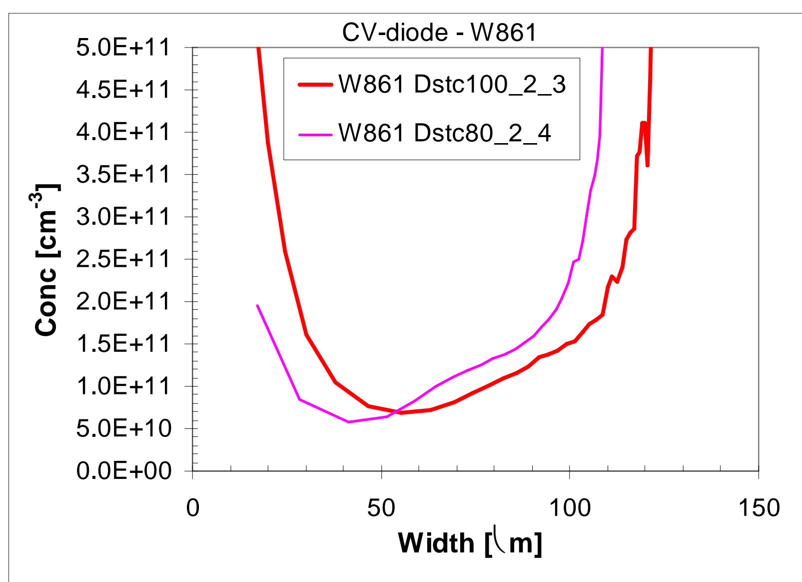
STC diodes, both 100um and 80 um pitch have the same capacitance value at full depletion (does not depend on pitch)





Diodi 3D stc – CV

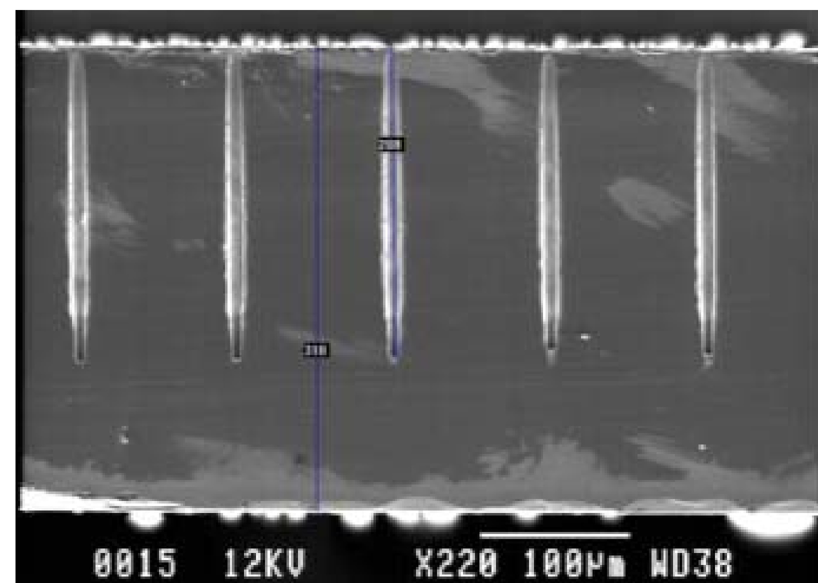
From 1/C2 the estimated junction column depth is 190um
(not optimized, as expected)



Wafers thickness 300um

Depleted region under 3D-stc diodes is about ~ 110 - 125um

30-50pA (~2.56mm2; 16x16 or 20x20 colums)



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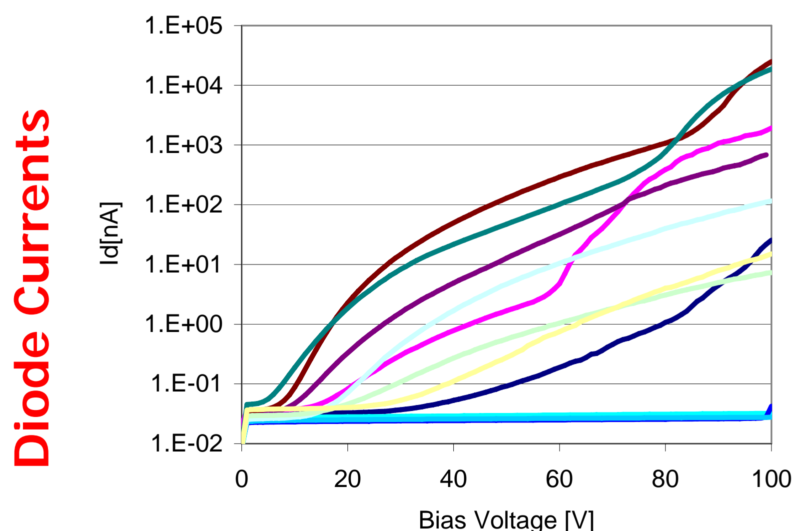
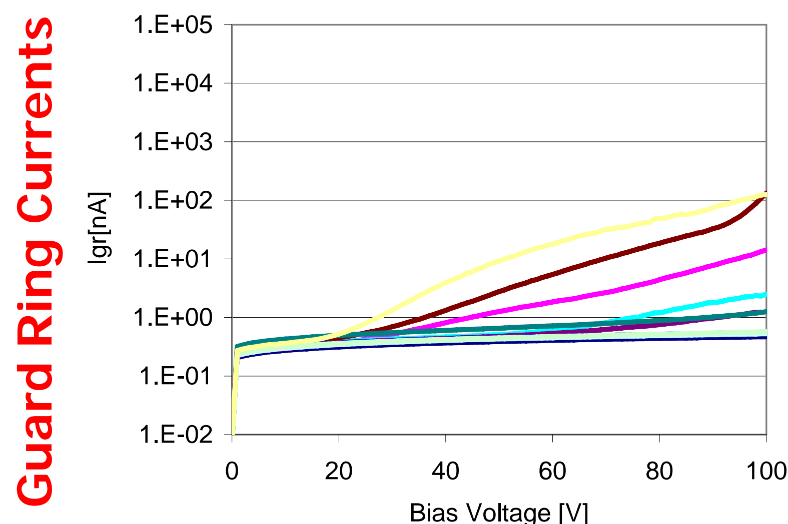
3D-ddtc diodes I-V measurements



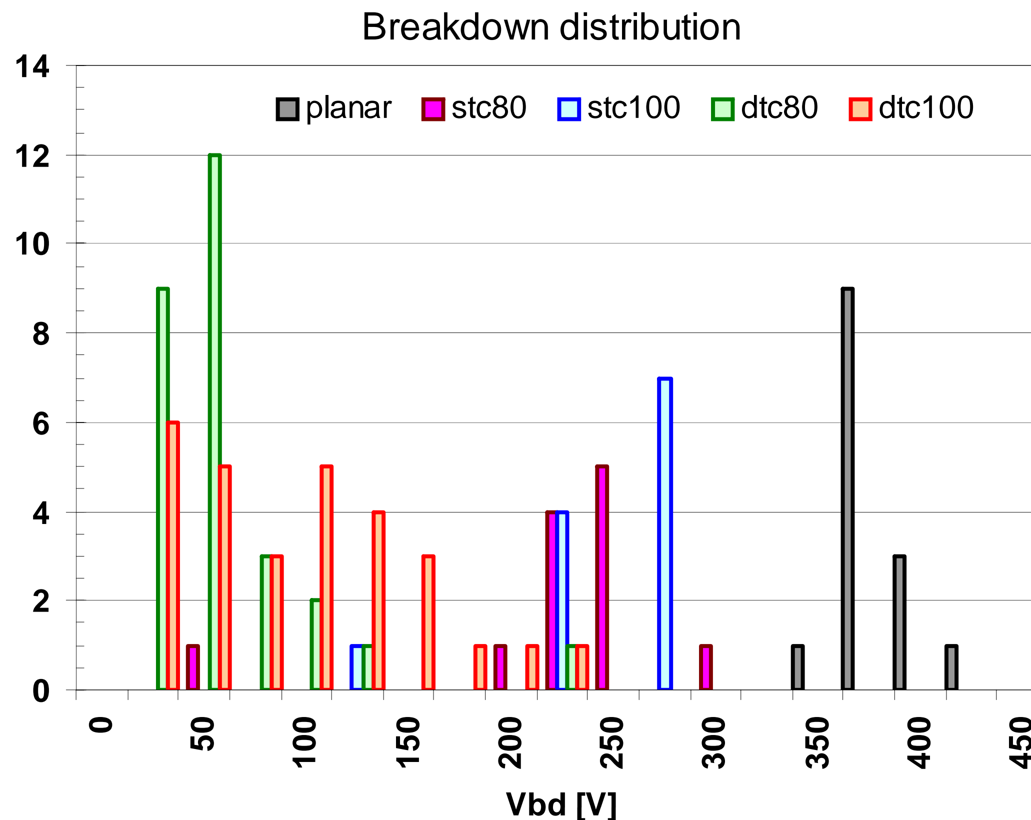


Some DDTC diodes exhibit low dark current similarly to STC ones

Some DDTC diodes show early *"breakdown"* (current raise) already at low voltage

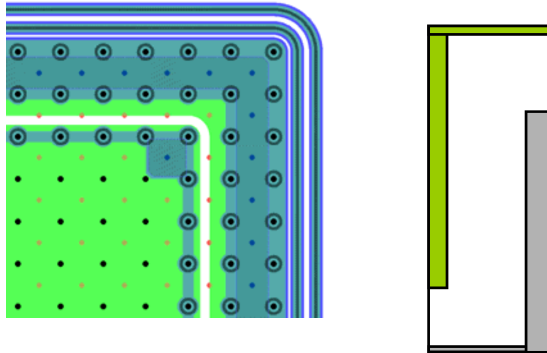
- This effect is present both on main diode and guard ring, but more frequently on the diode.
- This suggests a dependence on the number of columns (diode = 256, guard-ring =144)

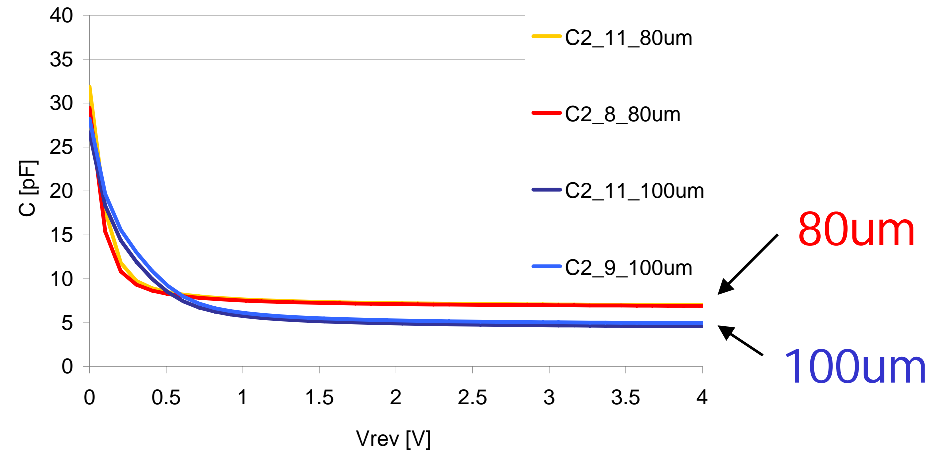
3D & planar diodes *"breakdown"* distribution



- Planar Diode (single guard ring) show a VBK ~ 400V
- DTC diodes show early *"breakdown"* in comparison with STC

3D-ddtc diodes, C-V

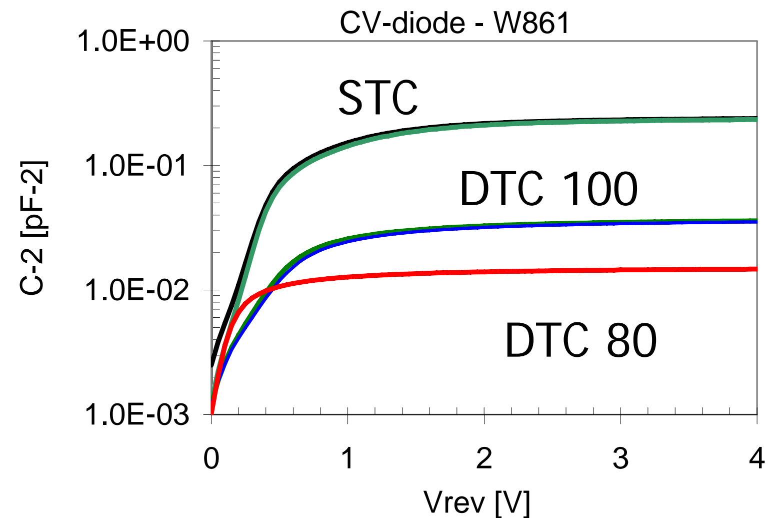




Lateral depletion occurs already at built-in voltage.

Full depletion at 2V.

DTC 80 capacitance saturates before DTC 100 because of the shorter electrode distance.



C_{3D_80um} (400cols) = 7pF
C_{3D_100um} (256 cols) = 4.8pF

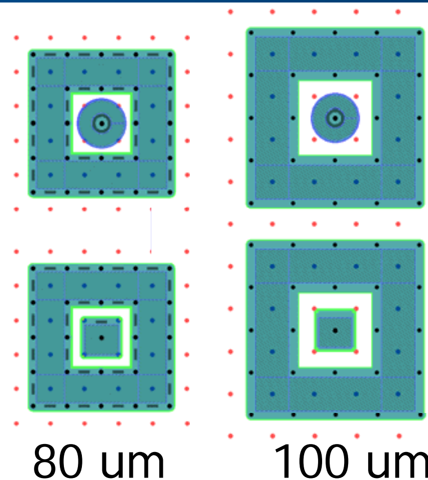
18 fF/column

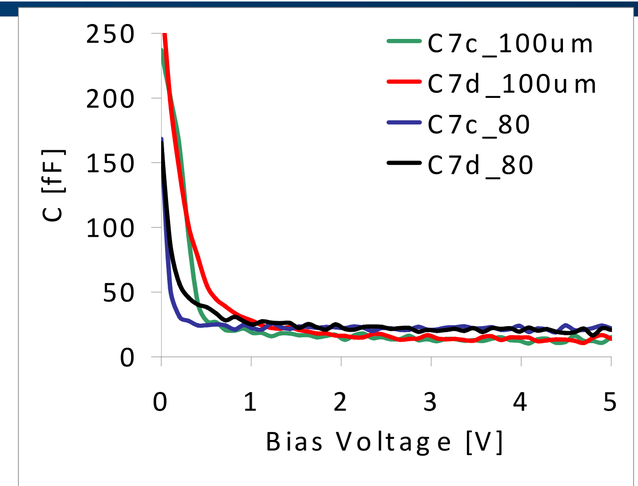
C-V on DDTC test structures (1 col.)

The C-V on 1-column diodes gives:

C_{80} = 20 fF
C_{100} = 18 fF

In good agreements with previous C-V measurements on large diodes.





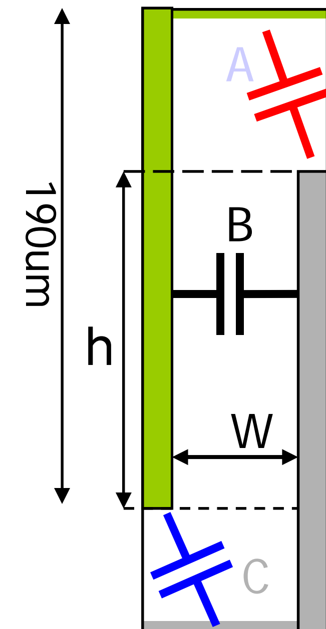
C-V simulation

Simulations made with different h coefficient
In order to find the value of the ohmic column depth.
The structure that fit measurements has ohmic column penetrating 160um into the substrate (not optimized, worse than expected)

Because B contribution is dominant,
a rough capacitance calculation with the following formula has also been performed :

$$C_{CYL} = 2\pi\varepsilon \cdot \frac{h}{\ln W}$$

and fits measures with h= (50 ÷ 60)um→ 160-170um back column etching



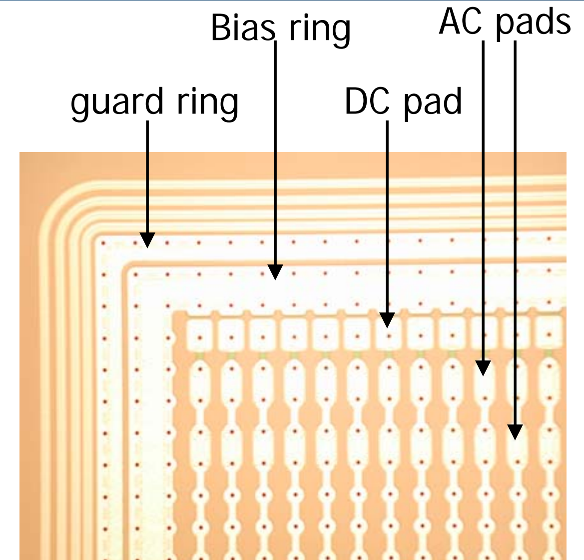
Strip detectors

For each detector:
horizontal pitch= vertical pitch
number of columns = number of strips

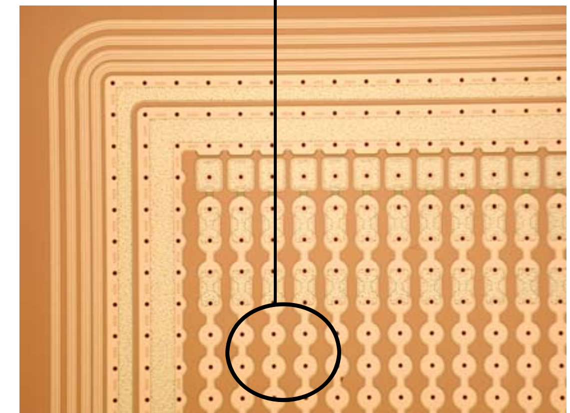
→ Square detectors
Cell size = $(1x1)cm^2$

All strips biased by punch-through

type	pitch	columns (strips)	readout	Radius (um) Surf. implant
STC	80	102	dc	22
STC	80	102	ac	22
STC	100	81	dc	22
STC	100	81	ac	22
DTC	80	102	dc	22
DTC	80	102	ac	22
DTC	100	81	dc	22
DTC	100	81	ac	22
DTC	80	102	ac	30
DTC	100	81	ac	33
DTC	100	81	ac	43



30um radius surface implant
(other surface geometries available)



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3D-sdtc and ddtc detectors I-V measurements

Measurements performed on one wafer

30 strip square detectors Cell size = $1x1cm^2$

total IV and DC scan @ 5V, 10V, 50V

Results

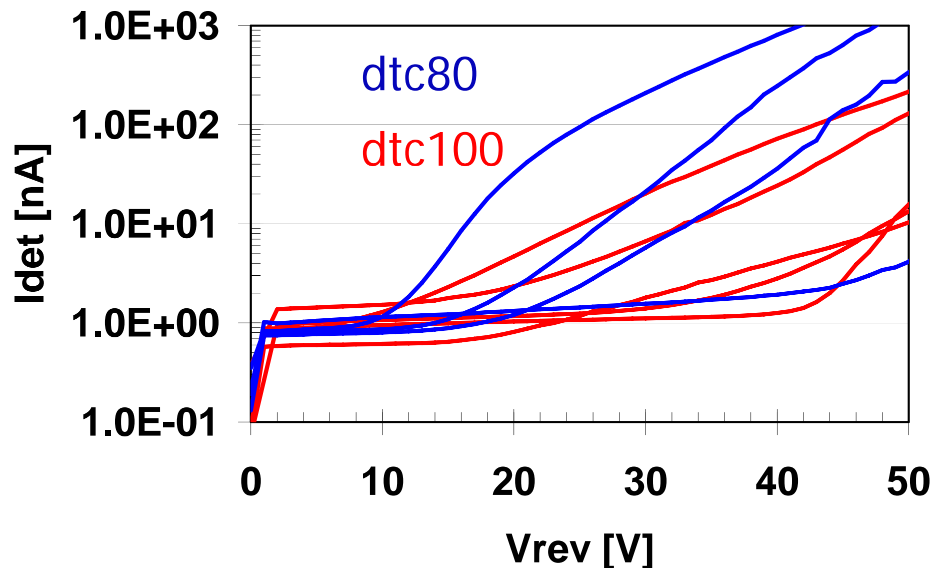
STC show a good characteristic

DTC detectors exhibit an early *"breakdown "*.

We need to investigate on forthcoming wafers if the problem is still present

BUT: *"Breakdown"* starts between 10V and 20V

Full depletion@2V → detectors are fully working in the low voltage range.



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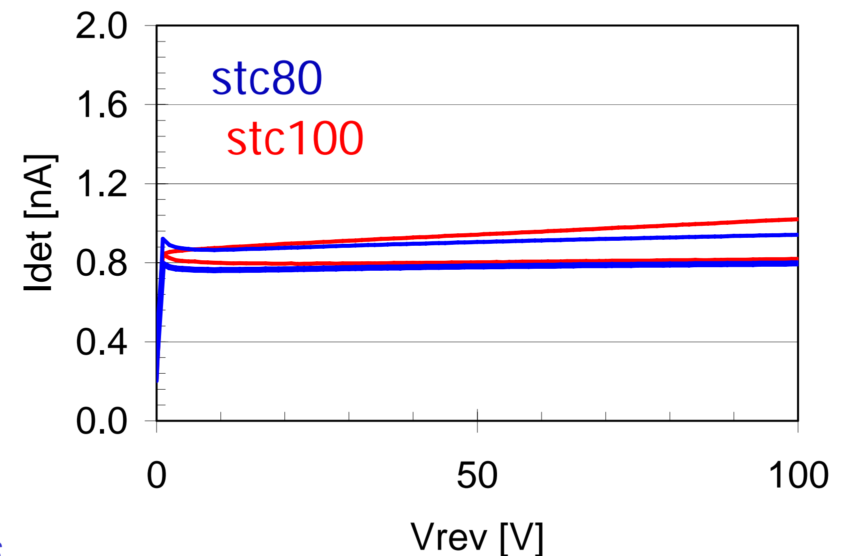
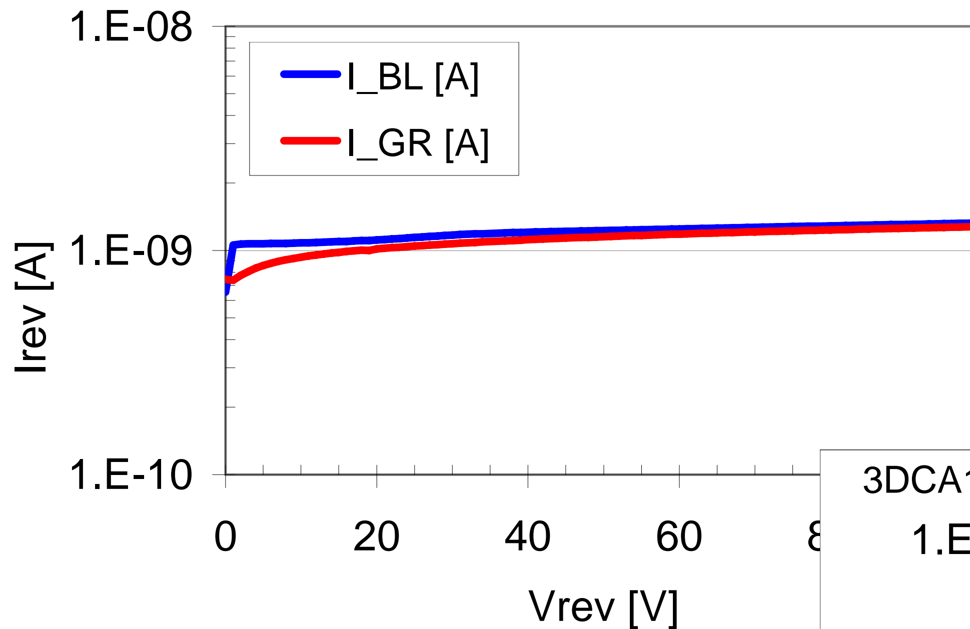
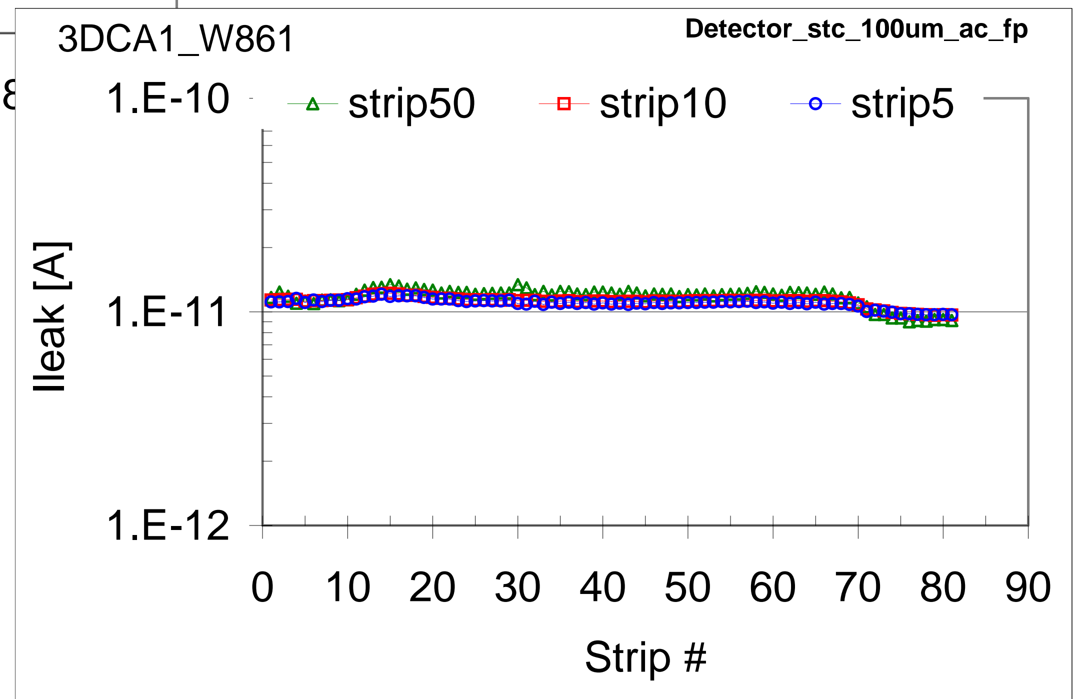


3D-sdtc detectors I-V measurements D16





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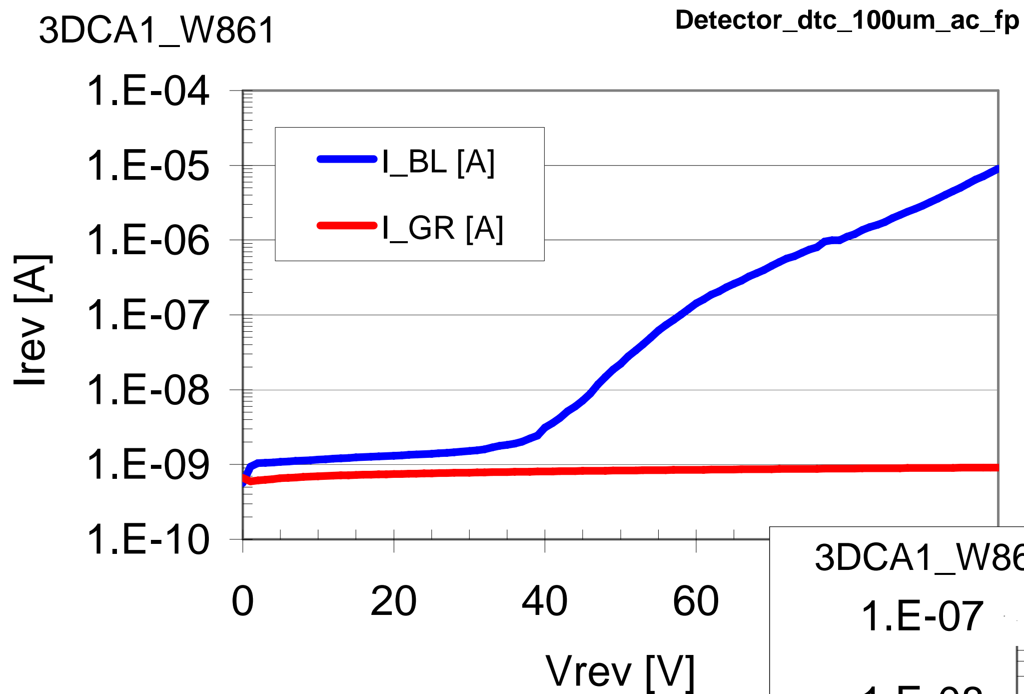
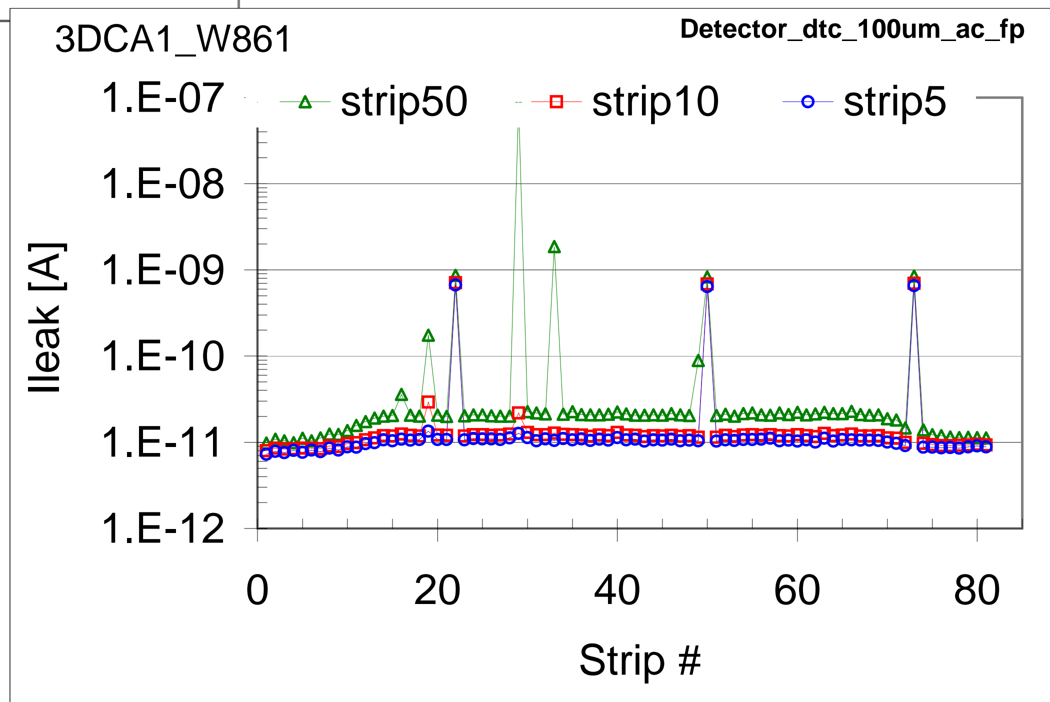
3D-ddtc detectors I-V measurements D13





M. Boscardin

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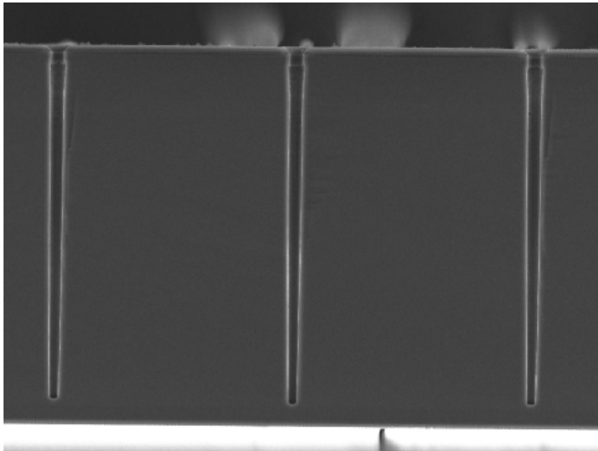
Deep-RIE equipment

- D-RIE Adixen AMS200
- Preliminary tests made for passing-through etching
- Available for processing



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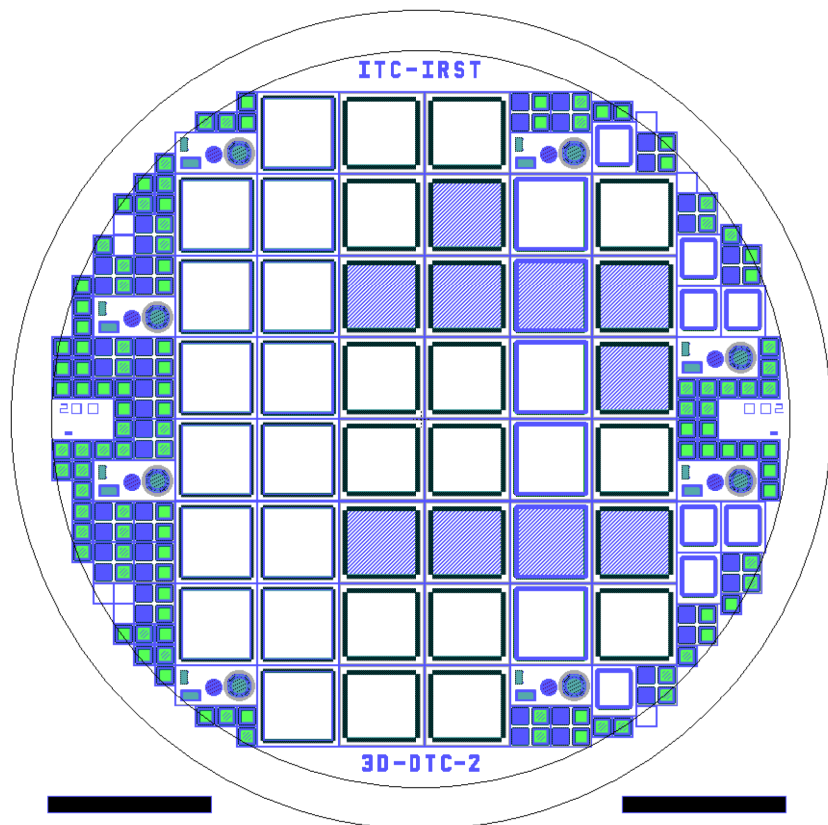
Next batch: n-on-p devices

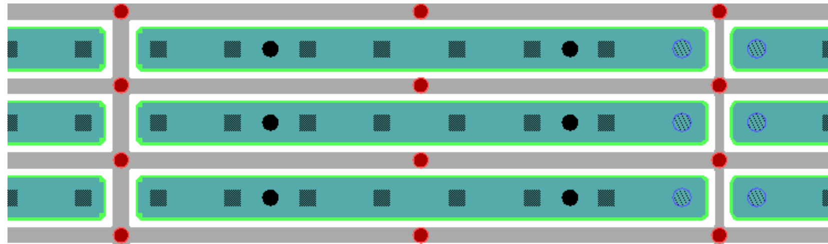
- Few wafers of n-on-p detectors made with external DRIE under way
- New batch with in-house DRIE due by end of july



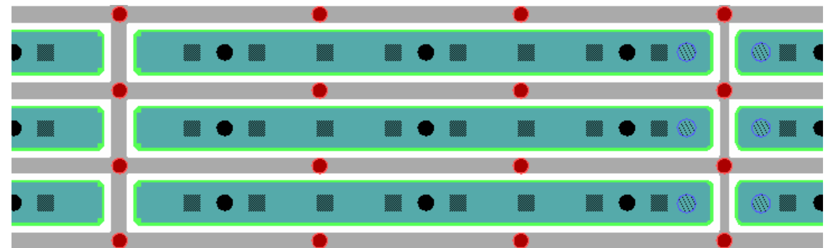
Batch	3D-DDTC 2
Substrate type	p-type
Substrate thickness	200 µm
Column depth	180 µm
Layout	13 microstrip detectors AC/DC coupled
	6 CMS pixel detectors
	22 ATLAS pixel detectors

3D – DDTC2: ATLAS pixel detectors

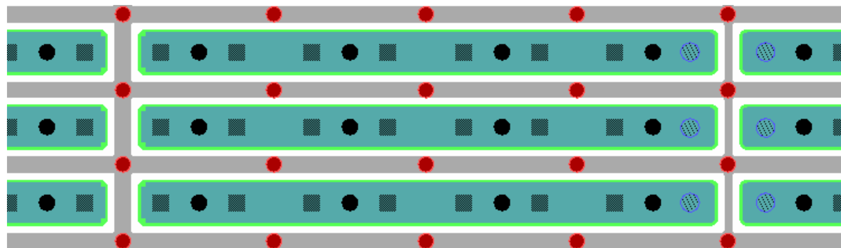
double tc version



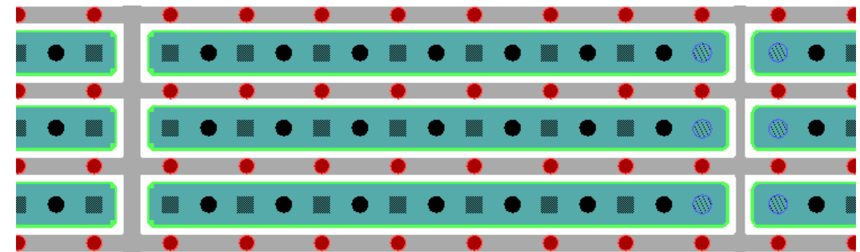
200µm-pitch   2 columns/pixel



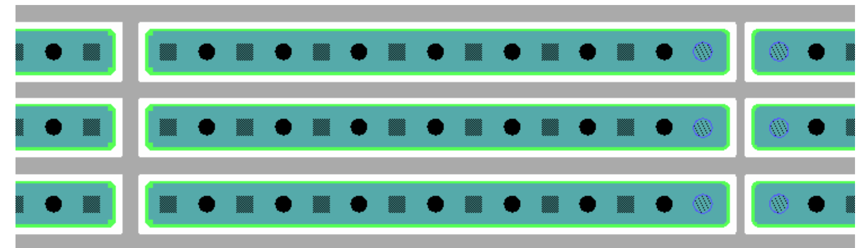
133µm-pitch   3 columns/pixel



100µm-pitch   4 columns/pixel



50µm-pitch   7 columns/pixel



single tc version

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Conclusions

- First batch of DDTC has been finally realized!
- Detectors feature columns of both doping types, but the process (column depth) is not optimized.
- Test structures and detectors were electrically tested, automatic testing (scans) on strip detectors to be completed.
- STC are perfect, DTC show early breakdown (with probability proportional to the area → defects).
- In spite of the non optimized column depth, simulations show a large improvement in the collection time with respect to STC. Functional measurements are under way.
- In-house DRIE equipment now available
- 3D-DDTC on p-type substrates (including ATLAS pixel layout) should be completed by the end of july

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