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3rd Workshop on Advanced Silicon Radiation Detectors

Barcelona
April 2008

3D interconnection for pixel detectors

Warning: this talk is **not** about 3D detectors

3D interconnection stands for new technologies to interconnect semiconductor devices

The term is used by the ITRS
(International Roadmap for Semiconductors)

It's also called "vertical interconnection"

It concerns mostly ASICs

It can be interesting for detectors
(even 3D detectors)

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3D Workshop one week ago

Vertical Integration Technologies for HEP and Imaging Sensors

6-9 April 2008 Ringberg Castle, Lake Tegernsee

Home

- Overview
- Scope of the Workshop
- Timetable
- Registration
- List of Participants
- Accommodation

Vertical Integration and High Density Interconnection Technologies for HEP and Imaging

There is considerable interest of the detector community in the opportunities offered by the new developments in the field of vertical integration of electronic components. This became evident in the very successful first 3DIT Workshop at Palaiseau end of November 2007. The semiconductor industry and the major process equipment manufacturer are very active in this field and the main objective of this workshop will be to investigate how the detector community can contribute and take advantage of these developments.
The interconnection of different technologies like for the sensors, analogue, and digital ASICs offers obviously a lot of advantages but R&D and prototyping in this field can be very cost intensive. One of the goals of this workshop is the formation of a common platform for the R&D on vertically integrated pixel detector systems which then would give the opportunity to share the experience and open new possibilities for the organization of common projects for LHC and ILC detector development.

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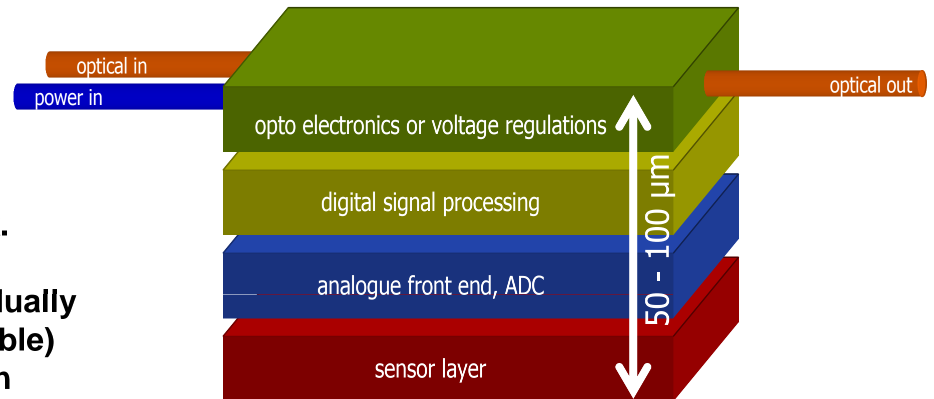
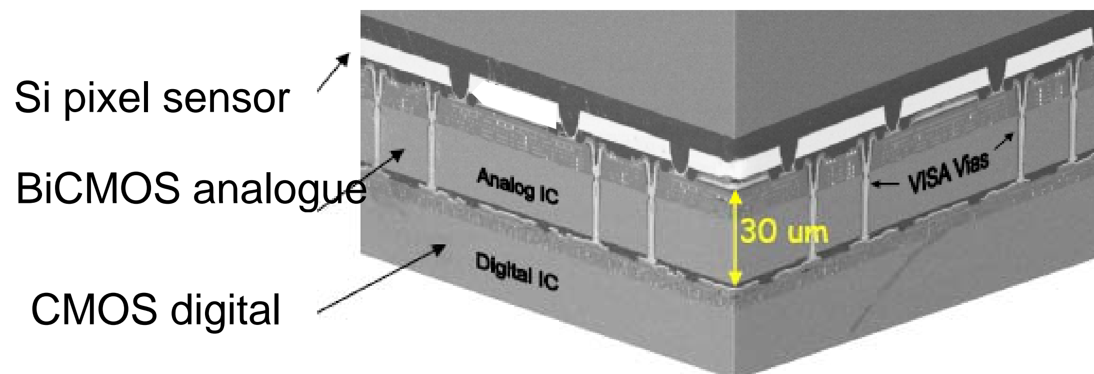
3D interconnection for pixel detectors

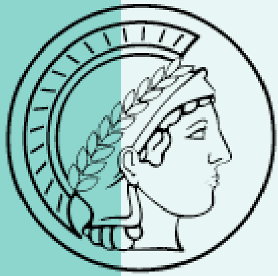
Two or more layers (="tiers") of thinned semiconductor devices interconnected to form a "monolithic" circuit.

- Different layers can be made in different technology (BiCMOS, deep sub-μ CMOS, SiGe,…..).

- 3D is driven by industry:
  - Reduces R,L and C.
  - Improves speed.
  - Reduces interconnect power, x-talk.
  - Reduces chip size.
  - Each layer can be optimized individually
  - Backside connectivity (4-side buttable)
  - Low cost, fine pitch interconnection







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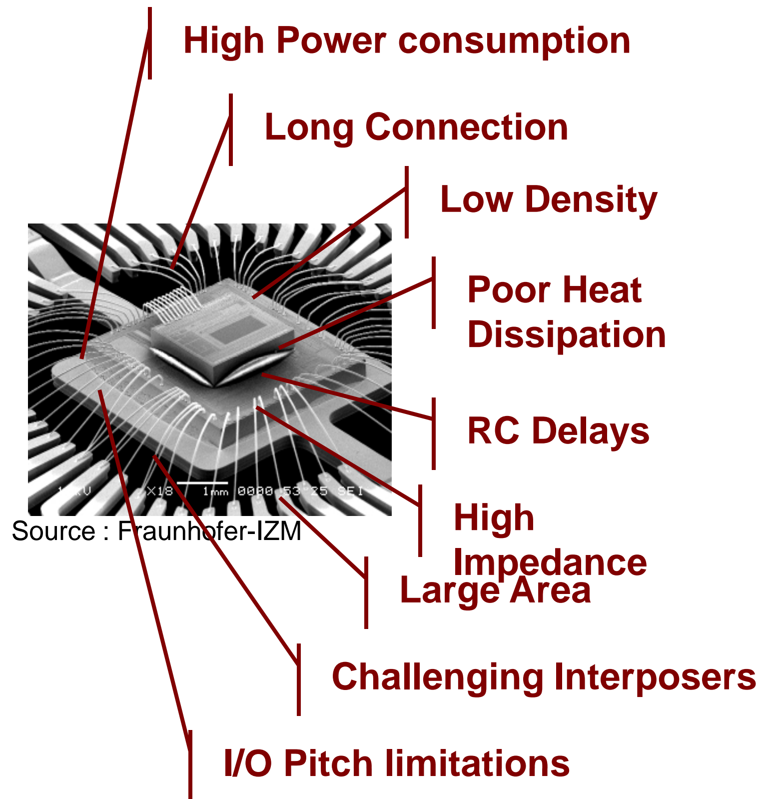
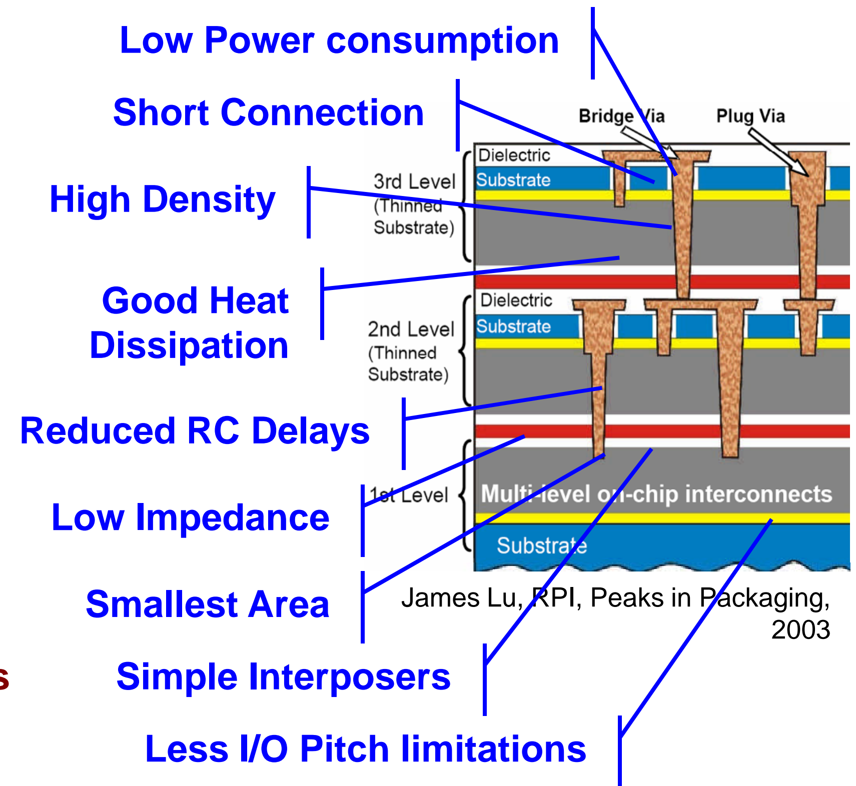
Industry Vision



Source : Fraunhofer-IZM



James Lu, RPI, Peaks in Packaging, 2003

3D will be used for:

memories (memory cards), optical sensors (CMOS), smart cards

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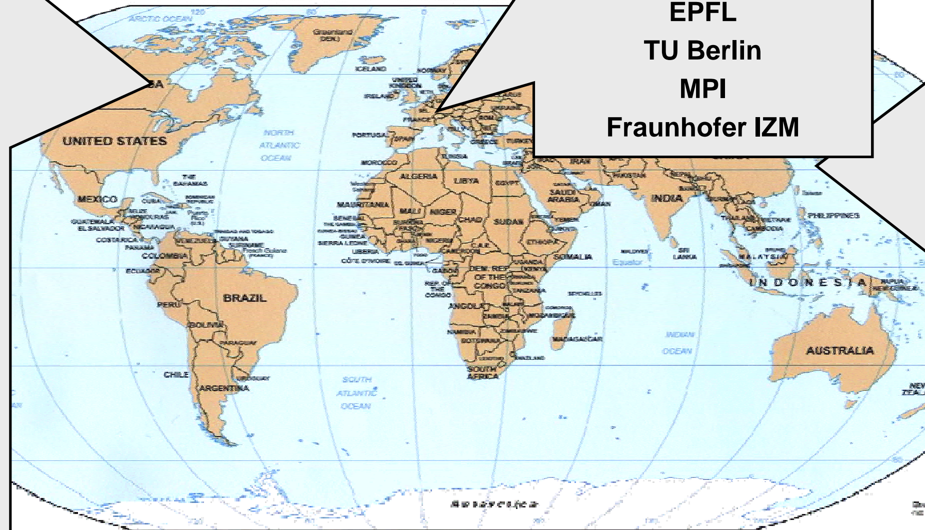
Global Activities in 3D Integration

IBM
Intel
Micron/Avago
Freescale
Tru-Si Technologies
Texas Instruments
Vertical Circuits
AT & T
Tessera
Tezzaron
Rensselaer Institute
University of Arkansas
Sandia National Labs
MCNC-RDI
MIT
Ziptronix
Irvine Sensors



Infineon/Qimonda
Philips
Thales
Alcatel Espace
NMRC
CEA-LETI
IMEC
EPFL
TU Berlin
MPI
Fraunhofer IZM

Samsung
Hynix
ASET
NEDO : Oki/NEC/Elpida
Tohoku University
University of Tokyo
ZyCube
CREST
Fujitsu
Sanyo
Sony
Toshiba
Denso
Mitsubishi
Sharp
Hitachi
Matsushita
TSMC
SPIL

e.g.:
Consortium created for cost effective development of 3D technology: materials, equipment and technology
(Semitool, Alcatel, EVG, Fraunhofer, LETI, SAIT, KAIST..)

3D Roadmap

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Memory

Via : >20um by Laser
Hole : <100
t : <50um

NAND

MCP

POP

Via : 1-5um
Hole : <1000
t : 20-50um

DRAM

Dram
Si Interposer

CMOS image sensors & memories (NAND, DRAM & NOR + Logic) are requiring 3D stacking with TSVs.
(Via sizes are variable depending upon applications.)

→Thin wafer
→Multi-layer

Multi function OC

t=>50um
Via : 5-10um
Hole : >100K
t=<200 um

Dram
Dram
Logic

Sensor
Logic
Analog
RF
DRAM
MPU

CMOS Image Sensor

High Speed

Multi Function

→ Small vias
→ Vias density

CIS
Dram
Logic
Organic Interposer

CIS
Si Interposer
DSP

Via : 40um
Hole : <100
t=200um

CIS
Organic Interposer

2005 2006 2007 2008 2009 2010 2011 2012 2013 2014

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IBM Press Release

the third-dimension

Breakthrough demonstrates viability of 3-D chip stacking technique for manufacturing

ARMONK, N.Y., April 12, 2007 -- IBM today announced a breakthrough chip-stacking technology in a manufacturing environment that paves the way for three-dimensional chips that will extend Moore's Law beyond its expected limits. The technology – called "through-silicon vias" -- allows different chip components to be packaged much closer together for faster, smaller, and lower-power systems.

The IBM breakthrough enables the move from horizontal 2-D chip layouts to 3-D chip stacking, which takes chips and memory devices that traditionally sit side by side on a silicon wafer and stacks them together on top of one another. The result is a compact sandwich of components that dramatically reduces the size of the overall chip package and boosts the speed at which data flows among the functions on the chip.

"This breakthrough is a result of more than a decade of pioneering research at IBM," said Lisa Su, vice president, Semiconductor Research and Development Center, IBM. "This allows us to move

[High-res image]

IBM extends Moore's Law to the third-dimension: An IBM scientist holds a thinned wafer of silicon computer circuits, which is ready for bonding to another circuit wafer, where IBM's

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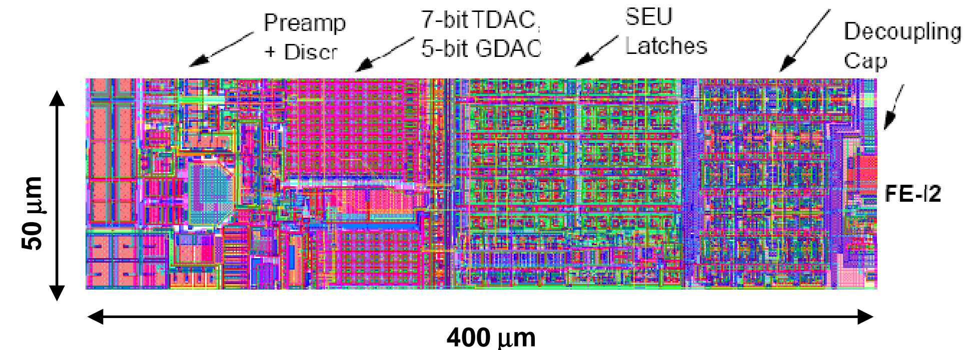
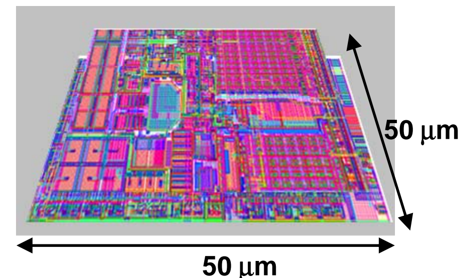
Advantages of 3D for HEP detectors

Multilayer electronics:

Split analogue and digital part
Use different, individually optimized technologies:

-> gain in performance, power, speed, rad-hardness, complexity.
-> smaller area (reduce pixel size or more functionality).





50 x 400 μm^2 (0.25 μm)
May shrink to ~ 50 x 50 μm^2 (130 nm)

4-side abuttable devices:

-> no dead space.
-> simpler module layout.
-> larger modules.

(reduce complexity and material)

Conventional CMOS sensor
(optical, similar: MAPS)

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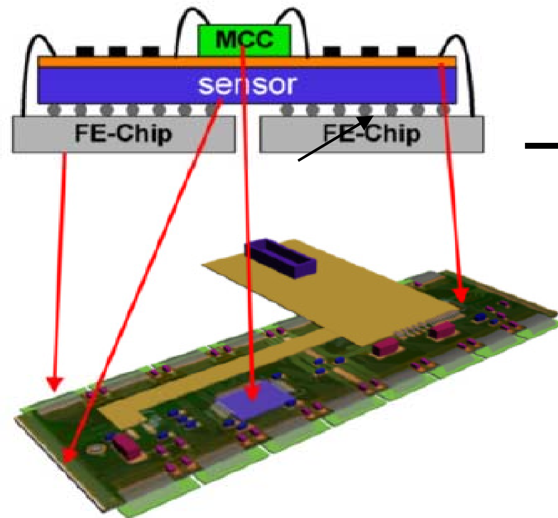
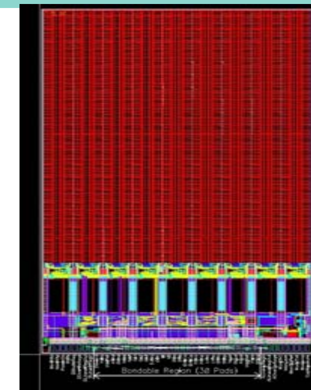
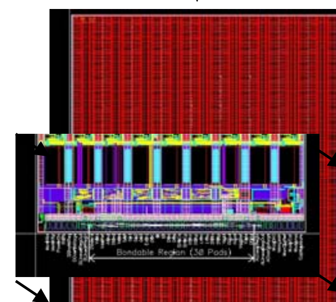
Advantages for Module Design

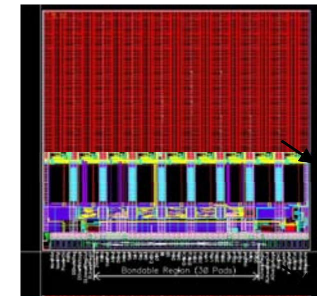




Pixel area
(facing sensor)

Periphery
Pipeline and control
Bond pads
(cantilever)

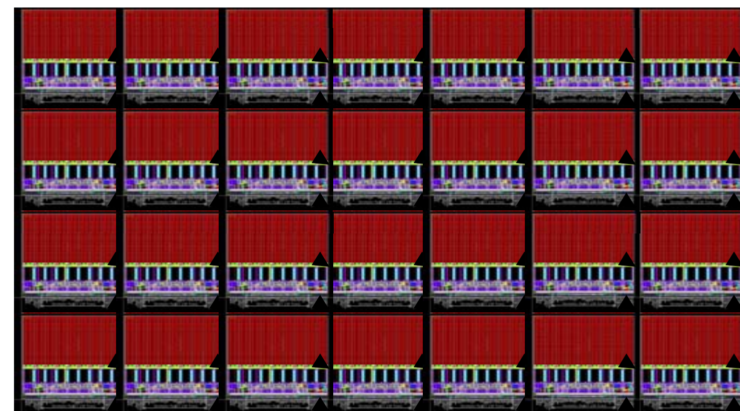




Control on top of pixel area.
External contact from top.
Contact pixels through vias:
-> 4-side buttable.
-> No "cantilever" needed.

Larger module with minimal dead space.

Less support structures & services.
Substantial material savings.



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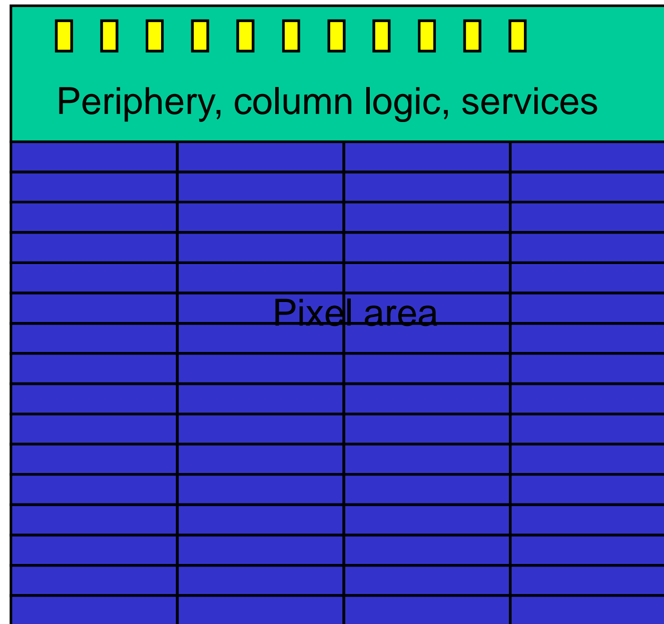
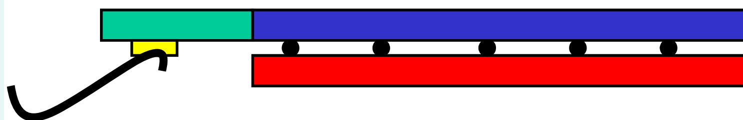
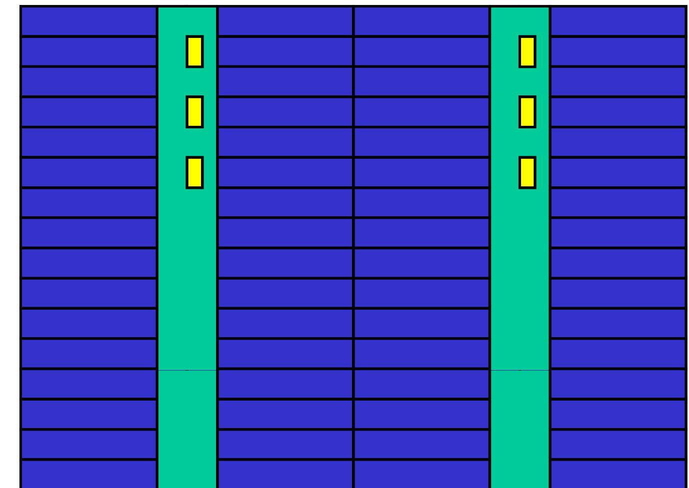
Advantages even for single layer

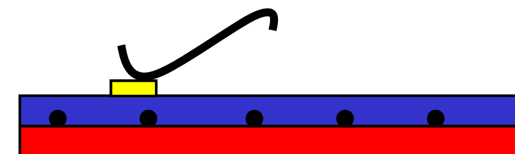
Conventional Layout





3D Layout





Make use of smaller feature size (gain space)
-> move periphery in between pixels (can keep double column logic)
-> backside contacts with vias possible
-> no cantilever needed, 4-side abuttable

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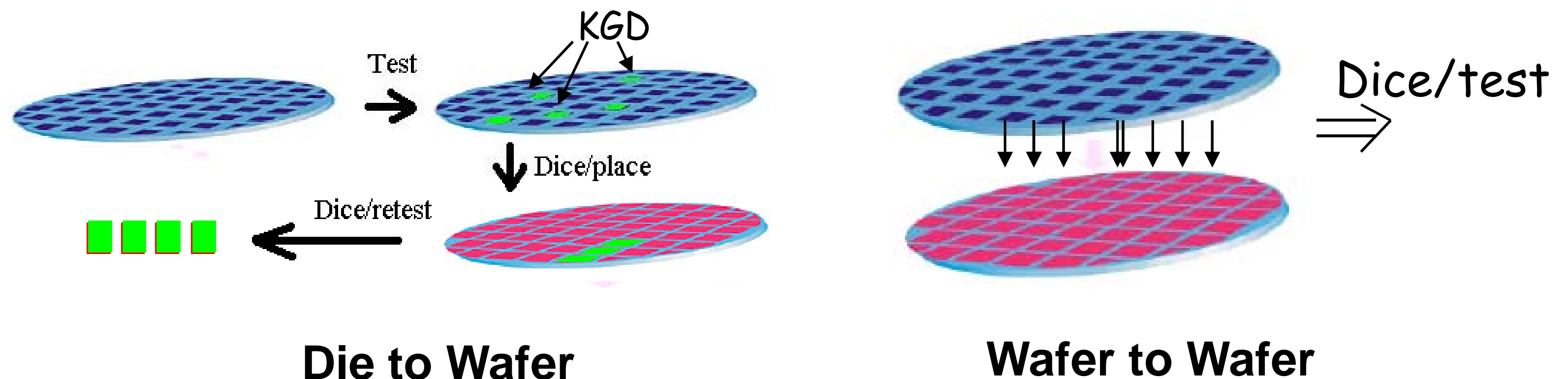
Two Different 3D Approaches

Wafer to Wafer bonding

- Must have same size wafers
- Less material handling but lower overall yield

Die to Wafer bonding

- Permits use of different size wafers
- Lends itself to using KGD (Known Good Die) for higher yields



Die to Wafer **Wafer to Wafer**

Die to Wafer processing -> optimal for prototyping

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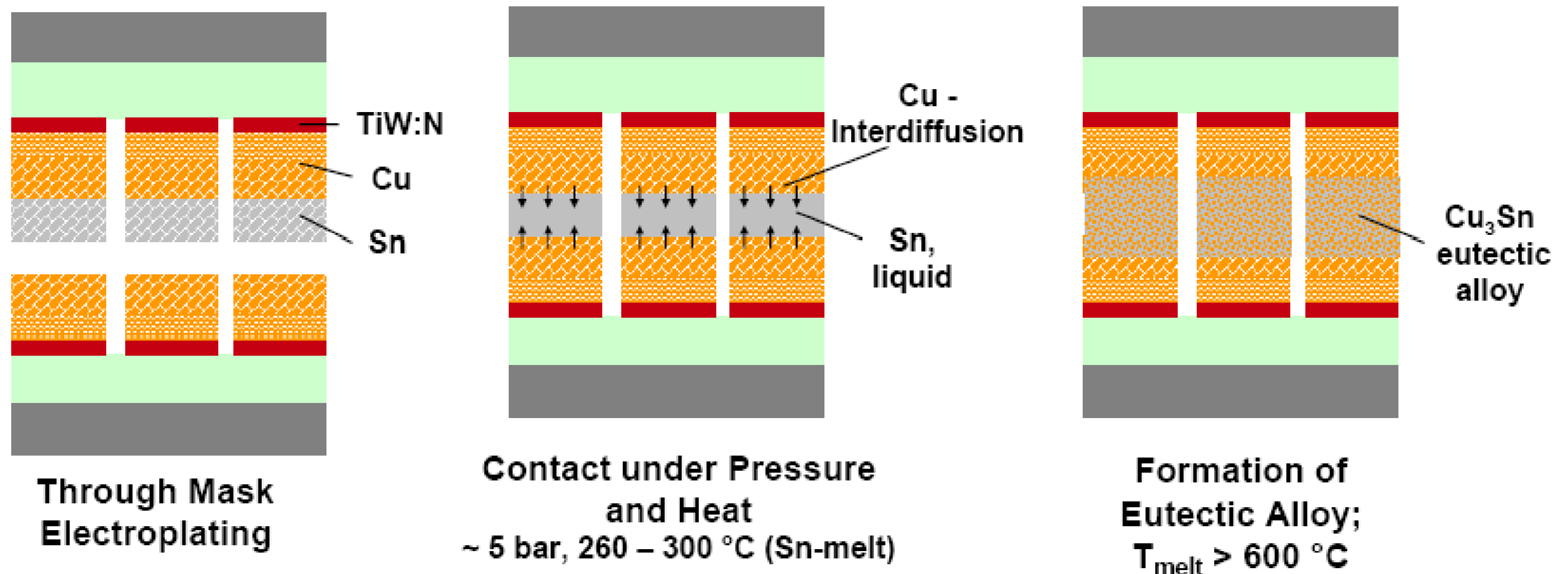
IZM SLID Process

Metallization SLID (Solid Liquid Interdiffusion)



- Alternative to bump bonding (less process steps "low cost" (IZM)).
- Small pitch possible (<< 20 μm, depending on pick & place precision).
- Stacking possible (next bonding process does not affect previous bond).
- Wafer to wafer and chip to wafer possible.

IZM
Fraunhofer Institut Zuverlässigkeit und Mikrointegration

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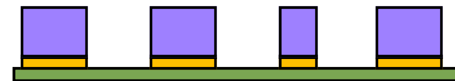
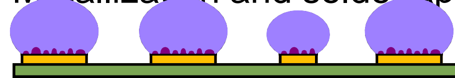
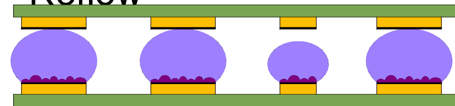
Comparison: bump bonding - SLID



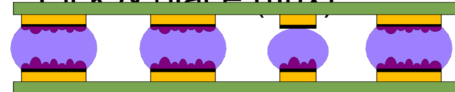
Metallization and solder apply



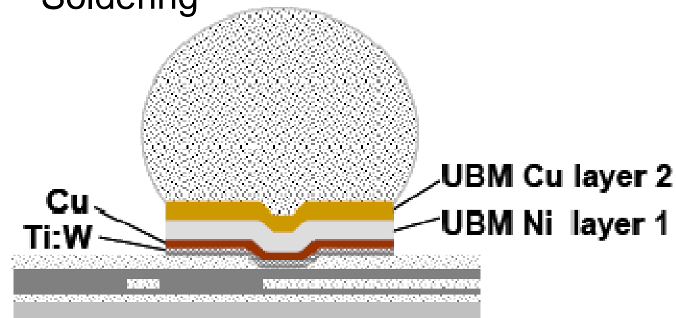
Reflow



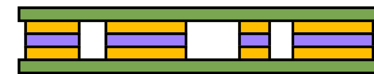
Pick & place (flux)



Soldering

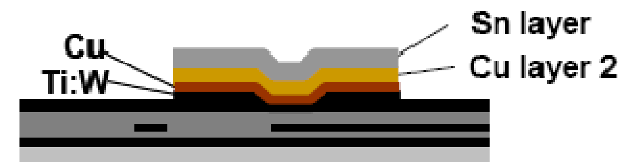


Metallization and solder apply



Pick & place (no flux)

Soldering



More processing steps
Pitch limited by bump size
No complete alloy formed -> soft, less strength
No stacking
Rework possible

Less processing steps
Fine pitch (limited by alignment accuracy)
Complete alloy formed -> good strength
Stacking possible
No rework possible

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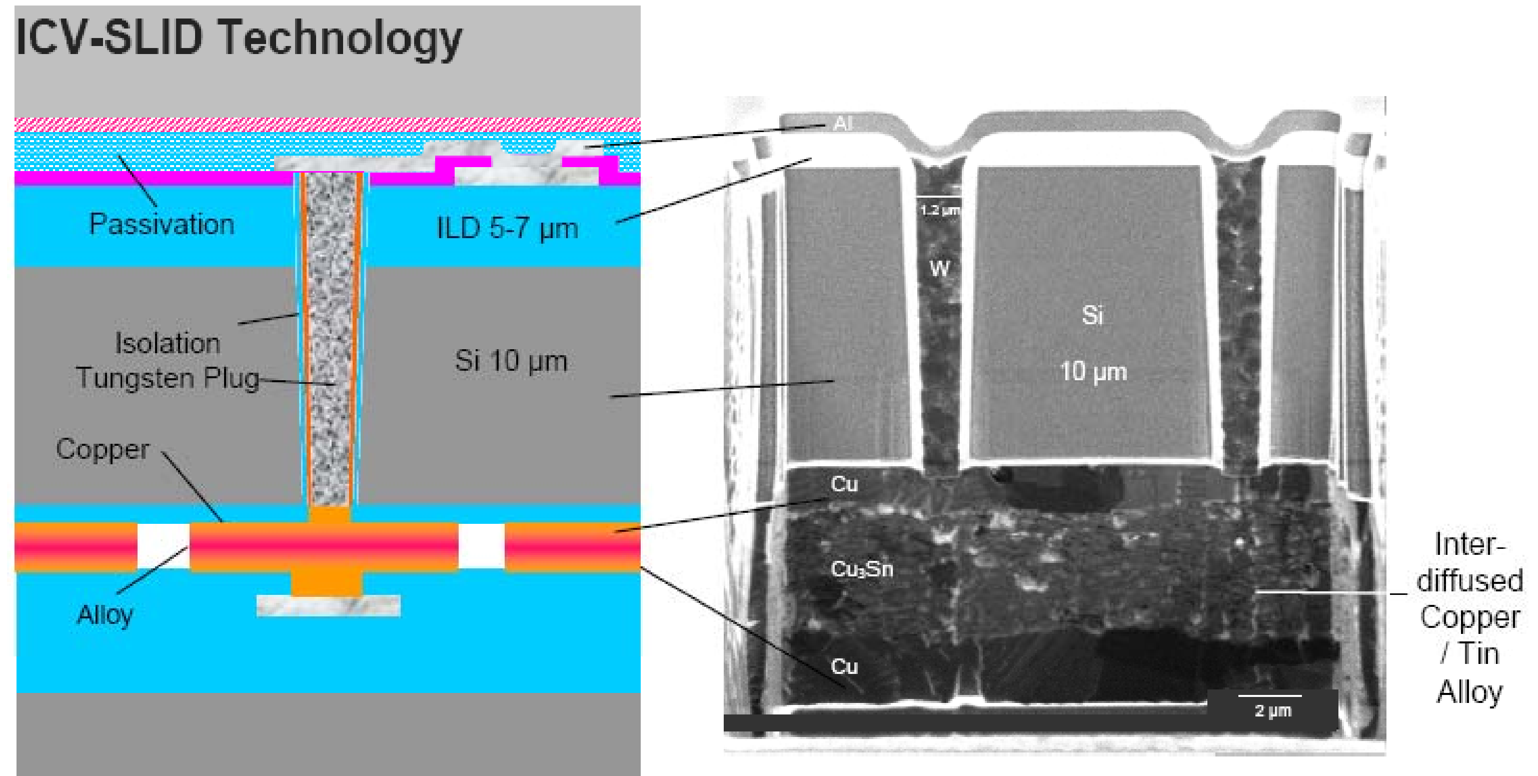
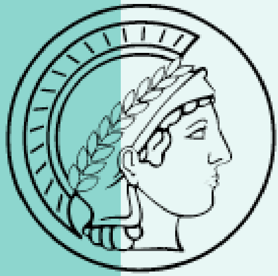
Through Silicon Vias



ICV = Inter Chip Vias

- **Hole etching and chip thinning**
- **Via formation with W-plugs.**
- **Face to face or die up connections.**
- **2.5 Ohm/per via (including SLID).**
- **No significant impact on chip performance (MOS transistors).**

Fraunhofer IZM
Institut Zuverlässigkeit und Mikrointegration



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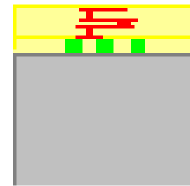
Vias last – vias first

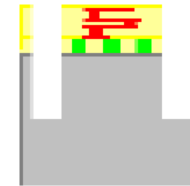
Two different concepts:

Via last: postprocess CMOS (and other) wafers with vias

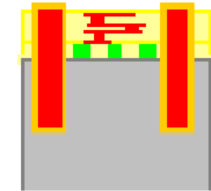
- any technology can be used (however, there might be restrictions)
- area for vias introduces dead area in CMOS chip
- complicated process flow



CMOS with space reserved for vias



Etch vias



Fill and contact vias

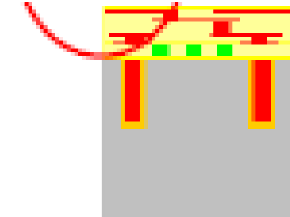
Via first: Vias etched before CMOS processeing

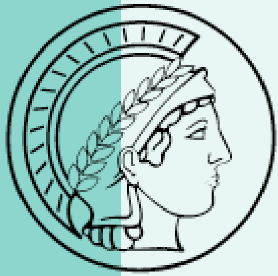
- integrated part of the CMOS process
- vias don't add dead area
- limited to few producers and technologies

Etch vias

Fill contact planarize

CMOS on top of vias





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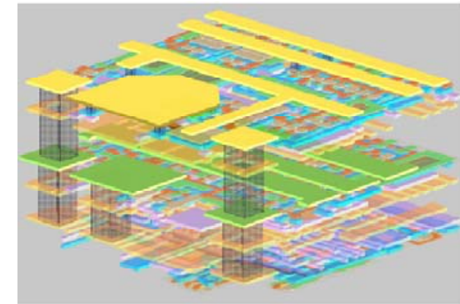
R&D activities

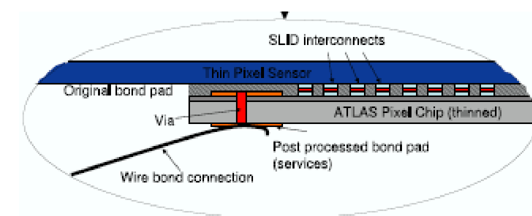
Fermilab: started about two years ago

- First tries with MIT – Lincoln Lab
- Move to Tezzaron/Ziptronics
- focused on complex ASICs



MPI Munich: just started

- Work with IZM-Fraunhofer
- focused on Sensor-ASIC interconnections



IN2P3 France

- Orsay, Marseille, Strasbourg, Paris
- several projects (multilayer ASICs, sensor-ASICs, 3D-MAPs)
- probably: ATLAS FEI4-3D using Tezzaron process

3D Integrated Technology Perspectives -
First workshop on LHC-ILC prospects
29-30 November 2007
Ecole Polytechnique

EU: DevDET FP7 call:

- includes 3DIT workpackage

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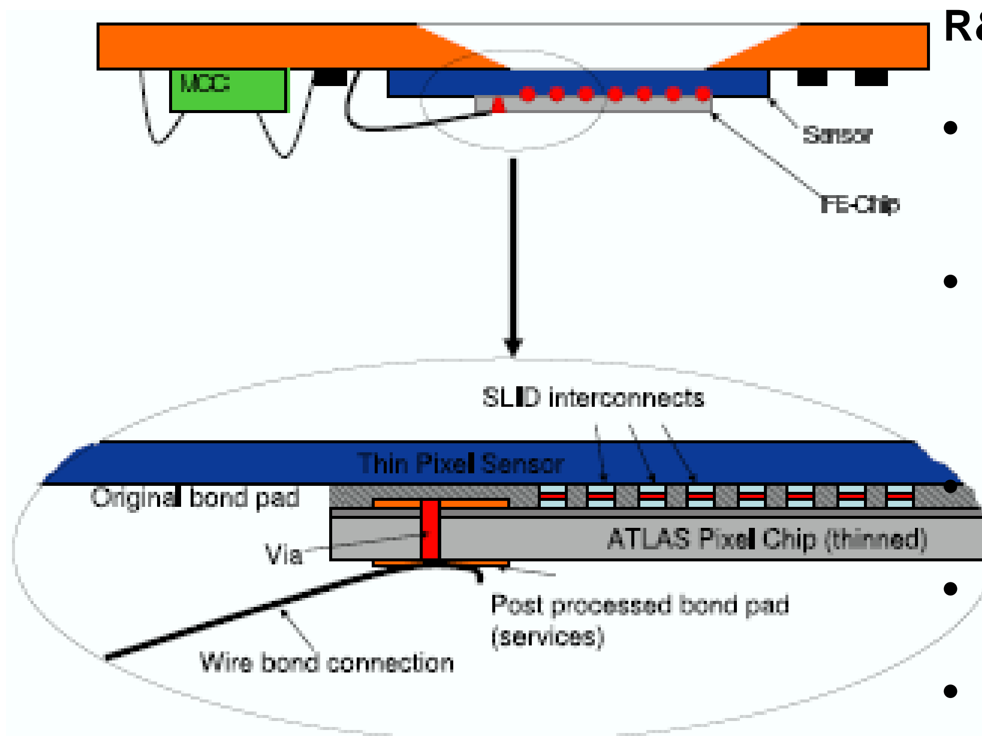
MPI 3D R&D Program

- Build demonstrator using ATLAS pixel chip and pixel sensors made by MPI
- Use the IZM Fraunhofer SLID and ICV technology



R&D Issues:

- Technology: compatible with sensors, ASICs?
- Interconnection quality: e.g. capacitance (face-to-face or die up?).
- Yield & Costs.
- Production in industry.
- Reduce material (copper layer).

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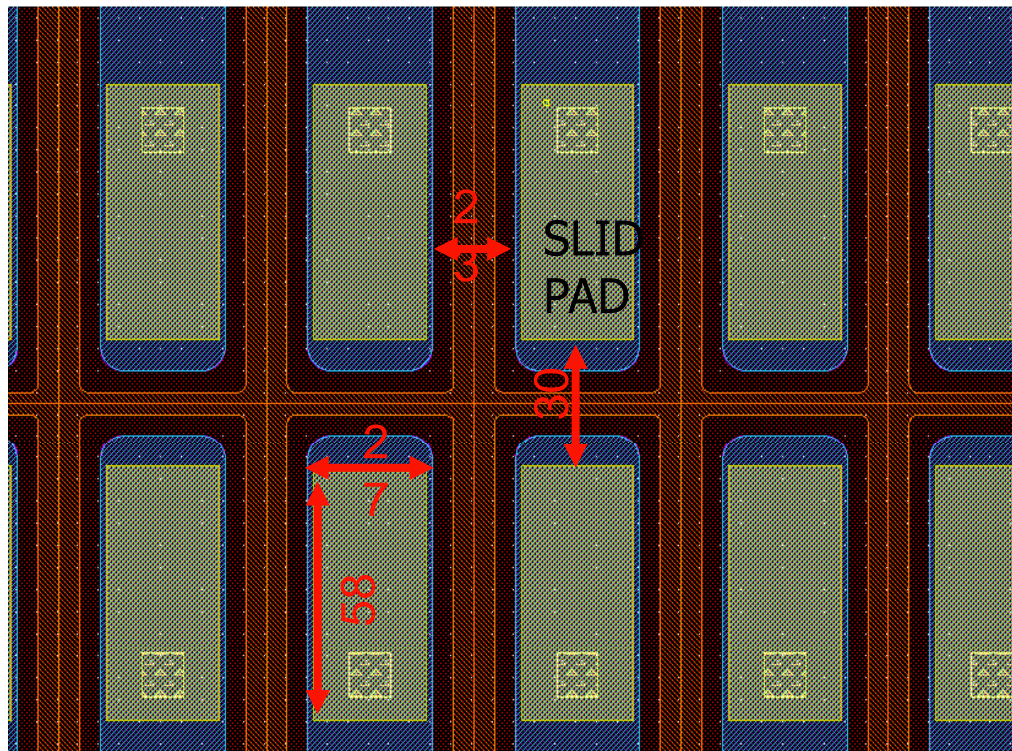
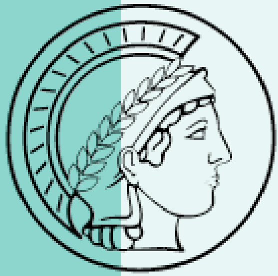
Test Pixel Matrices

- Pixel cells to be read out by a single FE chip (ATLAS FEI2)
- The active identical to standard Atlas pixels:
  DC coupled, isolation by moderated p-spray, punch-through biasing
- Added a guard-ring structure on the front side needed in the case of the n-in-p detectors



- width and distance between the SLID pads along the x-axis most critical parameter for the interconnection → IZM specs for SLID “chip to wafer” require slightly larger spacing to allow for possible misalignment of the chip in the handle wafer



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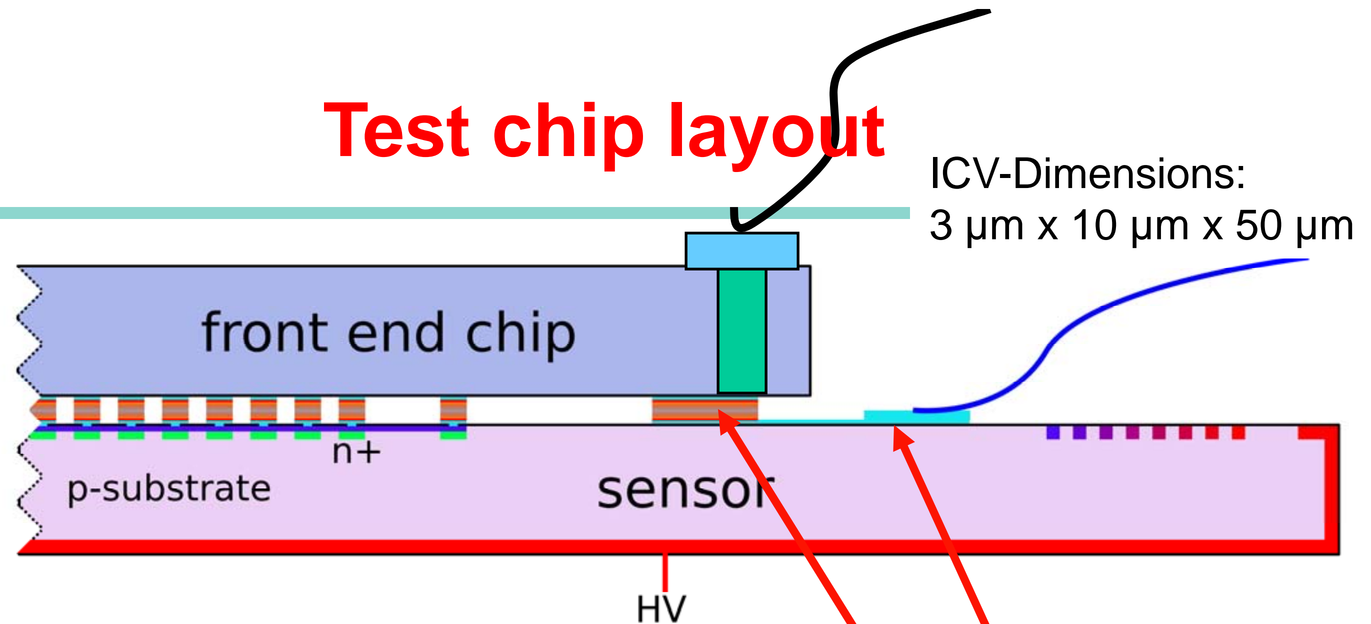
Test chip layout

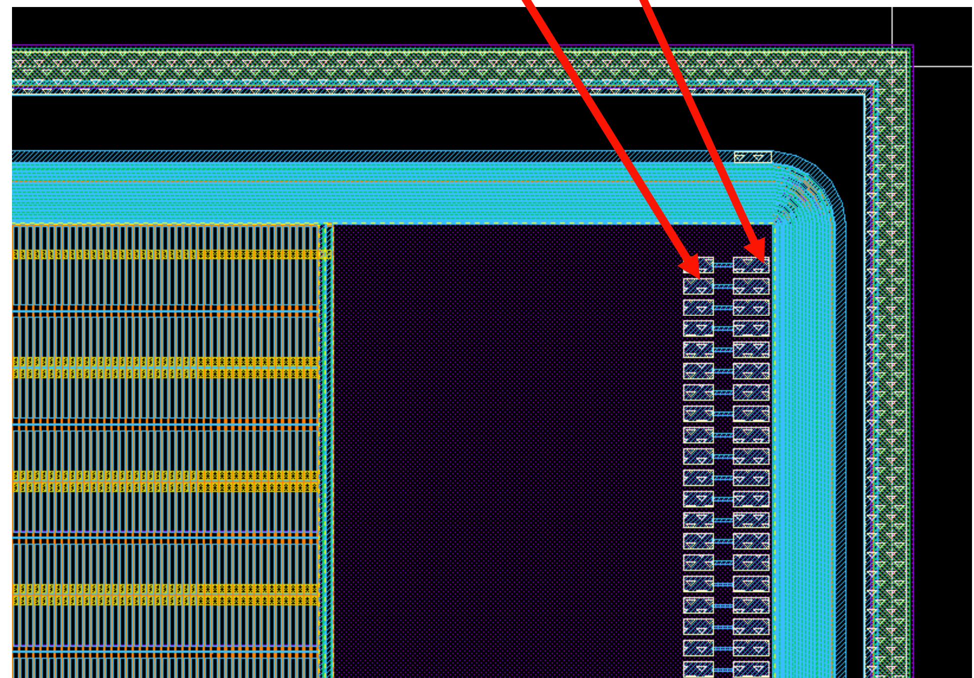
ICV-Dimensions:
3 µm x 10 µm x 50 µm



- *n-in-n: sensor edge at ground*
- *n-in-p: sensor edge at HV*
- *in future productions the GR extension can be avoided if BCB isolation is proved to stand the potential difference between detector and chip surfaces*

Chip can be serviced:

-using ICV (vias)
-fan-out (redundant)



Tests on Diodes at IZM

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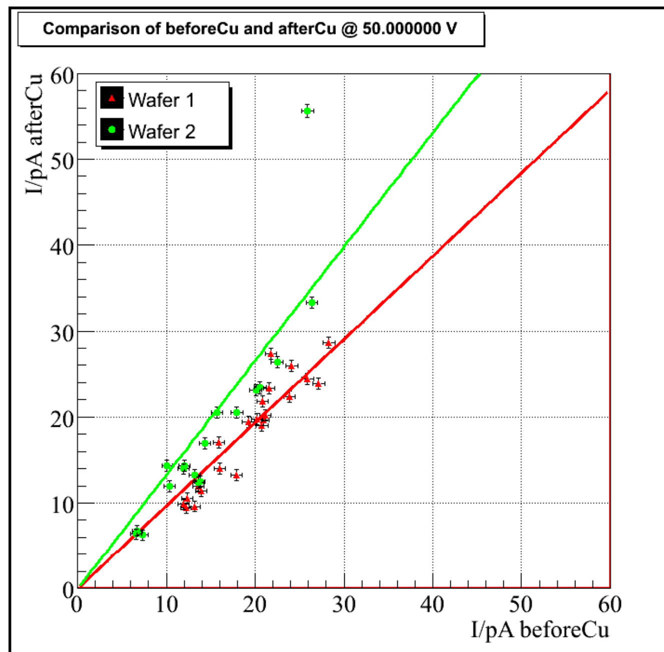
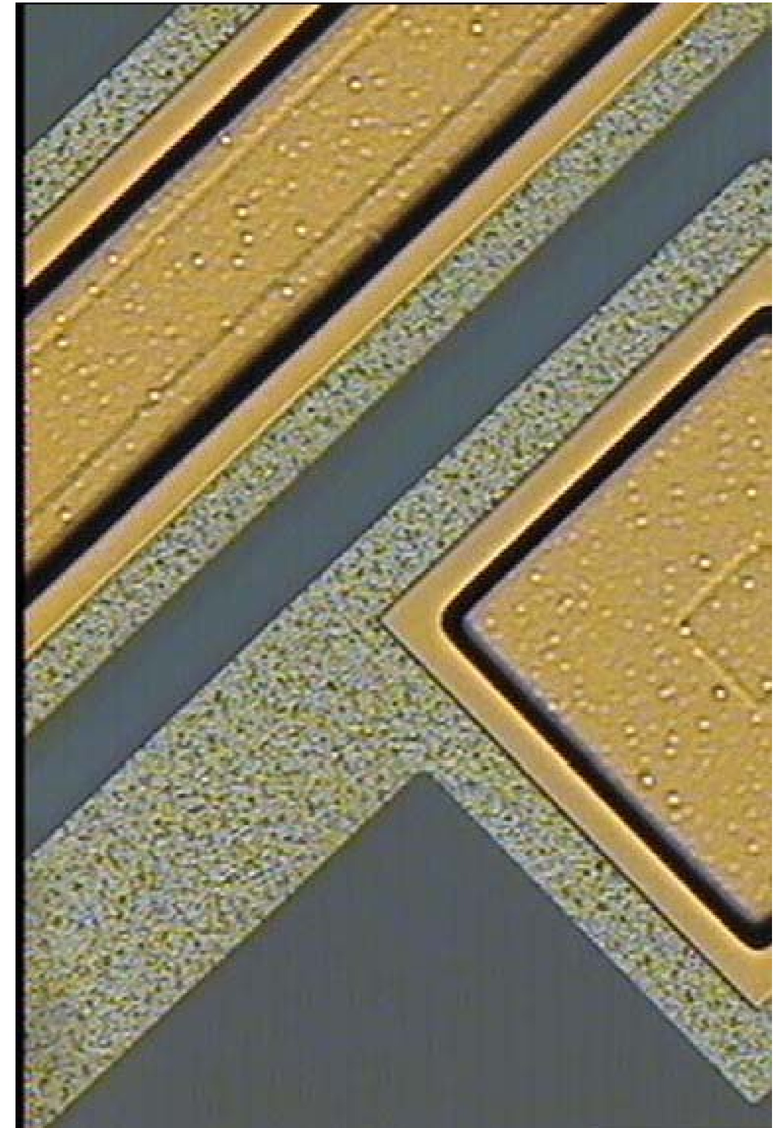
Diode Test wafers processed at IZM

- Preparation for SLID process
- Diffusion barriers & Cu layers
- Thermal treatment

Diode properties unchanged





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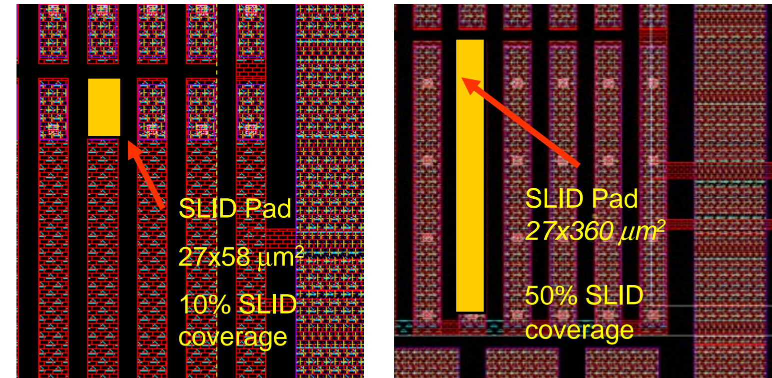
3rd Workshop on Advanced Silicon Radiation Detectors

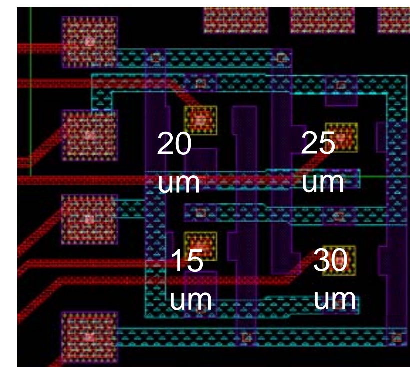
Barcelona
April 2008

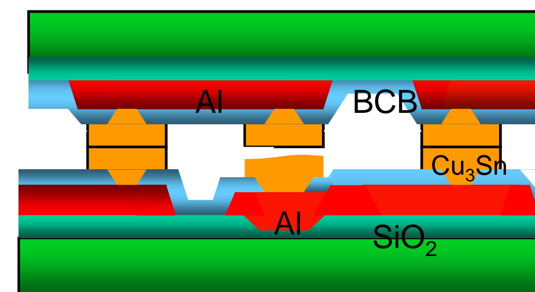
Tests on metal dummies at IZM

Test of "chip on wafer" SLID interconnection with metal dummies.

- Aim: determine the feasibility of the SLID inter-connection within the parameters we need for the ATLAS pixels.
- Test of the mechanical strength as a function of different area coverage by the SLID pads
- Test the SLID efficiency varying the dimensions of the SLID pads
- Study the SLID efficiency when degrading the planarity of the structure underneath the pads
- Determine the alignment precision between single "chip" and "detector" wafer
- Investigate the BCB isolation capability between the detector and chip surfaces







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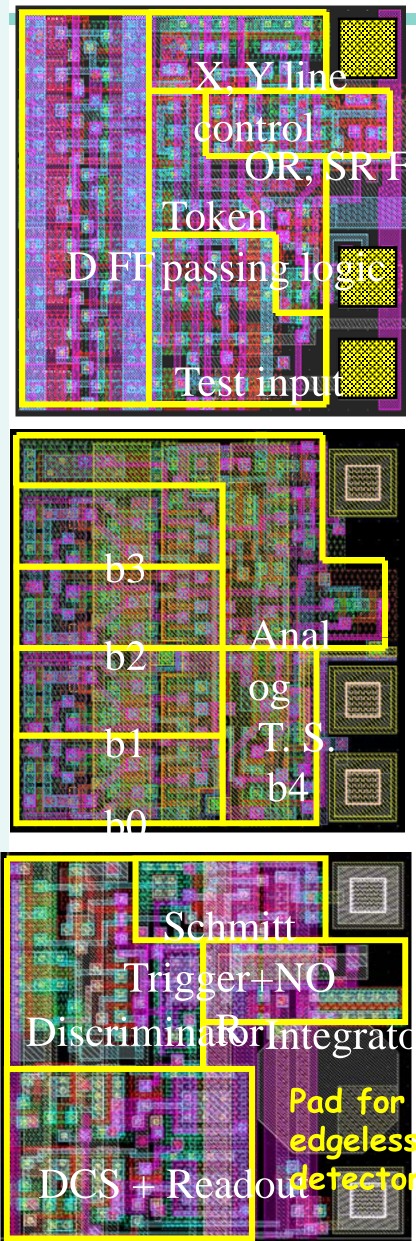
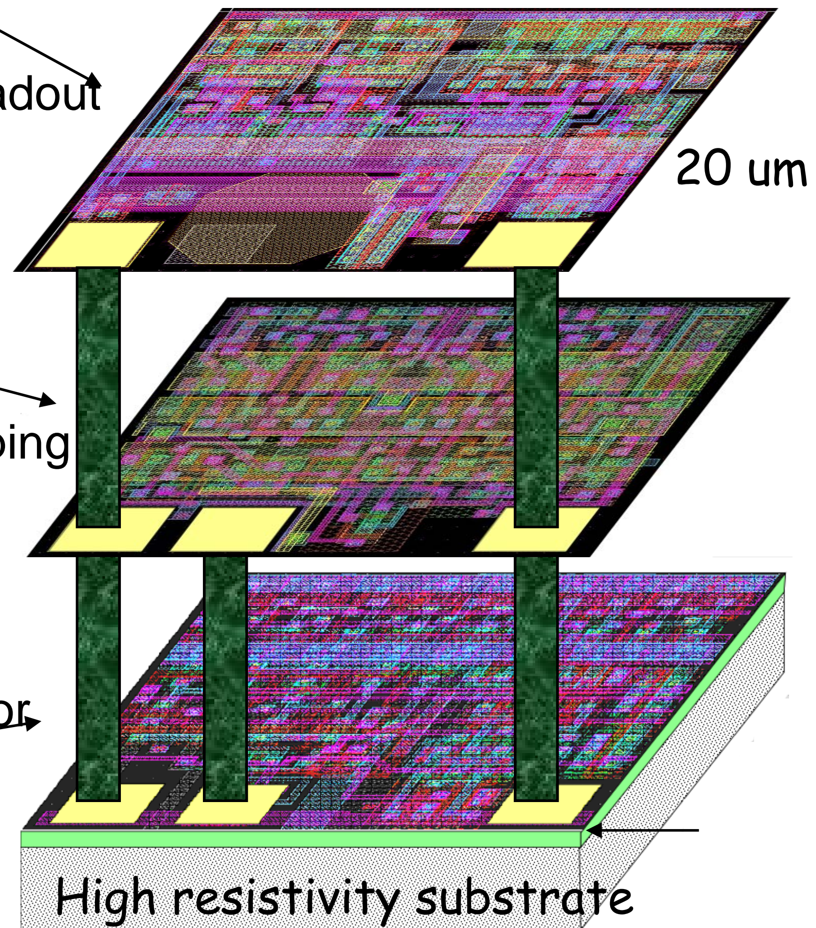
R&D at Fermilab (for ILC)



3 Tier readout chip for ILC – R. Yarema
Complex processing (time stamp)
Processed by MIT Lincoln Lab
No Sensor yet!



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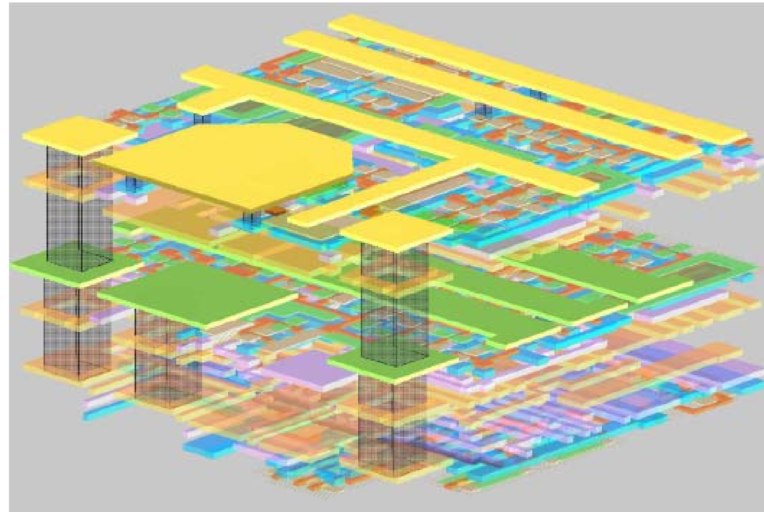
“sort of works” (or not ?)



- Trapped charge between tiers 2 and 3 during fabrication caused NMOS transistor thresholds to shift from 500 mv to 200 mv.
  - Attempts are being made by vendor to correct the problem after the fact with UV radiation
  - Backup lot being processed with different tier2-tier3 bonding conditions to remove threshold shift problem.
- ESD protection diodes are very leaky causing serious problems for circuits with analog inputs.
- Current mirrors used for biasing are not working properly - problem thought to be due to leakage path in the current mirror circuits.
- There are significant variation between chips resulting in low yields - reasons unknown at this time.
  - Testing will continue with parts from a different wafer

Only parts of the chip working
However: no problems with vias and interconnects

Conclusion: move to commercial supplier

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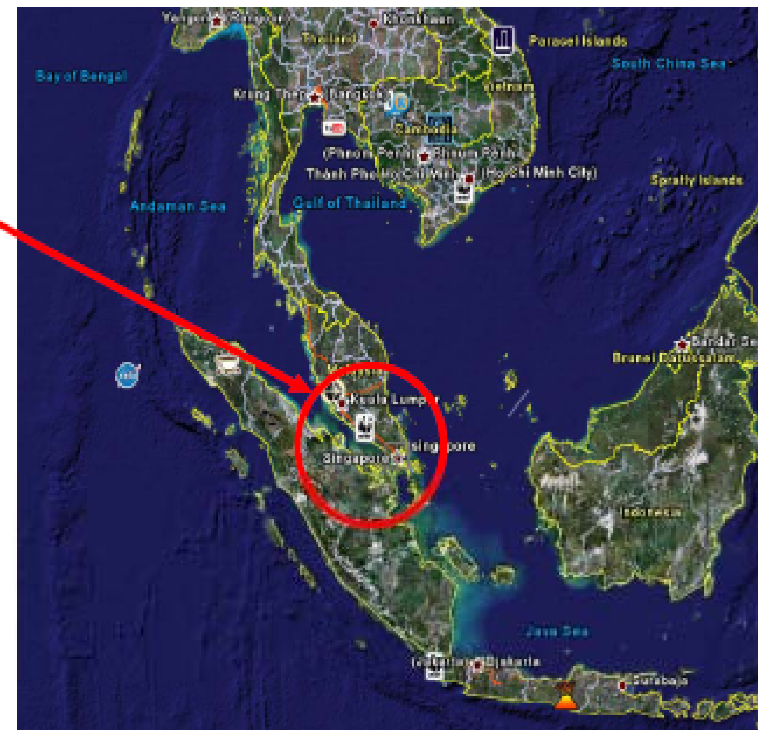
Commercial Vendor: Tezzaron

Tezzaron Background

- Founded in 2000, located in Naperville, Illinois
- Has fabricated a number of 3D chips for commercial customers
- Tezzaron uses the "Via First" process
- Wafers with "vias first" are made at Chartered Semiconductor in Singapore.
- Wafers are bonded in Singapore by Tezzaron.
  - Facility can handle up to 1000 wafers/month
- Bonded wafers are finished by Tezzaron
  - Bond pads
  - Bump bond pads
- Potential Advantages
  - Lower cost
  - Faster turn around
  - One stop shopping!!
- Process is available to customers from all countries



Ray Yarema, Ringberg, April 2006

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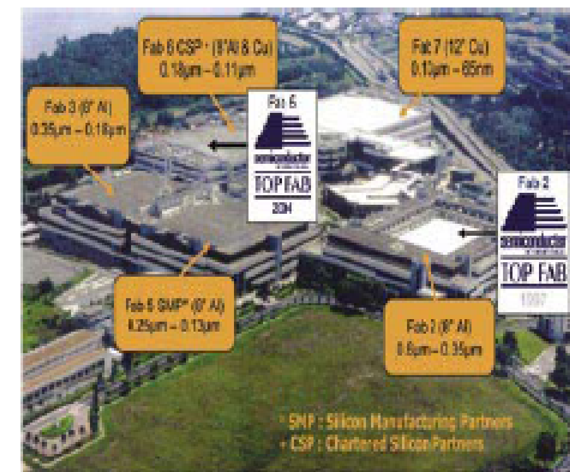
More Commercials…..

Chartered Semiconductor

- One of the world's top dedicated semiconductor foundries, located in Singapore, offering an extensive line of CMOS and SOI processes from 0.5 um down to 45 nm.
- Offers Common Chartered-IBM platform for processes at 90 nm and below.
- Chartered 0.13 um mixed signal CMOS process was chosen by Tezzaron for 3D integration
  - Chartered has made nearly 1,000,000 eight inch wafers in the 0.13um process
- Extension to 300mm wafers and 45nm TSVs underway
- Chartered 0.13 um process is similar to the IBM 0.13 um process but has different layer arrangement and transistor thresholds.
- Commercial tool support for Chartered Semiconductor
  - DRC – Calibre, Hercules, Diva, Assura
  - LVS - Calibre, Hercules, Diva, Assura
  - Simulation – HSPICE. Spectre, ELDO, ADS
  - Libraries – Synopys, ARM, Virage Logic



Chartered Campus

Ray Yarema, Ringberg, April 2006

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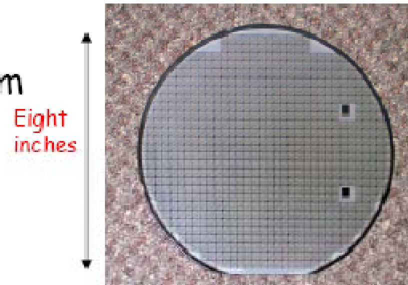
Tezzaron 3D Process

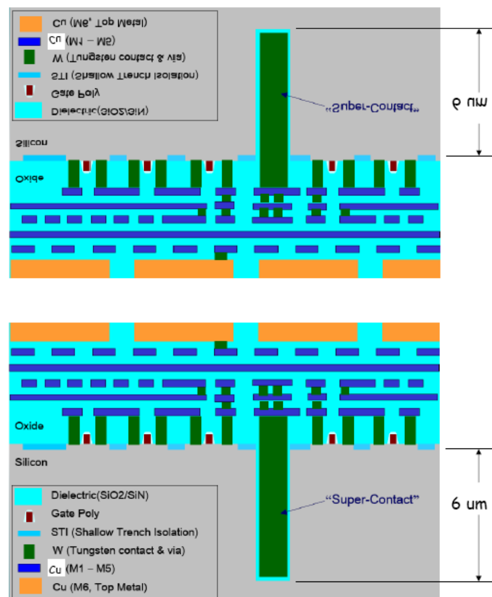
Chartered 0.13 um Process

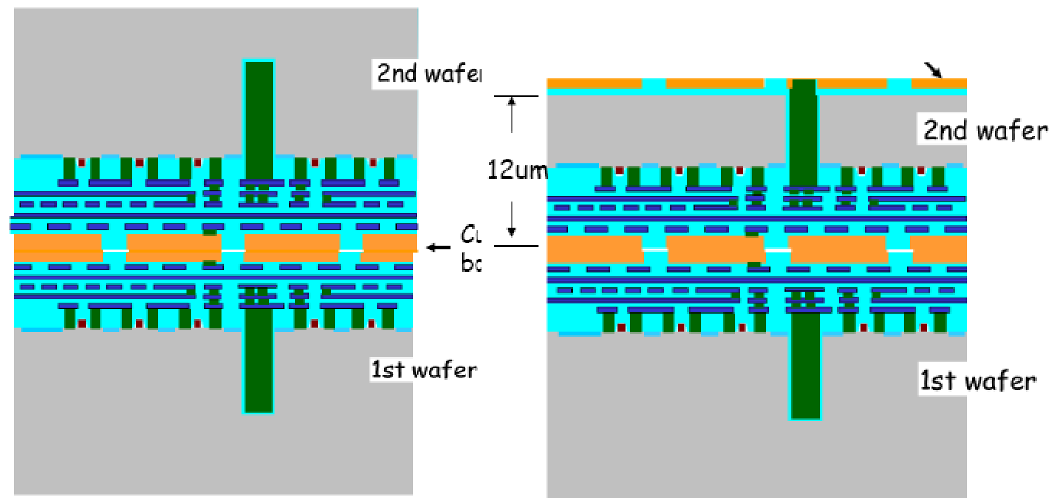
- 8 inch wafers
- Large reticule - 24 mm x 32 mm
- Features
  - Deep N-well
  - MiM capacitors - 1 fF/um²
  - Reticule size 24 x 32 mm
  - Single poly
  - 8 levels of metal
  - Zero Vt (Native NMOS) available
  - A variety of transistor options with multiple threshold voltages can be used simultaneously

Eight inches



Very small vias:
1.2 μm diameter
2.5 μm pitch
"vias first"





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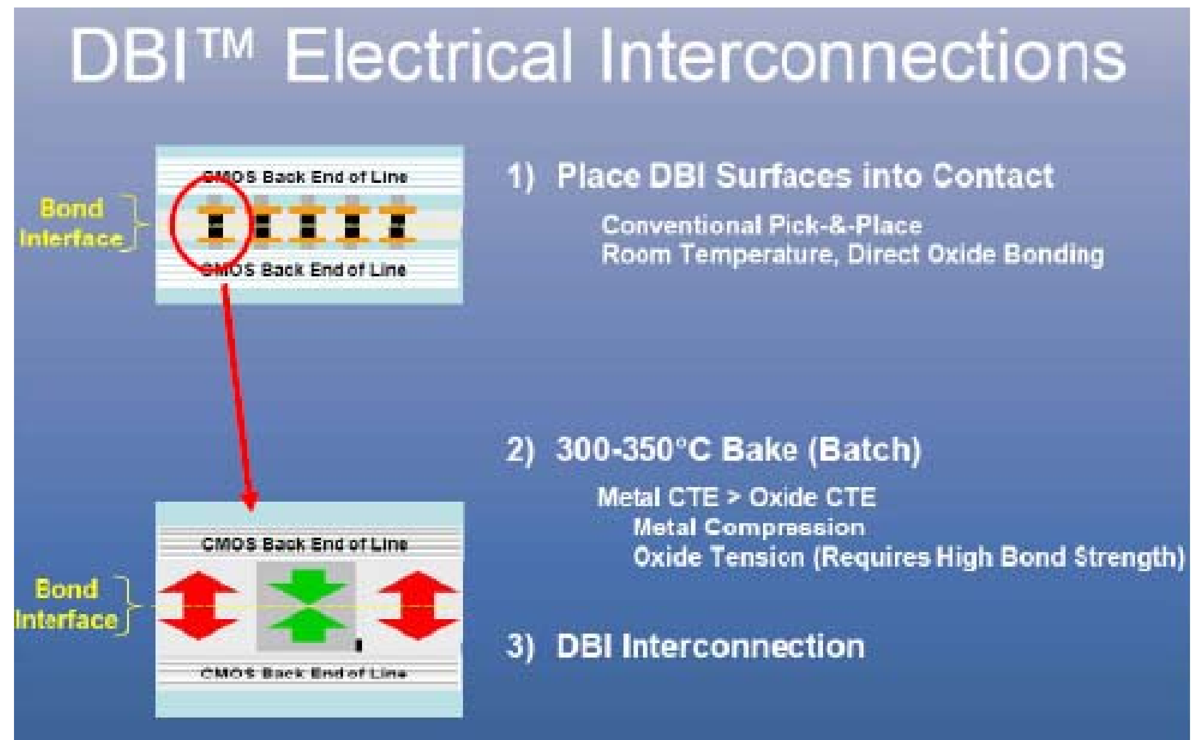
Ziptronix bond process



1) Wafer bonding (oxide-oxide bond like in SOI)
2) Thermocompression to fuse “magic” metal connection

Test: connect FPIX chips wit sensors
Ziptronix and Tezzaron formed an alliance

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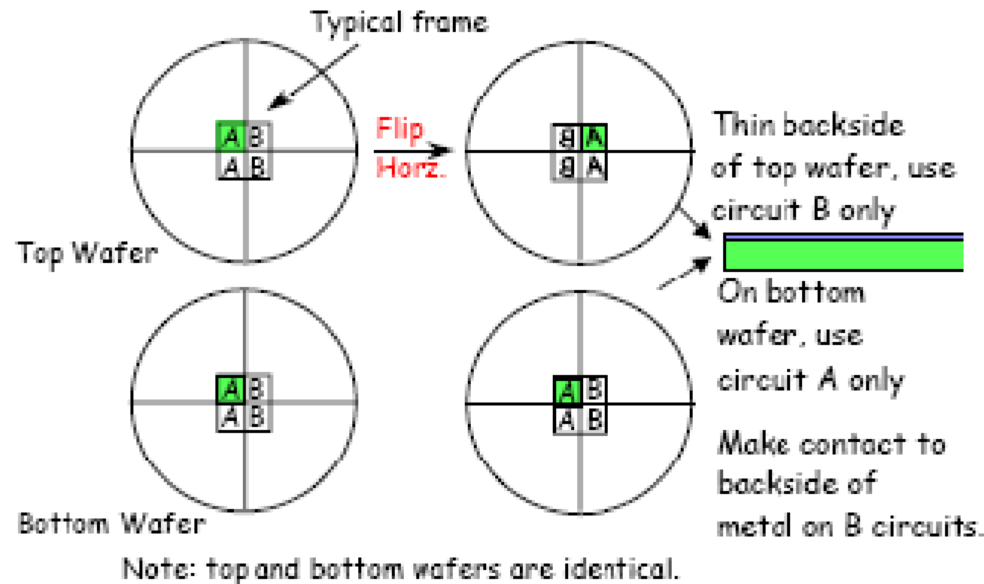
Fermilab project with Tezzaron



- Two tiers on one wafer (only one mask set needed)
- Face to face bonding brings two tiers together (1/2 reticul useful)
- Costs: 250 k$ for 12 wafers
- Sensor bonding: later with Ziptronix
- Fermilab invites other groups to join the MPW

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3D interconnection in the DevDET FP7 proposal

RECFA Coordination Group for Detector R&D in FP7 programmes

Combination of Collaborative Projects and Coordination and Support Actions for Integrating Activities

Capacities – Research Infrastructures

FP7-INFRASTRUCTURES-2008-1

Detector Development Infrastructures for Particle Physics Experiments

DevDet

Date of preparation: 29th February 2008
(Corrections dated 4th March 2008)

FP7-INFRASTRUCTURES-2008-1
INFRA-2008-1.1.1

Name of the coordinating person: Nigel Hessey
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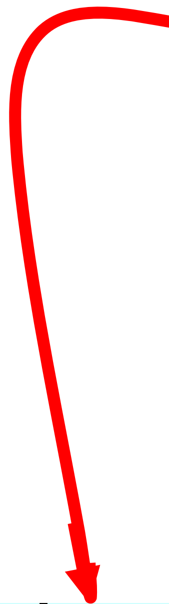
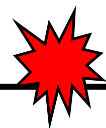
Workpackages

Work Package Number	Work PackageTitle
WP1	DevDet project management
WP2	Common software tools
WP4	Project office for Linear Collider detectors
WP5	Coordination office for long baseline neutrino experiments
WP6	Transnational access to CERN test beams and irradiation facilities
WP7	Transnational access to DESY test beam
WP8	Transnational access to European irradiation facilities
WP9	Construction of irradiation facilities at CERN
WP10	Test beam infrastructures for fully integrated detector tests
WP11	Detector prototype testing in test beams



3	COORD		Network for Microelectronic Technologies for High Energy Physics
		3.1	Microelectronics Technologies and enabling Tools
		3.2	Shareable IP blocks for HEP
		3.3	3D Interconnection of microelectronics and semiconductor detectors



Bonn, CERN, CNM, CNRS/IN2P3, INFN, Glasgow, Liverpool, MPI, RAL, Uppsala

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WP3 objectives

WP3 Network for Microelectronic Technologies for High Energy Physics

The main objective of this workpackage is to establish a network of groups working collaboratively on advanced semiconductor technologies and high density interconnections in High Energy Physics.

Task 3 3D Interconnection of microelectronics and semiconductor detectors

- Demonstration of the feasibility of high density 3D interconnection for applications in Particle Physics (mainly for sensor-electronics interconnection).
- Subdivision of the final objectives into a set of well defined sub-tasks:
  - Design of and production of dedicated ASIC and sensors
  - Preparation of wafer thinning and via etching.
  - Development of high density interconnection technology with direct chip-chip contact by different techniques

A primary objective is to organize MPW runs with access to full wafers:

: many process steps need complete wafers
postprocessing of ASICs
barrier layers, metal layers
even chip-to-wafer needs such processing

single chips form MPW cannot be used!

Proposal:
Organize common MPW runs of 3D-community
Possible if organized by CERN (has happened before)

Final goal: 3D demonstrator with sensor and 2-tier ASIC

Summary

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3D interconnection offers a solution for highly integrated, complex, high performance pixel detectors

-Could be used with many sensor types (planar, 3D, DEPFET,………)

-Can combine different ASIC technologies

-Backside-connection of 4-side abuttable chips

-Thinning of ASICs is basic ingredient -> low mass!

-R&D driven by industry -> potentially cost effective solutions

-Several HEP groups started to develop 3D-IT (Fermilab, MPI, IN2P3)

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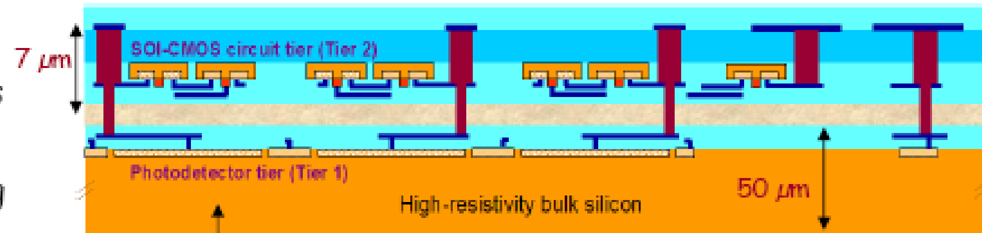
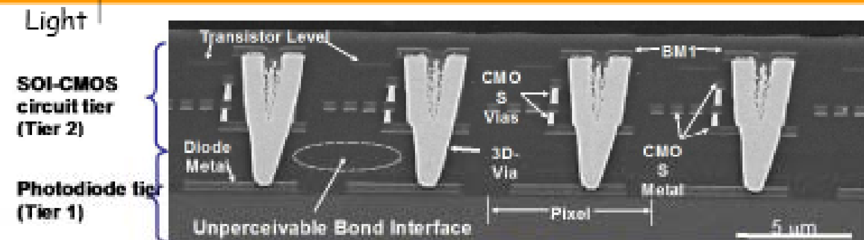
R&D at MIT Lincoln Lab

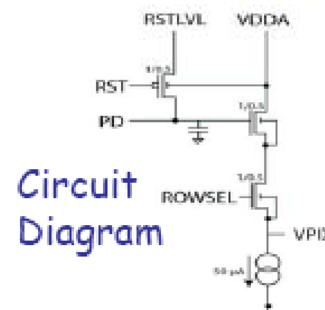
3D Megapixel CMOS Image Sensor

- 1024 x 1024, 8 μm pixels
- 2 tiers
- Wafer to wafer stacking (150 mm to 150 mm)
- 100% diode fill factor
- Tier 1 - p⁺n diodes in >3000 ohm-cm, n-type sub, 50 μm thick
- Tier 2 – 0.35 um SOI CMOS, 7 μm thick
- 2 μm square vias, dry etch, Ti/TiN liner with W plugs
- Oxide-oxide bonding
- 1 million 3D vias
- Pixel operability >99.999%
- 4 side abuttable array





Drawing and SEM Cross section



Circuit Diagram

Image

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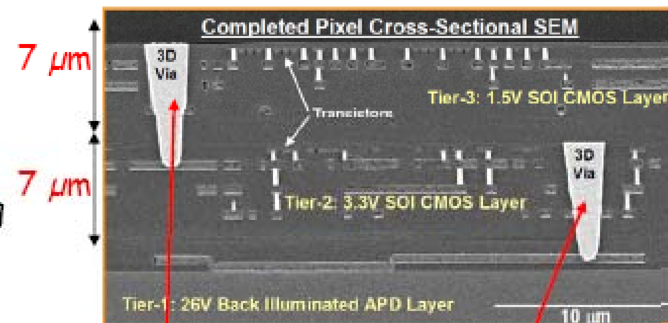
R&D at MIT Lincoln Lab

3D Laser Radar Imager

- 64 x 64 array, 30 μm pixels
- 3 tiers
  - 0.18μm SOI
  - 0.35 μm SOI
  - High resistivity substrate diodes
- Oxide to oxide wafer bonding
- 1.5 μm vias, dry etch
- Six 3D vias per pixel

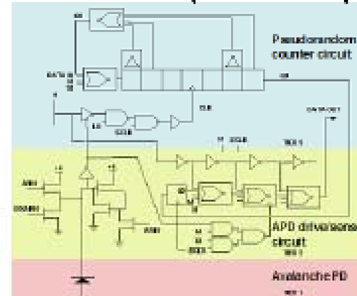
7 μm

7 μm



SEM Cross section

VISA APD Pixel Circuit (~250 transistors/pixel)

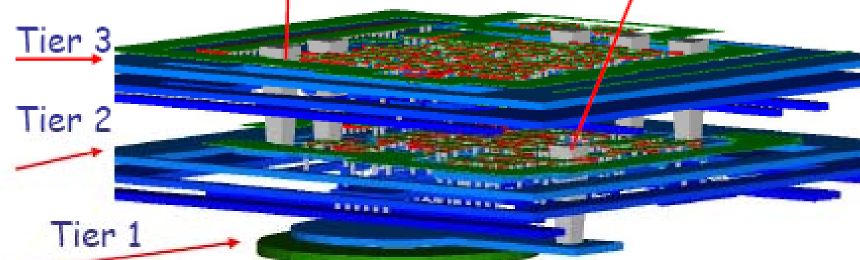


Schematic

Tier 3

Tier 2

Tier 1



CAD Drawing

May 2006 ILC VTX Workshop at Ringberg 20

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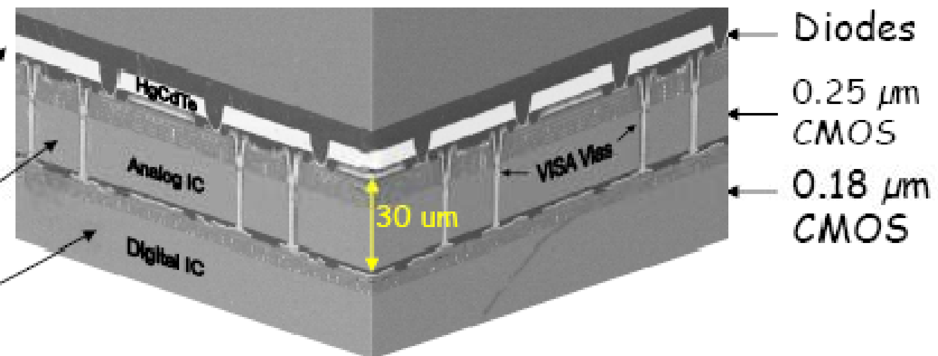
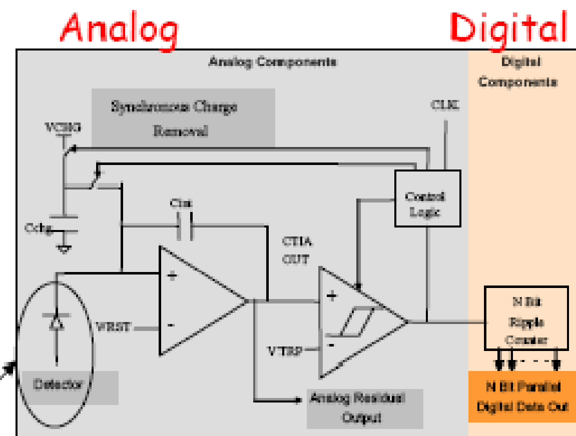
R&D at MIT Lincoln Lab

3D Infrared Focal Plane Array

- 256 x 256 array with 30 µm pixels
- 3 Tiers
  - HgCdTe (sensor)
  - 0.25 µm CMOS (analog)
  - 0.18 µm CMOS (digital)
- Die to wafer stacking
- Polymer adhesive bonding
- Bosch process vias (4 µm) with insulated side walls
- 99.98% good pixels
- High diode fill factor



Array cross section



3 Tier circuit diagram

Infrared image