Development of Monolithic Silicon Detectors based on OKI SOI CMOS Technology

Y. Unno (KEK)

for

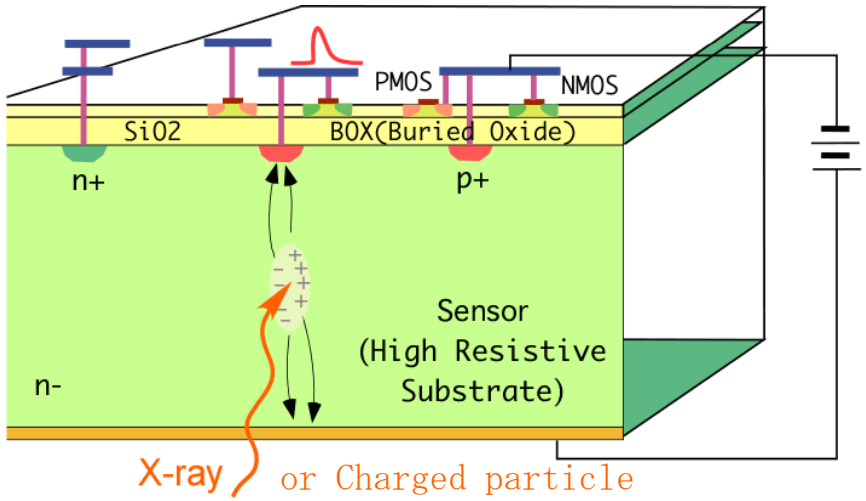
SOIPIX collaboration

(KEK,Univ. Tsukuba, Tokyo Inst. Tech., Osaka Univ., JAXA/ISAS, Kyoto Univ., JASRI, Univ. Hawaii, SLAC, LBNL, Fermilab)

Y. Unno, 3rd Workshop on Advanced Radiation Detectors, Barcelona, Spain, 14-16 April, 2008

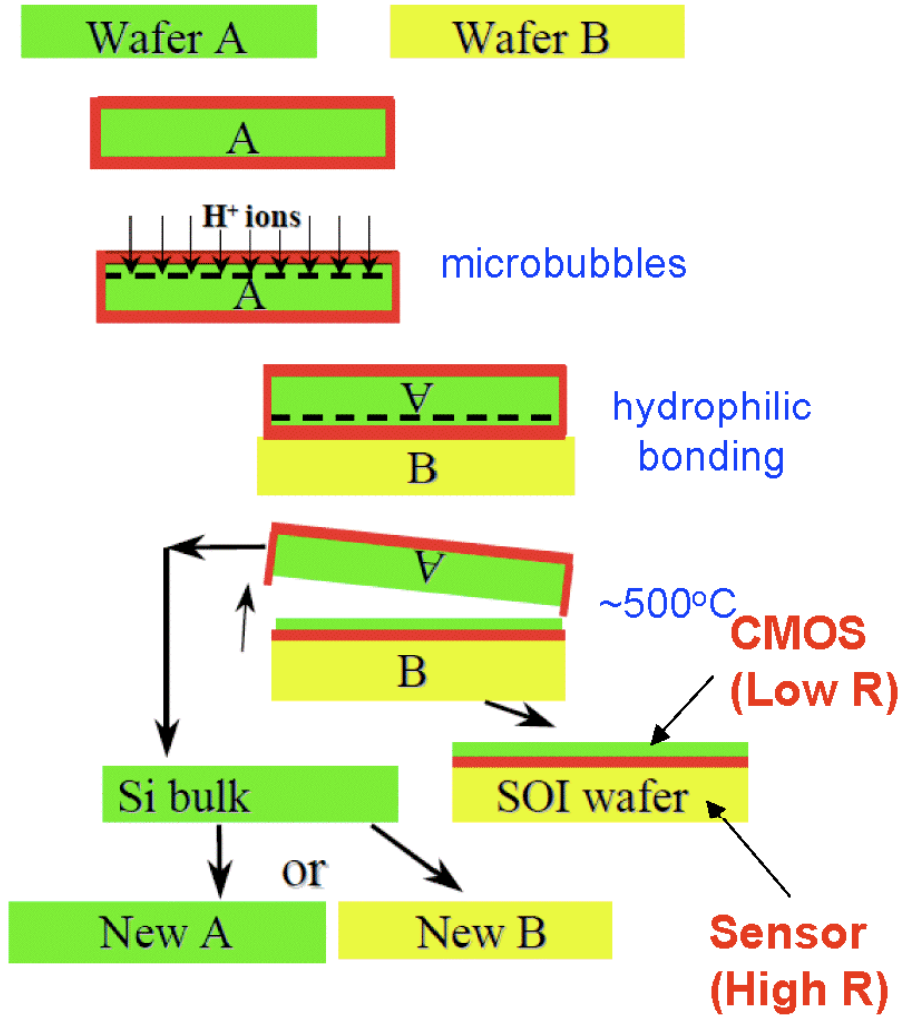
SOI Monolithic Pixel Detector

- SOI wafer
  - Two types of silicon wafers bonded with buried oxide layer (BOX)
  - SOI layer - CMOS electronics with low resistivity silicon
  - Handle wafer - Active radiation sensor with high resistivity silicon
- OKI SOI (FD)CMOS technology
  - Fully Depletion (FD) type for low power, high speed, less latch-up
  - Industrial CMOS technology
- Monolithic detector
  - No bump bonding
  - Less material, Higher reliability, ...



SOI Wafer (UNIBOND™, SOITEC)

1. Initial silicon wafers A & B
2. Oxidation of wafer A to create insulating layer
3. Smart Cut ion implantation induces formation of an in-depth weakened layer
4. Cleaning & bonding wafer A to the handle substrate, wafer B
5. Smart Cut - cleavage at the mean ion penetration depth splits off wafer A
6. Wafer B undergoes annealing, CMP and touch polish => SOI wafer complete
8. Split-off wafer A is recycled, becoming the new wafer A or B

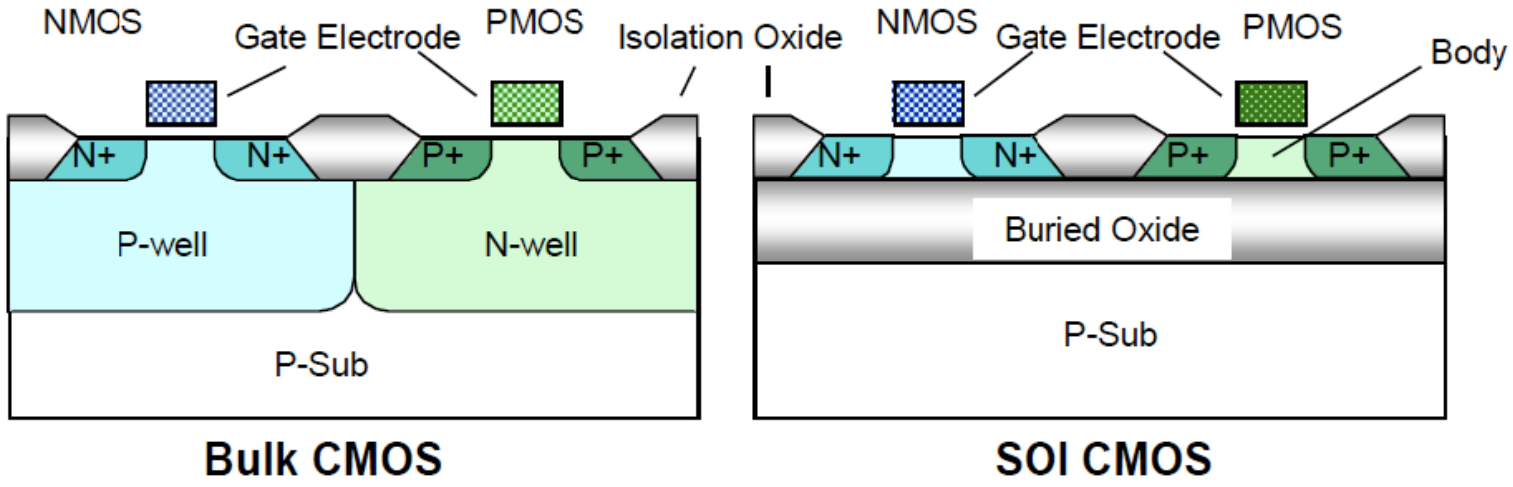


- Vendor does not assure the type of handle wafer

SOI CMOS Technology

- SOI (vs. Bulk)
- Full dielectric isolation
  - Latchup free, Small area
- Low junction capacitance
  - High speed, Low power
- No Well, thin Si film
  - Low leakage, Low Vt shift
- Small active volume
  - Low soft error for radiation

- FD-SOI
  - FD: Fully Depleted
  - Less floating body effect
  - Near ideal sub-threshold slope
  - Low operating power
  - Ultra-low stand-by power

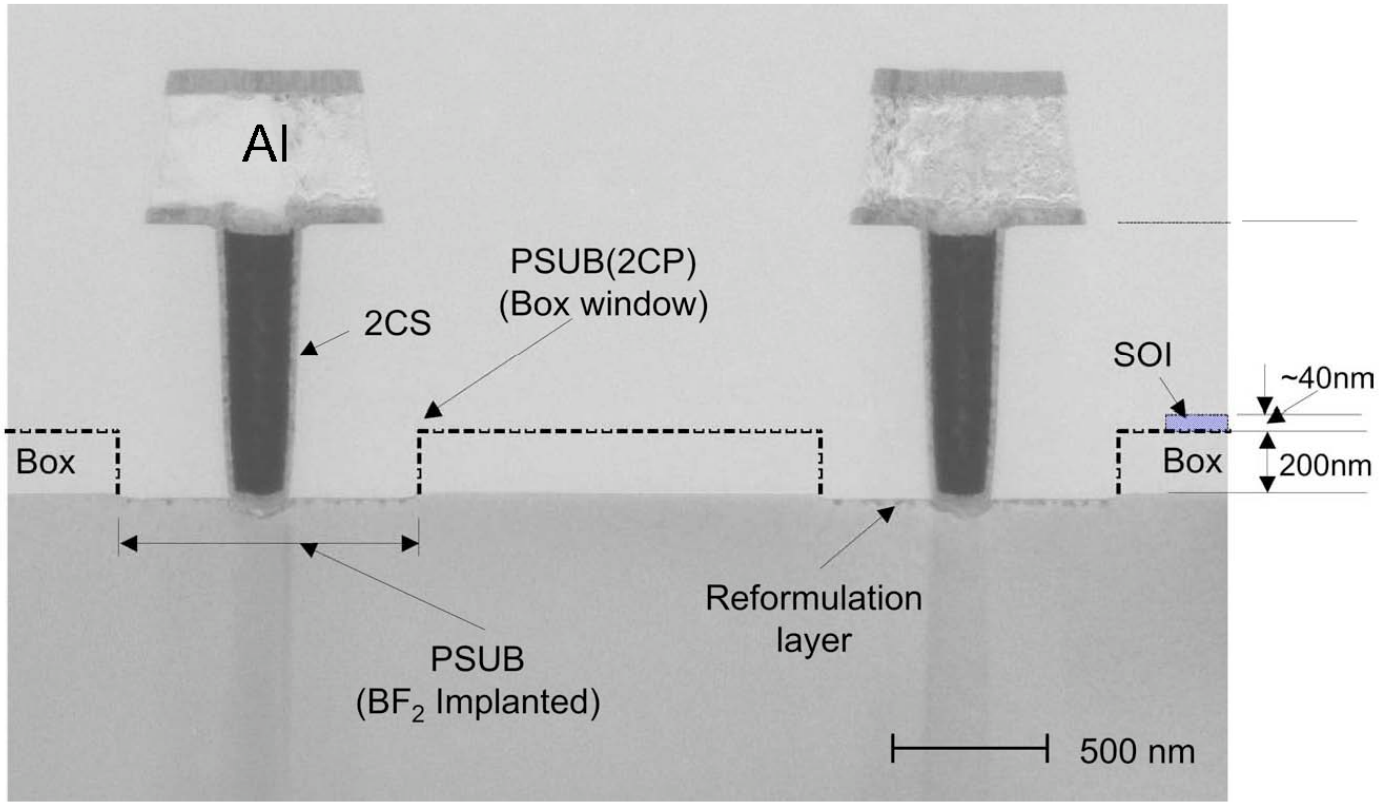


Y. Unno, 3rd Workshop on Advanced Radiation Detectors, Barcelona, Spain, 14-16 April, 2008

Development History

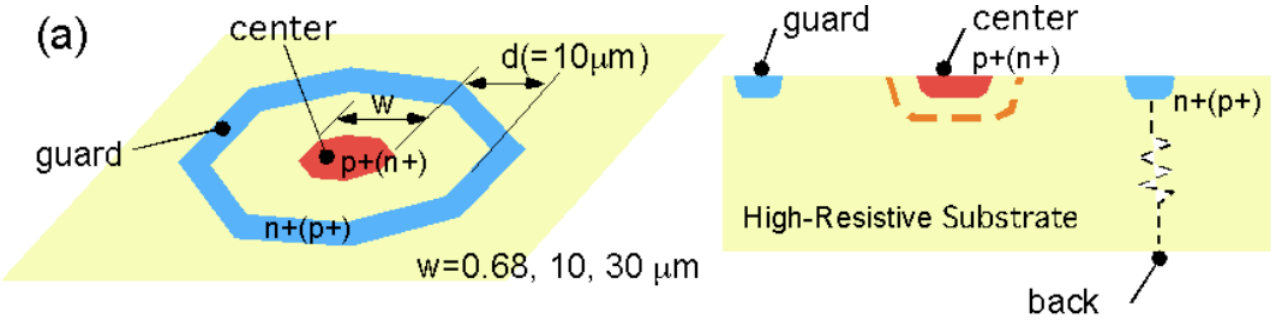
- 2005.07 - Start collaboration with OKI
- 2005.10 - Univ. Tokyo VDEC/OKI 0.15 μm MPW run
- 2006.03 - 1st Pixel chips
  - Confirmed sensitivity for light and beta-ray
- 2006.12 - KEK's MPW run (FY06), with 17 designs domestic and abroad
- 2007.04 - Closure of 0.15 μm line
  - This 0.15 μm process was Lab-based
- 2007.06 - Transfer to OKI Miyagi 0.20 μm production line
- 2008.01 - 2nd KEK's MPW run (FY08) in 0.20 μm line

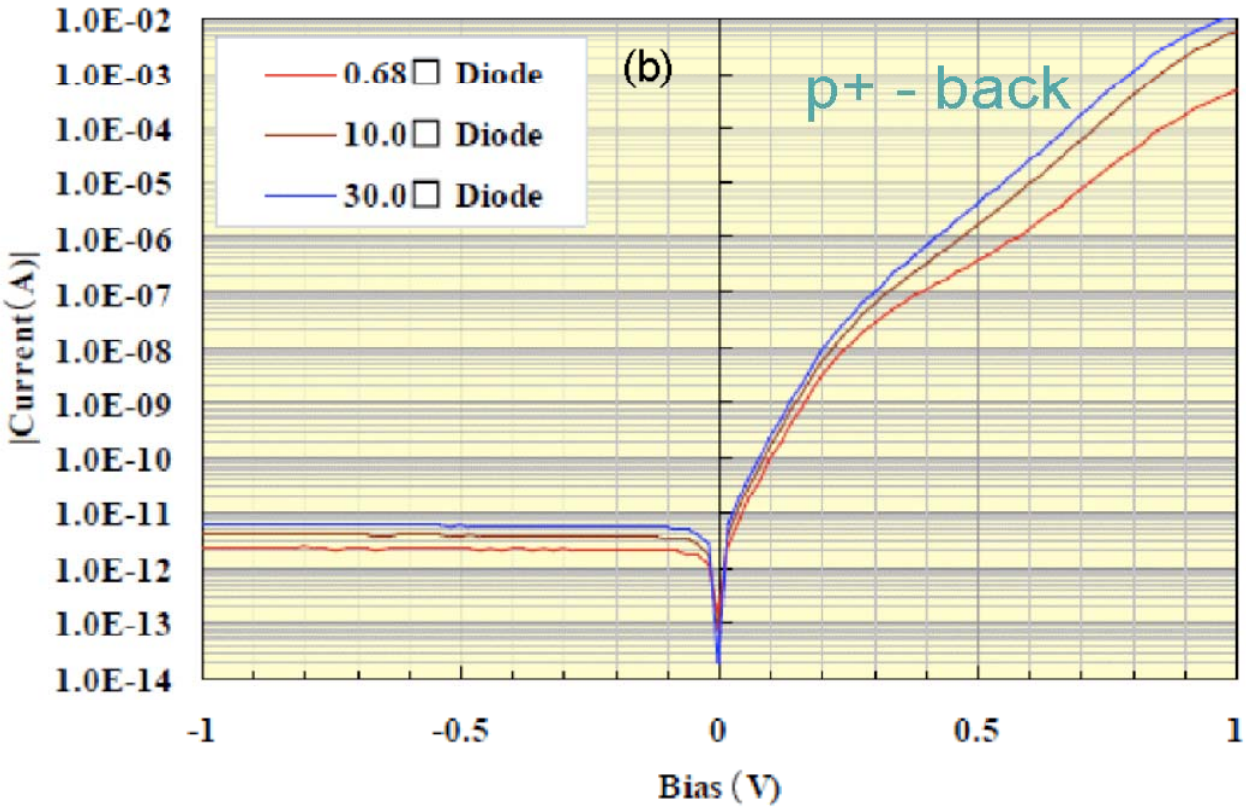
SOI Monolithic Detector Technology



- Handle wafer contact etched through BOX layer

p-n Junction I-V Characteristics



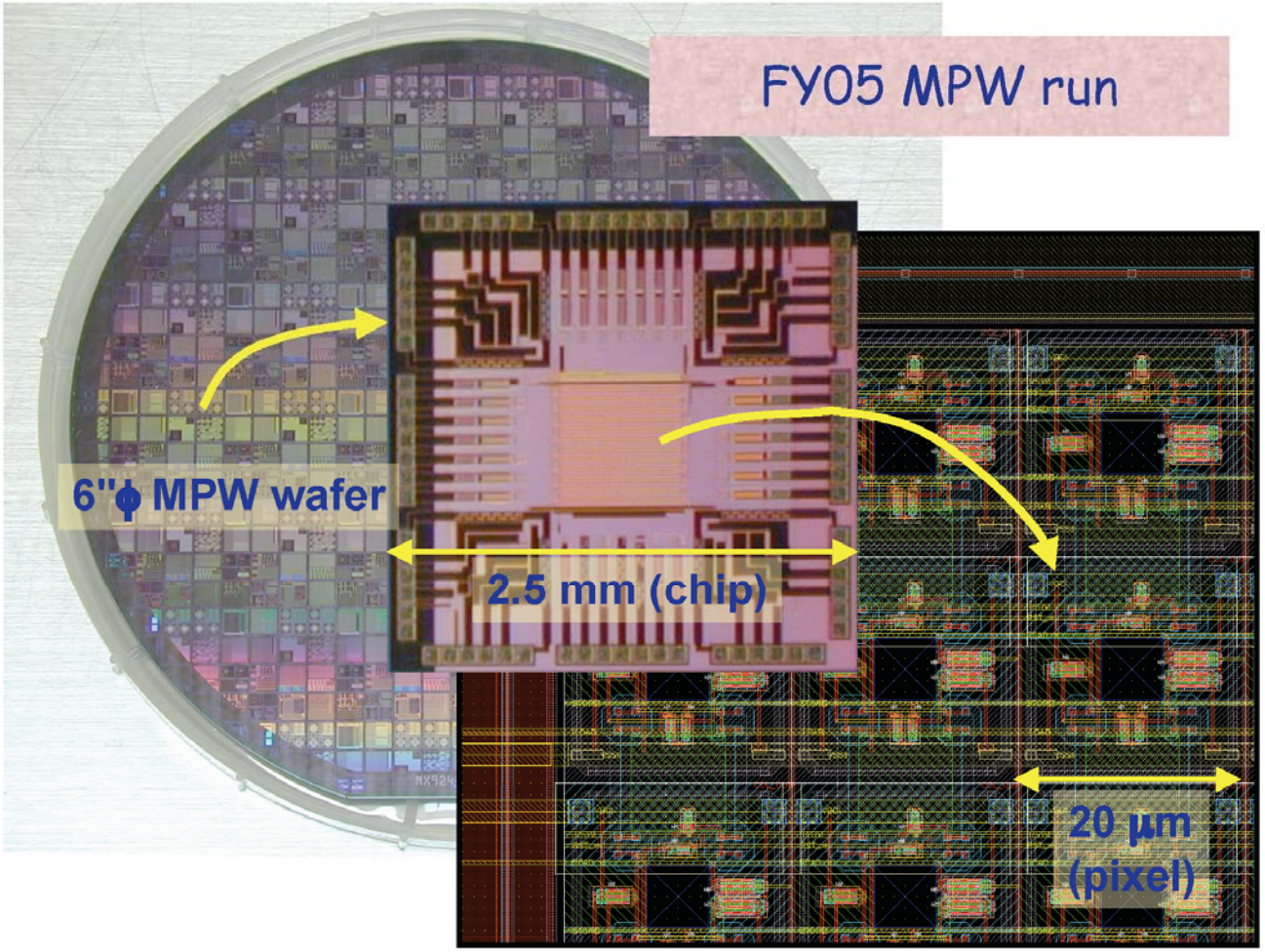


Good diode

Substrate is n-type

Y. Unno, 3rd Workshop on Advanced Radiation Detectors, Barcelona, Spain, 14-16 April, 2008

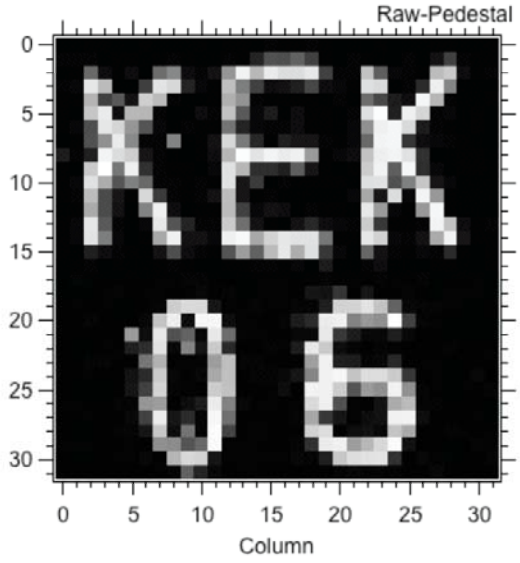
FY05 MPW run



CMOS Active Pixel Sensor Type

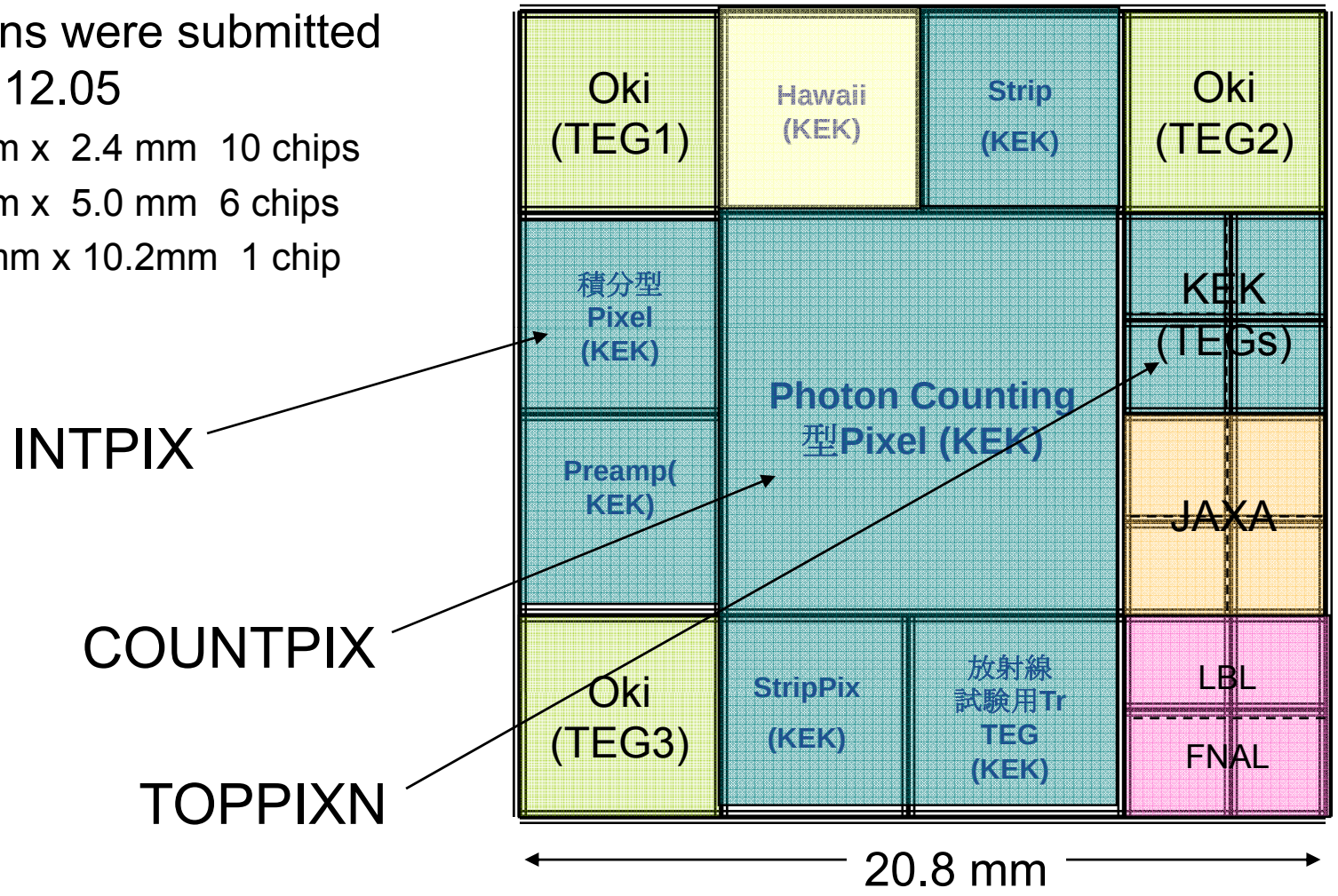
20 μm x 20 μm

32 x 32 pixels



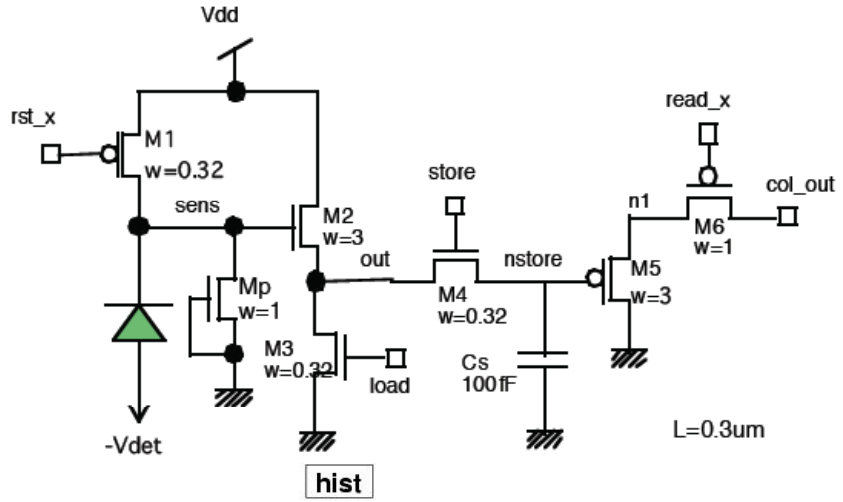
FY06 MPW run

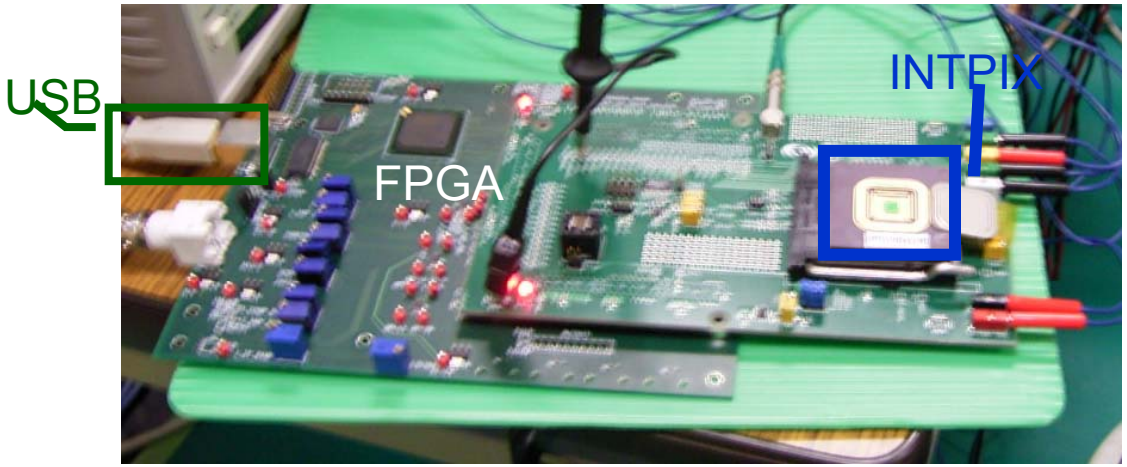
- 17 designs were submitted on 2006.12.05
  - 2.4 mm x 2.4 mm 10 chips
  - 5.0 mm x 5.0 mm 6 chips
  - 10.2 mm x 10.2mm 1 chip



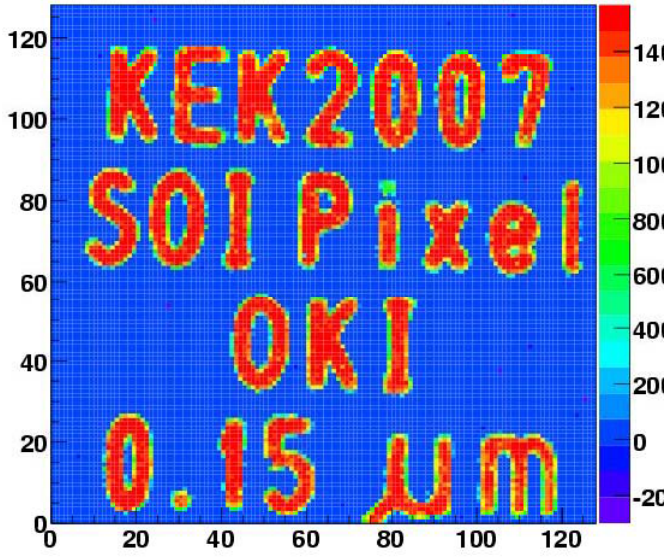
INTPIX

- Integrating type
  - 5 mm x 5 mm
  - 20 μm x 20 μm/pixel
  - 128 x 128 pixels



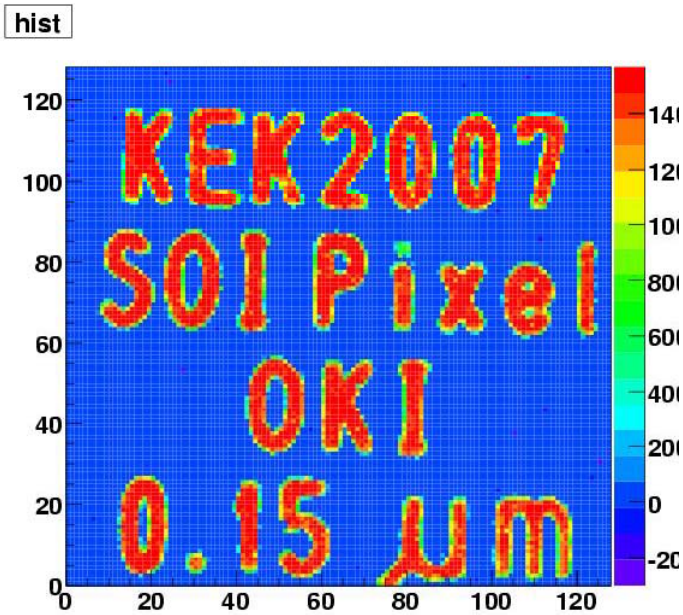


COB I/F for USB (Univ. Hawaii)



INTPIX (Cont'd)

- The movie
  - White light
  - Bias voltage: 10 V
    - Depletion ~40 μm
    - Back gate effect limit
  - DAQ
    - 128x8=1024 pixels
    - ~0.02 sec
    - 16 readouts/frame
- Others
  - Beta-ray
  - Beamtest



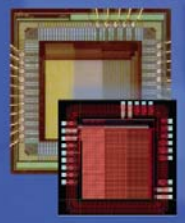
Move, Intensity, ...

Monolithic Pixel Sensor R&D at LBNL

Chip Design: P. Denes

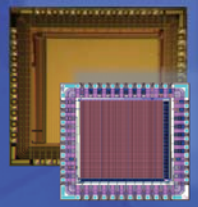
Analog Pixel Architecture

- Charge Interpolation [$\sigma \sim a/(S/N)$]
- In-pixel CDS & On-chip Digitisation
- Fast Readout

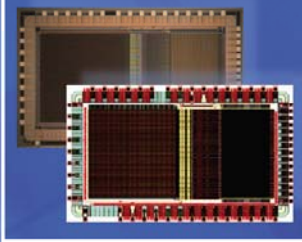


AMS 0.35μm-OPTO

LDRD-1 (2005):
10, 20, 40μm pixels



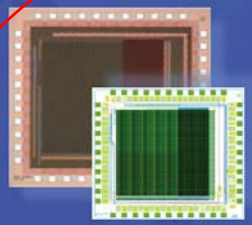
LDRD-2 (2006):
20μm pixels,
in-pixel CDS
3T and SB pixels



LDRD-3 (2007):
20μm pixels,
in-pixel CDS
on-chip 5-bit ADCs

Binary Pixel Architecture

- Small Pixels [$\sigma = \text{pitch}/\sqrt{12}$]
- In-pixel Discr. & Time Stamping
- In-situ Charge Storage



OKI 0.15μm FD-SOI

LDRD-SOI-1 (2007):
10μm pixels,
analog & binary pixels

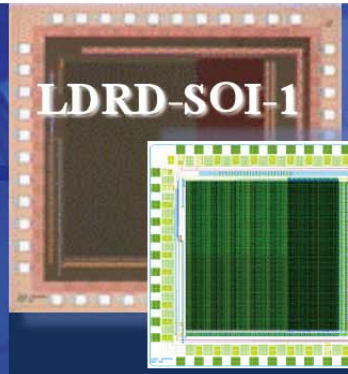
OKI 0.20μm FD-SOI

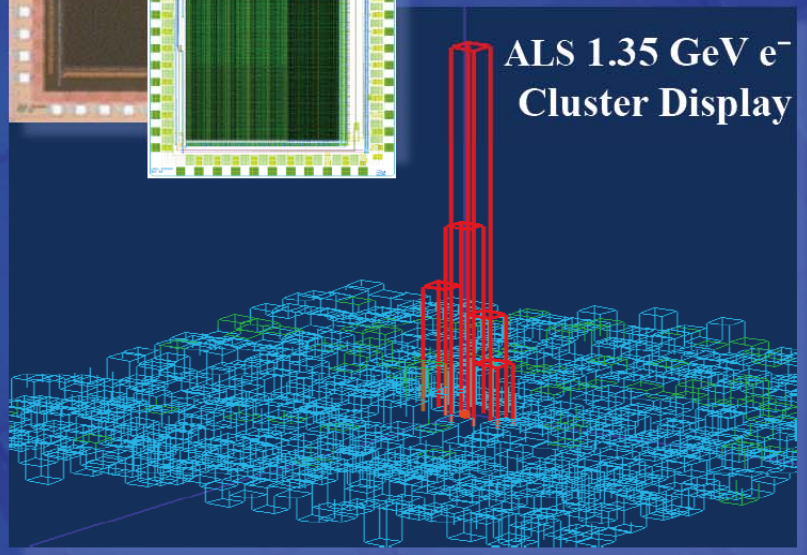
LDRD-SOI-2 (2008):
10-15μm pixels,
analog & binary pixels

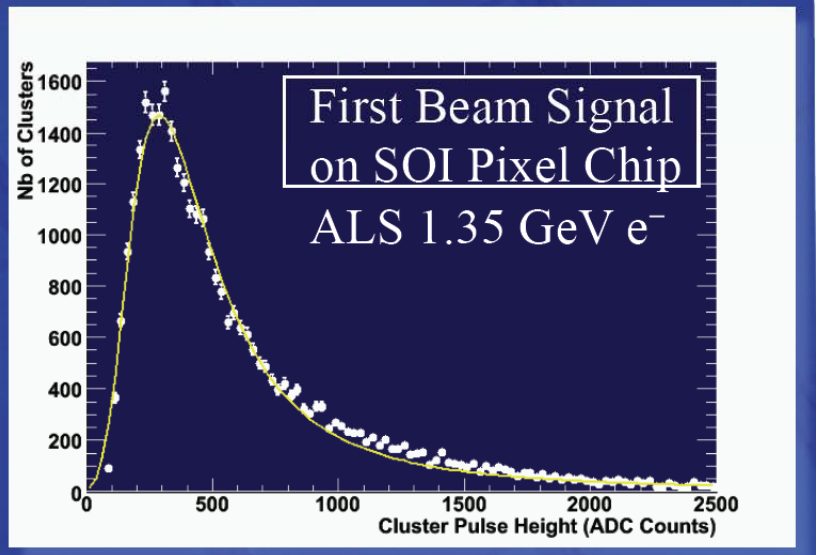
• • •

LAWRENCE BERKELEY NATIONAL LABORATORY

LDRD-SOI-1 Analog Pixels: Beam Test







V_d (V)	Clusters/Evt w/ beam	Clusters/Evt w/o beam	<Nb Pixels>	Signal MPV (ADC)	S/N
1	9.7	0.05	3.31	132	8.9
5	14.0	0.12	3.39	242	14.9
10	7.8	0.20	3.31	316	15.0
15	3.9	0.01	2.45	301	13.6

to appear in NIM A (2007)

LAWRENCE BERKELEY NATIONAL LABORATORY

MAMBO - Monolithic Active pixel Matrix wit Binary cOunters in SOI Technology OKI 0.15µm

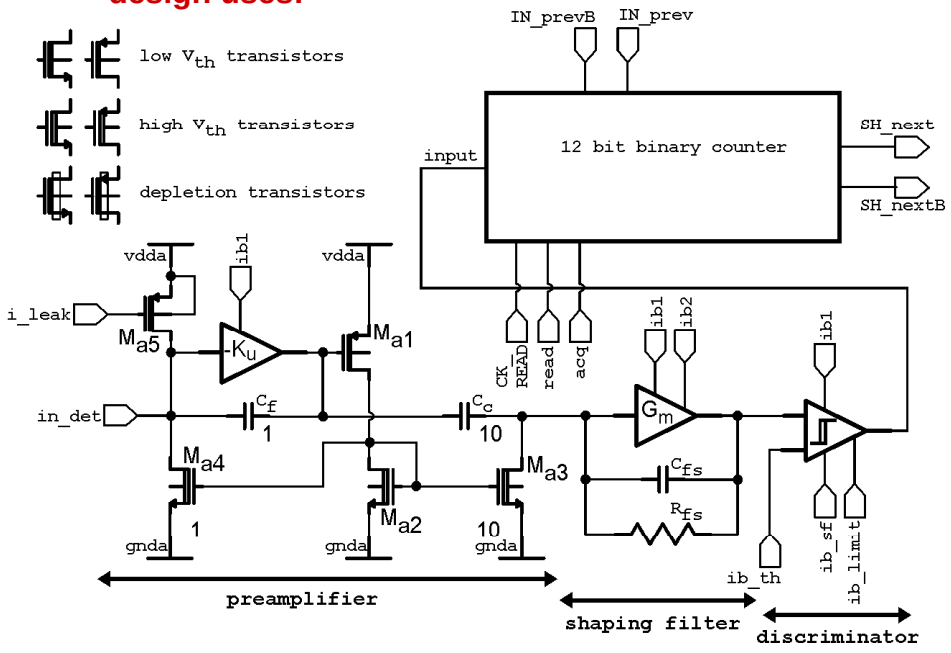
Fermilab

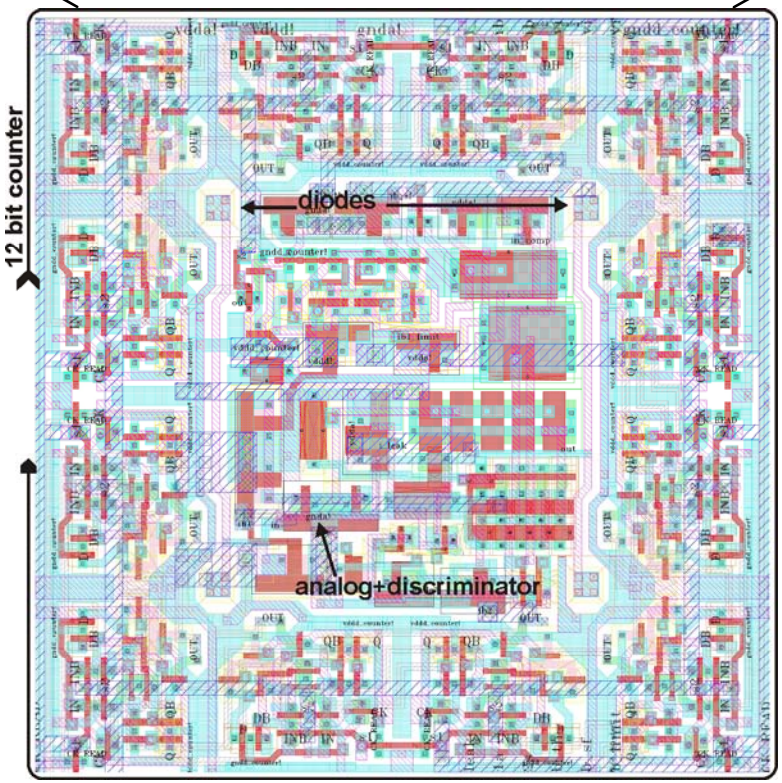
- **applications**
  - imaging detector for direct detection in electron microscopy (TEM), and soft X-rays,

design:

- test prototype 64x64 pixels, pitch 26µm, 4 parallel diodes /pixel (distance ~13µm),
- each pixel: CSA, CR-RC^2 shaper, discriminator + 12 bit binary counter,
- counter reconfigurable to shift register – readout serial (caterpillar) through all pixels,
- peripheral circuitry limited to digital drivers (RO clock distribution, I/O signals, configuration switch) and bias generator

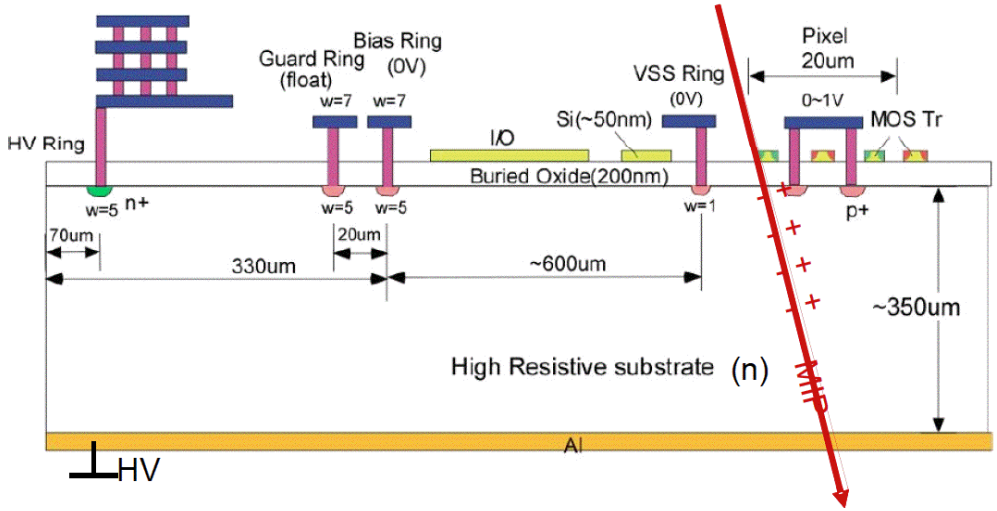
- **pixel:**
  - design uses:





CAP5 .15 µm SOI

Univ. Hawaii

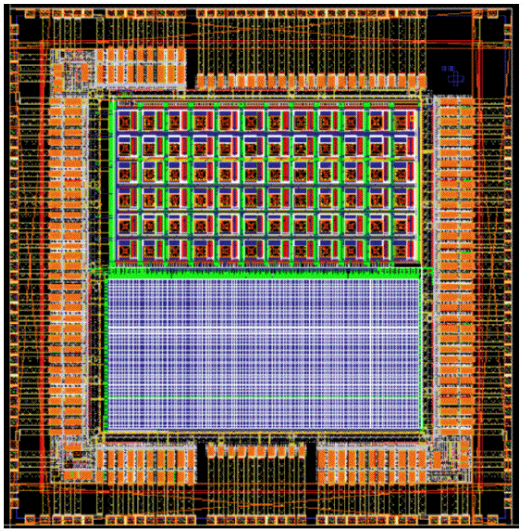


SOI advantages

- possibility to deplete substrate: higher signal
- charge transport: drift in E-field; faster; less spreading
- 100% fill factor: no loss of charge on parasitic structures
- no latch up
- radiation hard
- no bump-bonding, low collection electrode capacitance
- low power

Potential problems:

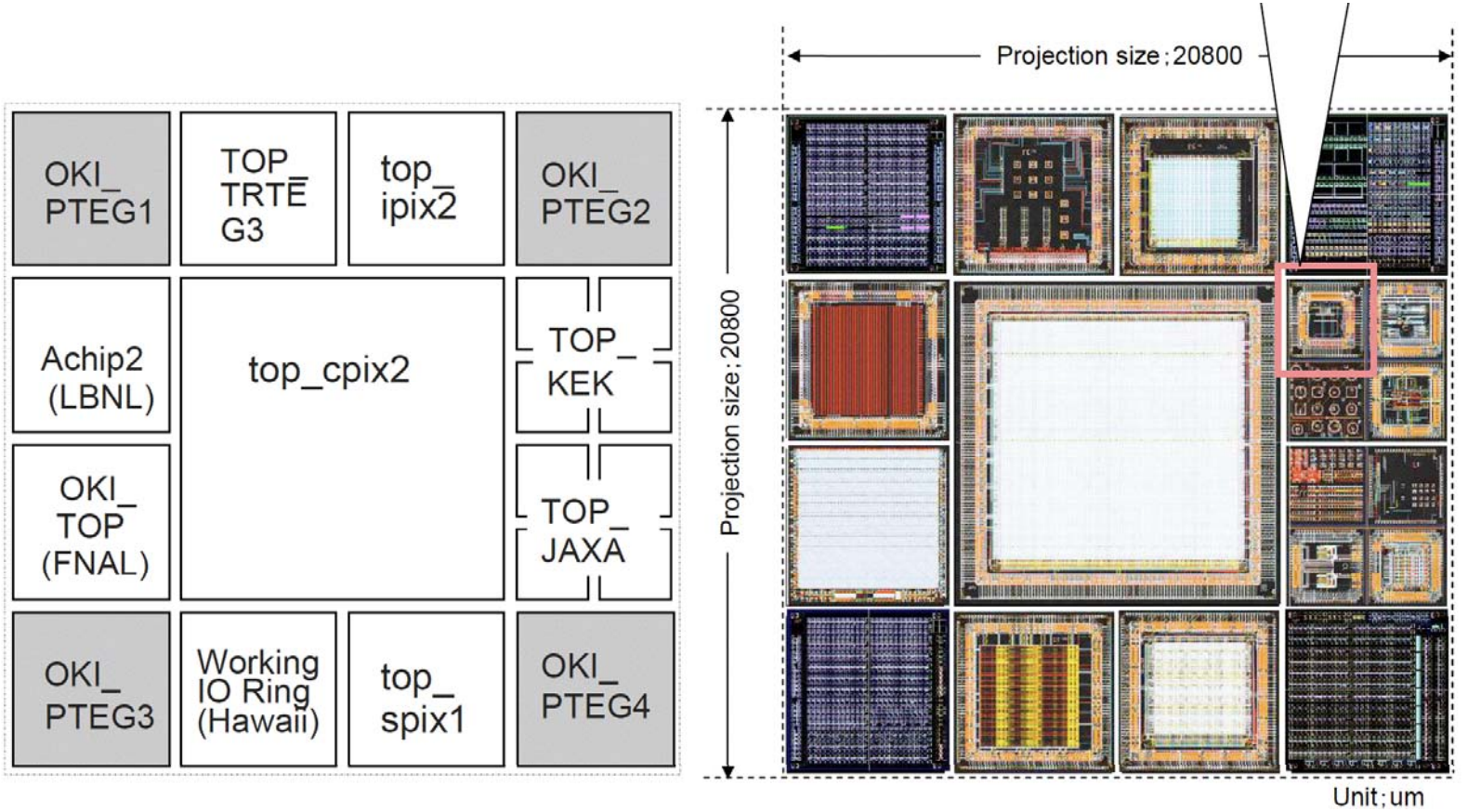
- back gate effect due to HV – limitation do depletion
- BOX can charge up under irradiation: back gate effect?
- charge injection from CMOS layer?



CAP5: binary design identical to CAP4

pixel matrix: 44 rows 108 columns
pixel size: 28.7 x 32.5 mm^2

FY07 MPW run



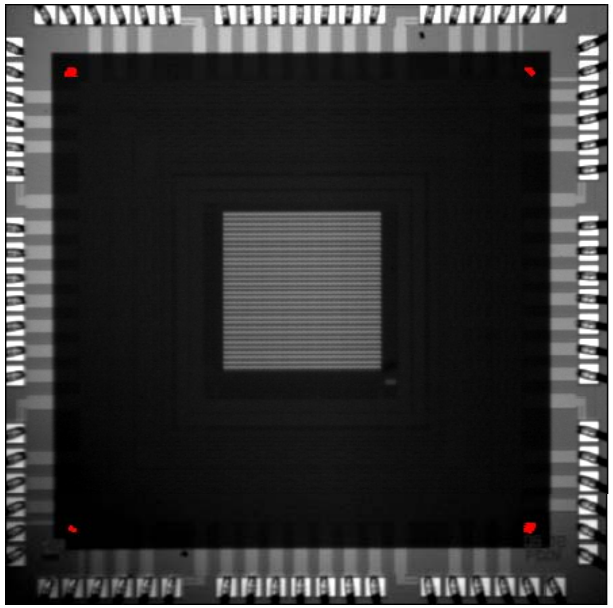
- 2008.01.15 submitted

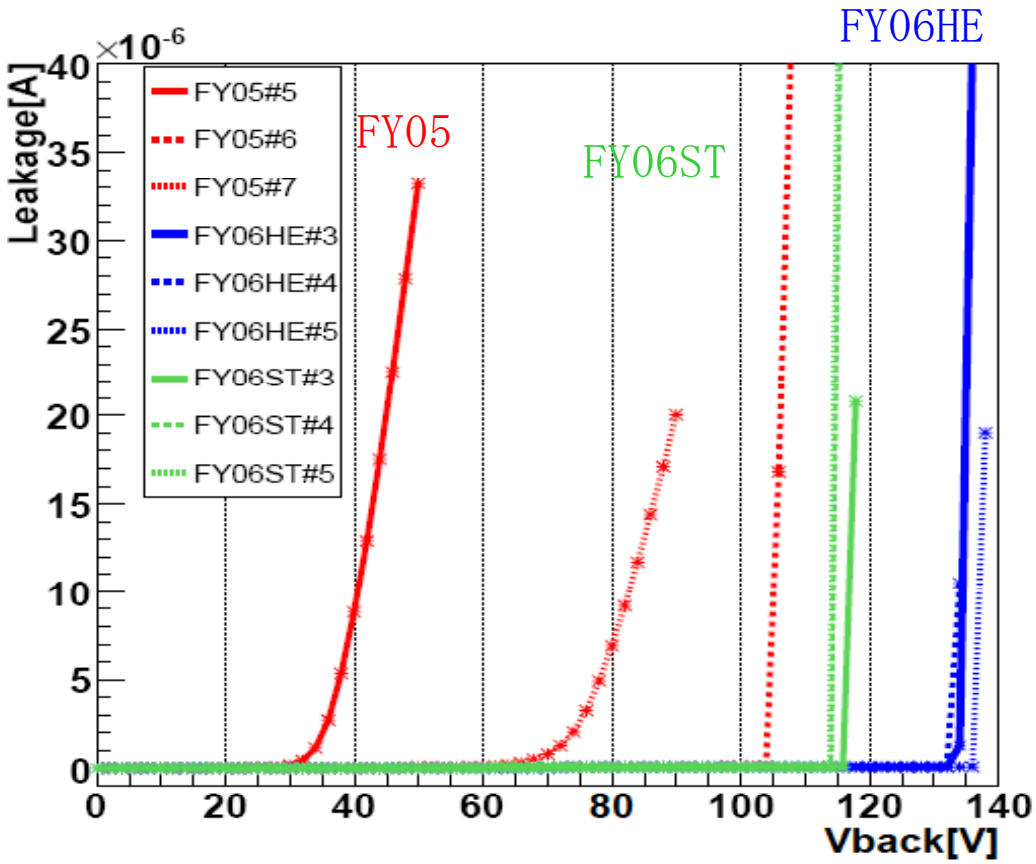
SOI Detector Issues

- Back gate effects
  - Sensor bias voltage
  - Si-SiO_2 Interface charge due to irradiation
  - Cross-talk charge injection
- Sensor bias voltage
  - Onset of microdischarge
  - Wafer thinning
- Unexpected surprise!

Microdischarge

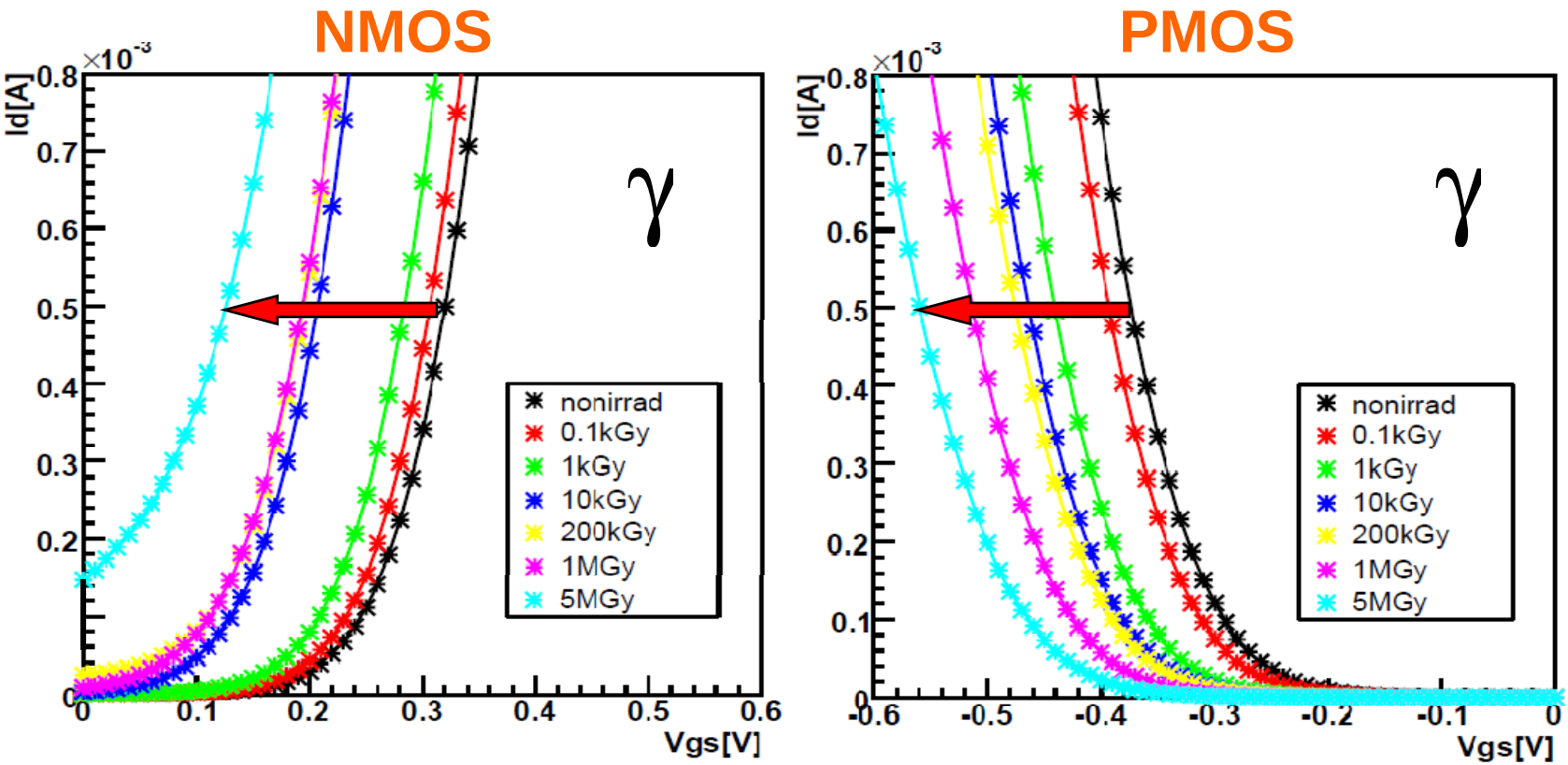
- TOPPIXN
  - Onset voltages improved
  - Rounding corners
  - Higher energy implantation





If ~700 Ωcm n-type, 140 μm at 100 V

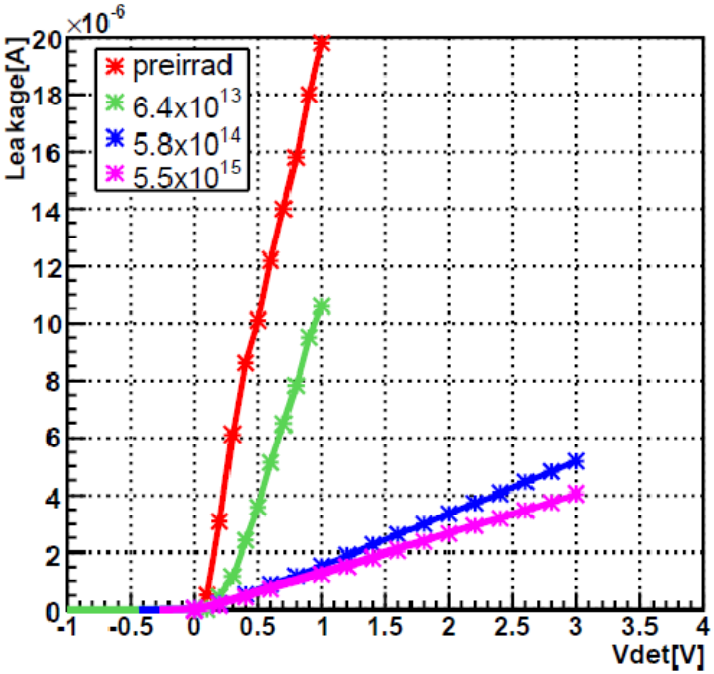
γ, Proton Irradiations

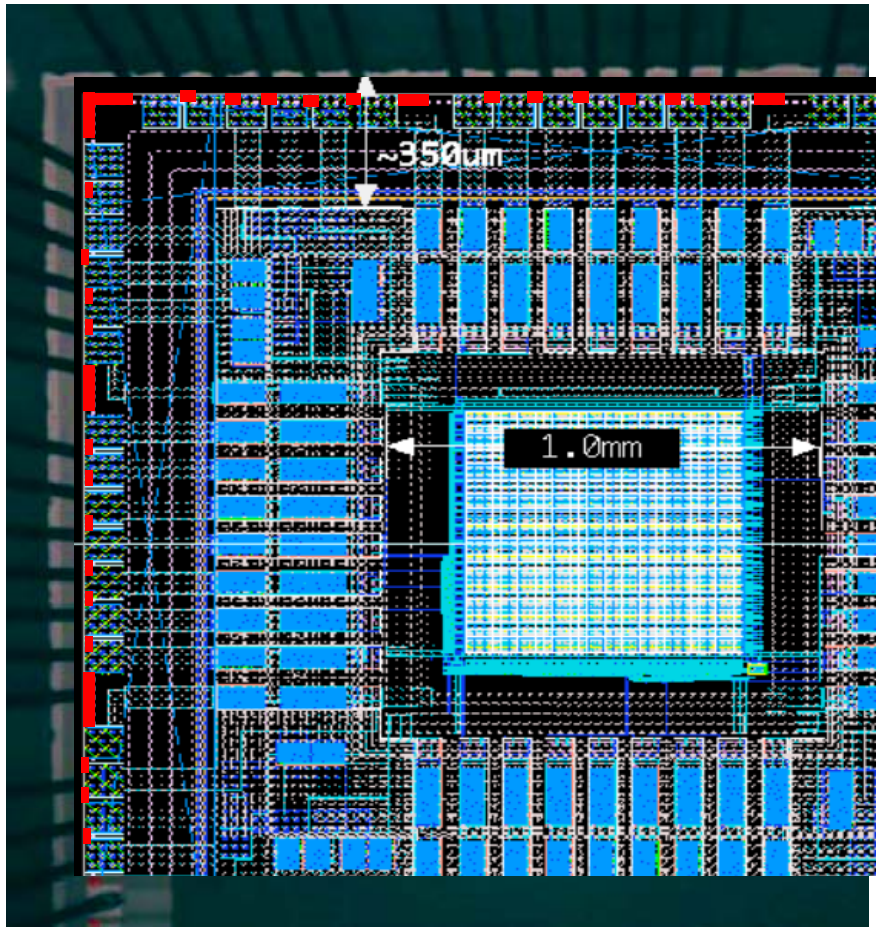


- Similar effect was confirmed with proton irradiations
- Si-SiO_2 interface charge works like a 2nd gate

Unexpected Surprise!!

- Proton irradiations at CYRIC
  - 6.4×10^{13} , 5.8×10^{14} ,5.5×10^{15} neq/cm^2
- Hot spot at "Bias" ring
- Diode characteristics





TOPPIXP: p-bulk assumption

Bulk (or Surface) is "n" even at 5.5×10^{15}

Summary

- We (SOIPIX collaboration) have started the R&D of making SOI monolithic pixel detector, in collaboration with an industry in the latest SOI technology, namely OKI electronics, in 2005

- With two MPW submissions, the basic has been demonstrated successfully

- It becomes the time to challenge the fundamental(?) issues in the SOI detector technology