Abstract

Timing systems for accelerators have operated in two domains: 1) *very* low jitter (~50 fs) phase stabilized reference lines over which information can not be transferred, and 2) higher jitter (~10 ns) timing and trigger lines over which fiducial signals can be sent. The ongoing developments in high speed serial data links and on-board processing should allow this gap to be bridged. We present a novel FPGA-based technique for the transmission of clocks and fiducial signals, over standard fiber optic data links, with a timing uncertainty on the order of 10 ps. Long term phase stability can be maintained with periodic calibrations while an on-board OCXO is used to reduce any high frequency jitter on the recovered clock.

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