ÖAW
Austrian Academy
of Sciences

Oregano Systems

Cern Timing Workshop 2008

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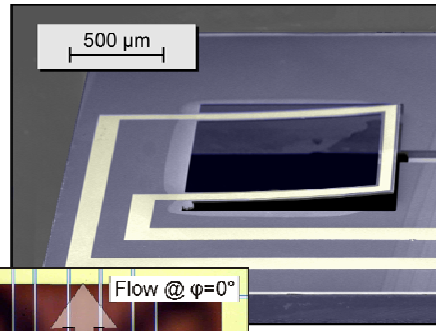
and Nikolaus Kerö

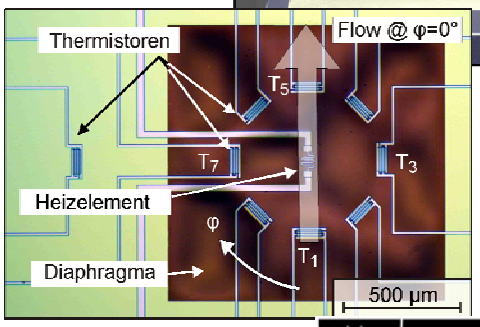
Research Unit for Integrated Sensor Systems
and Oregano Systems

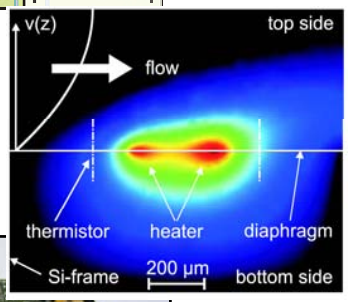
Research Unit for Integrated Sensor Systems

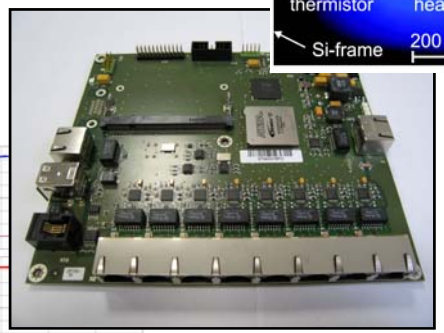
Research Unit for Integrated Sensor Systems

- Resonant and inertial sensors
  - Viscosity measurement
  - Magnetic field measurement
- Miniaturized thermal sensors
  - Flow measurement
  - Thermal conductivity measurement
- Capacitive sensors
- Architectures for smart sensor systems
  - Modular FPGA-based system-on-chip architectures
  - Signal processing for smart sensors
- Clock synchronization in sensor networks
  - Hard- and software support
- Security aspects
- Vertical integration
  - Software agents on RFIDs







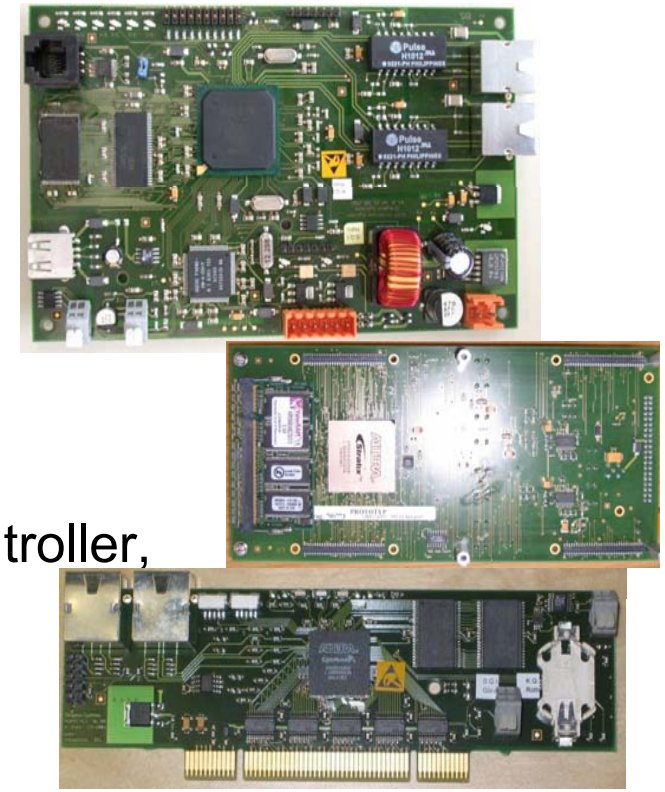


02/07/2008

Oregano Systems

Who is Oregano Systems ?

- Spin-Off from the Vienna University of Technology 2000/2001
- 12 Design Engineers
- Business Areas
  - Design Services
    - ASIC, FPGA, Embedded Systems
  - IP Cores
    - SYN1588®, 8051, VGA-Controller, ADPCM, AES, ...
  - Embedded Systems Design
    - System Specification
    - Module Design and Bring-up
    - Transfer to Series Production



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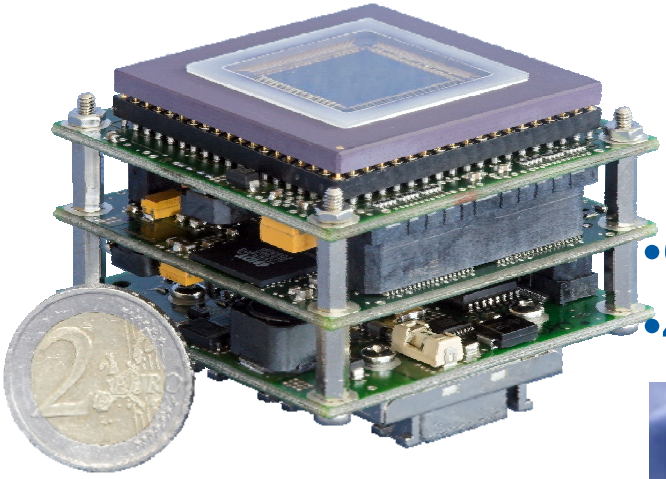
High-Speed Digital Image Processing

- CMOS Image Sensor
  - 1024 x 1280 at 500 fps
  - 1 x 1280 rd. 500.000 fps
  - 10 Pixel with 10 bit @ 66 MHz
- FPGA image pre-processing



- On-line quality assessment
- 40 Bank note sheets per second

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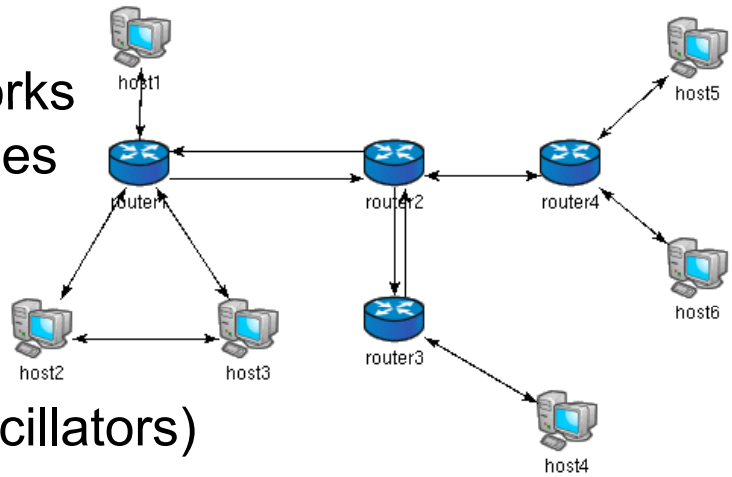
Network simulator

- Based on the Omnet++ platform
  - Discrete event simulation environment available under academic pubic license
  - Generic and flexible
  - Models for IP, TCP, UDP, and Ethernet available
- Advantages
  - Simulation of huge networks with non-uniform topologies possible
  - Monitoring the impact of system parameters (e.g. network load, aging of oscillators)
  - Evaluation of fault models
  - Usage of existing software is possible



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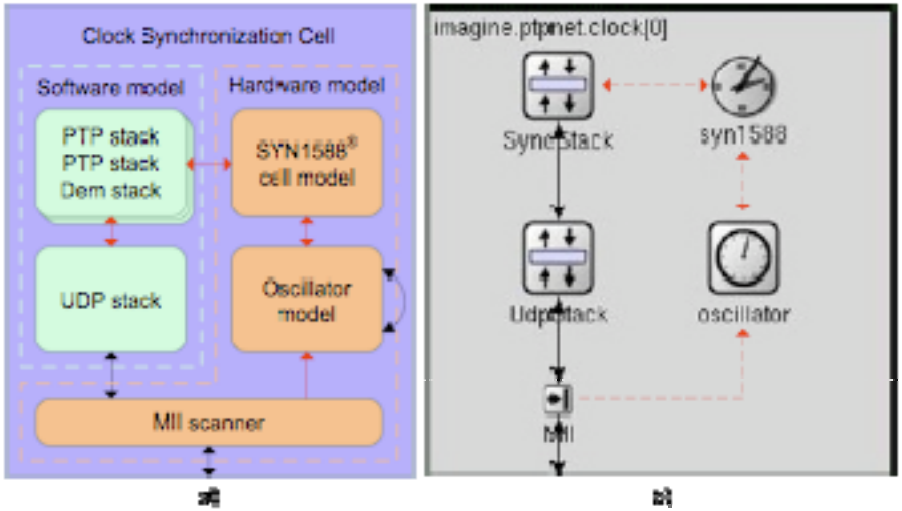
Network simulator

- Clock synchronization node
  - Oscillator: provides individual time base for each node
  - Clock Core: event based model of hardware functionality
  - MII timestamp unit: C++ representation of hardware
  - IEEE 1588 Stack: almost unmodified synchronization stack
  - UDP Stack: links OS calls to the simulator kernel



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SYN1588® Clock Synchronization

- IP Cores
  - SYN1588®Clock_S, M, L
  - Time stamp event FIFO
  - Digital and analog clock adjustment
  - User IOs (Event, Period, Trigger)
- PCI Ethernet NIC
- SYN1588® 8-port Switch
  - End-2-end & peer-2-peer
- IEEE1588 PTP Stack + Drivers
  - Version 2002 & 2008
  - Linux & Windows

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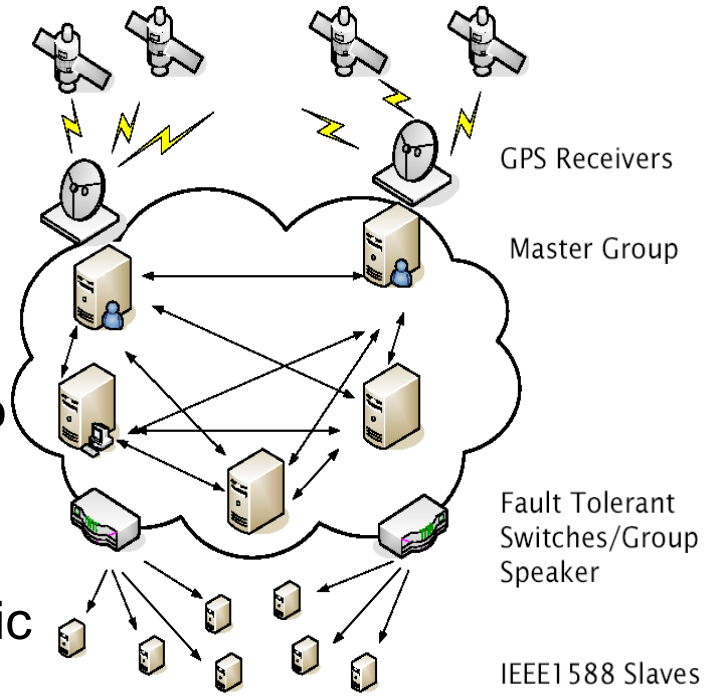
Fault tolerance for IEEE 1588 based networks

- Master Group
  - Democratic group of nodes
  - Fault tolerant
  - Some nodes with GPS
  - Backup nodes
- IEEE1588 Slaves
  - Synchronization according to standard
  - Less traffic between Master Group speaker and slaves (compared to pure democratic approaches)
- Better efficiency with m masters and n slaves (m<<n)



$$\eta_{\text{hybrid}} = \frac{(m-1)+n}{m \times (m-1)+n} = \frac{m+n-1}{m^2-m+n}.$$

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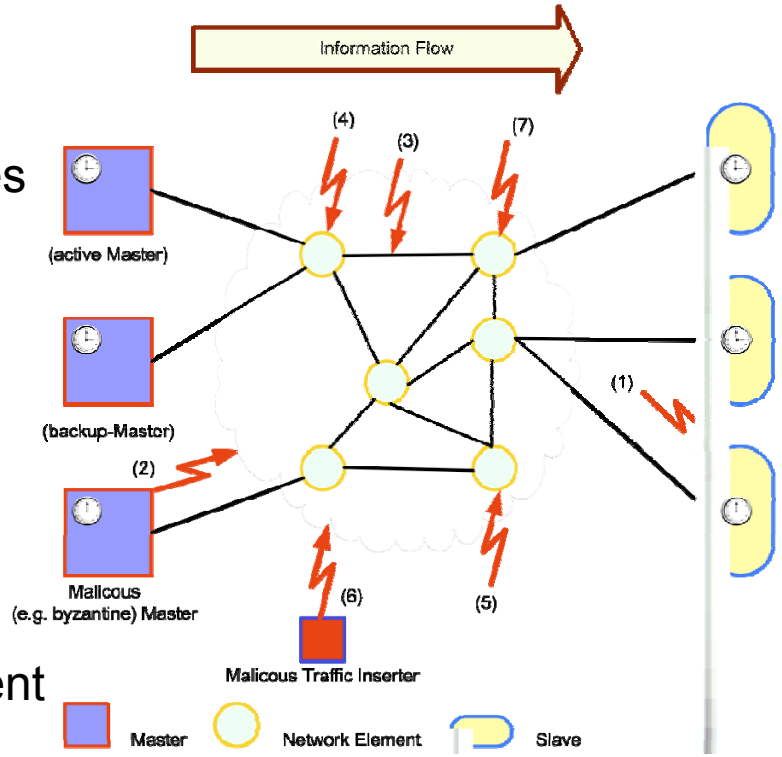
IEEE 1588 Security Implementation

- Approach:
  - Security analysis
  - Definition of parameters
    - Minimum sync cycles
    - Limited set of messages
  - Implementation
  - First published results
- Problems:
  - Security introduces jitter
  - Resource limited devices
  - Handling of intermediate nodes (Switches, transparent clocks, mixed secure and insecure)
  - Packet storm during secure system start up



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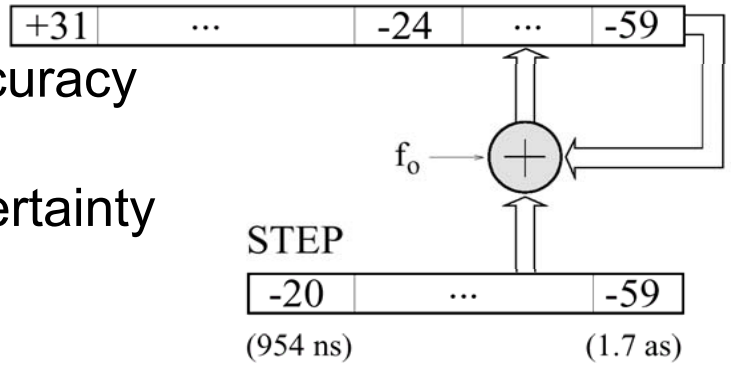
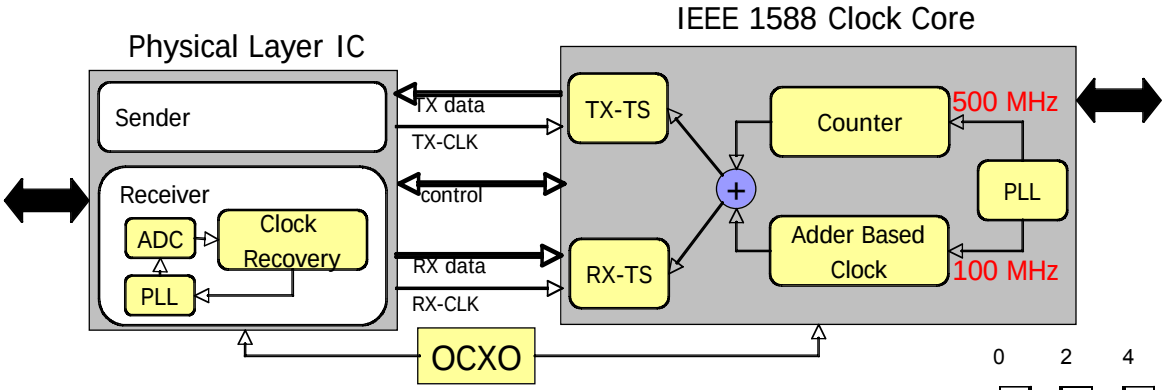
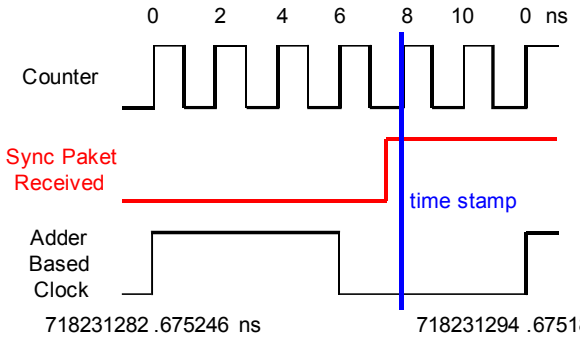
Synchronization Accuracy

- Accuracy depends on
  - Clock frequency, XO accuracy
  - Time stamp resolution
  - Transmission delay uncertainty
  - Sync-period
  - Algorithm







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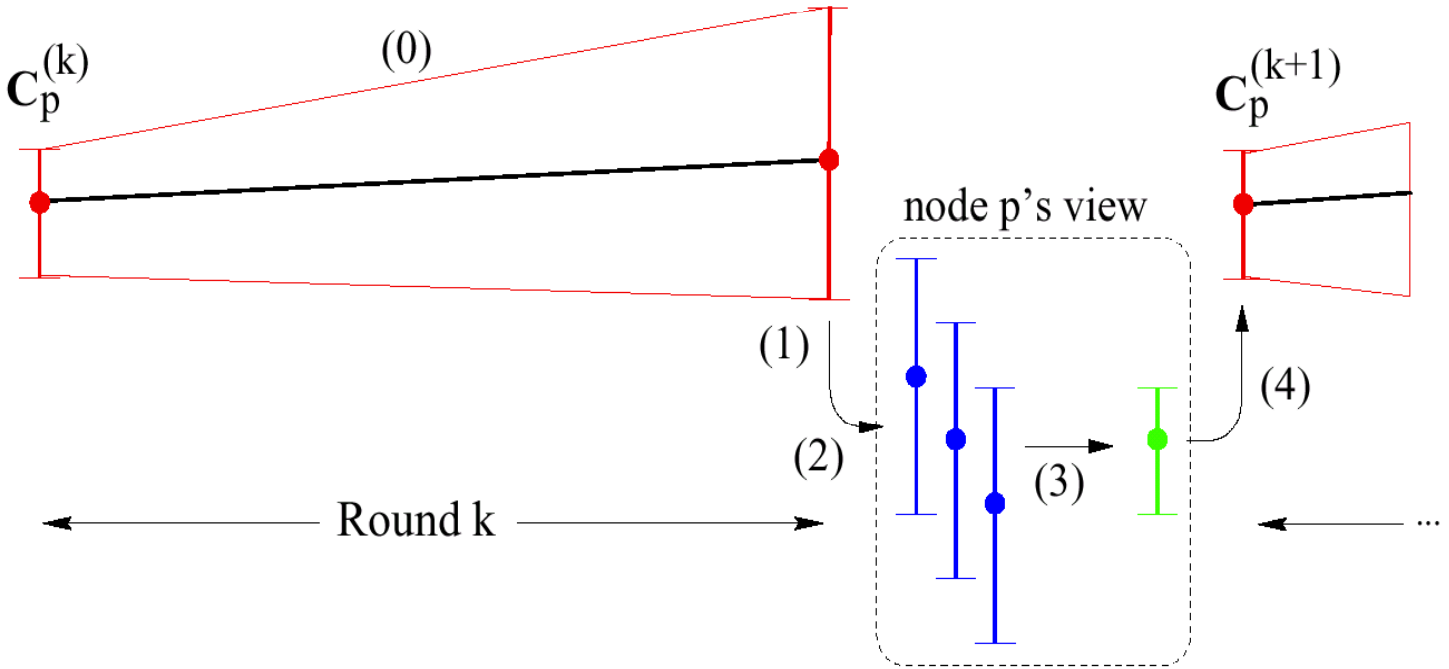
Interval Based Re-synchronization Mechanism

- Interval clocks instead of ordinary clocks
- Local clock values are adjusted
- Accuracy intervals are adjusted



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Laboratory experiments

- 100 Mbit/s, peer2peer, OCXO stabilized nodes, FPGA based added based clock, 1ns output resolution: σ≅900ps

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Thank You for Your Attention!

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Air Traffic Control Working Position

Oregano
Taste the difference

FREQUENTIS COMMUNICATION AND INFORMATION SOLUTIONS – FOR A SAFER WORLD!

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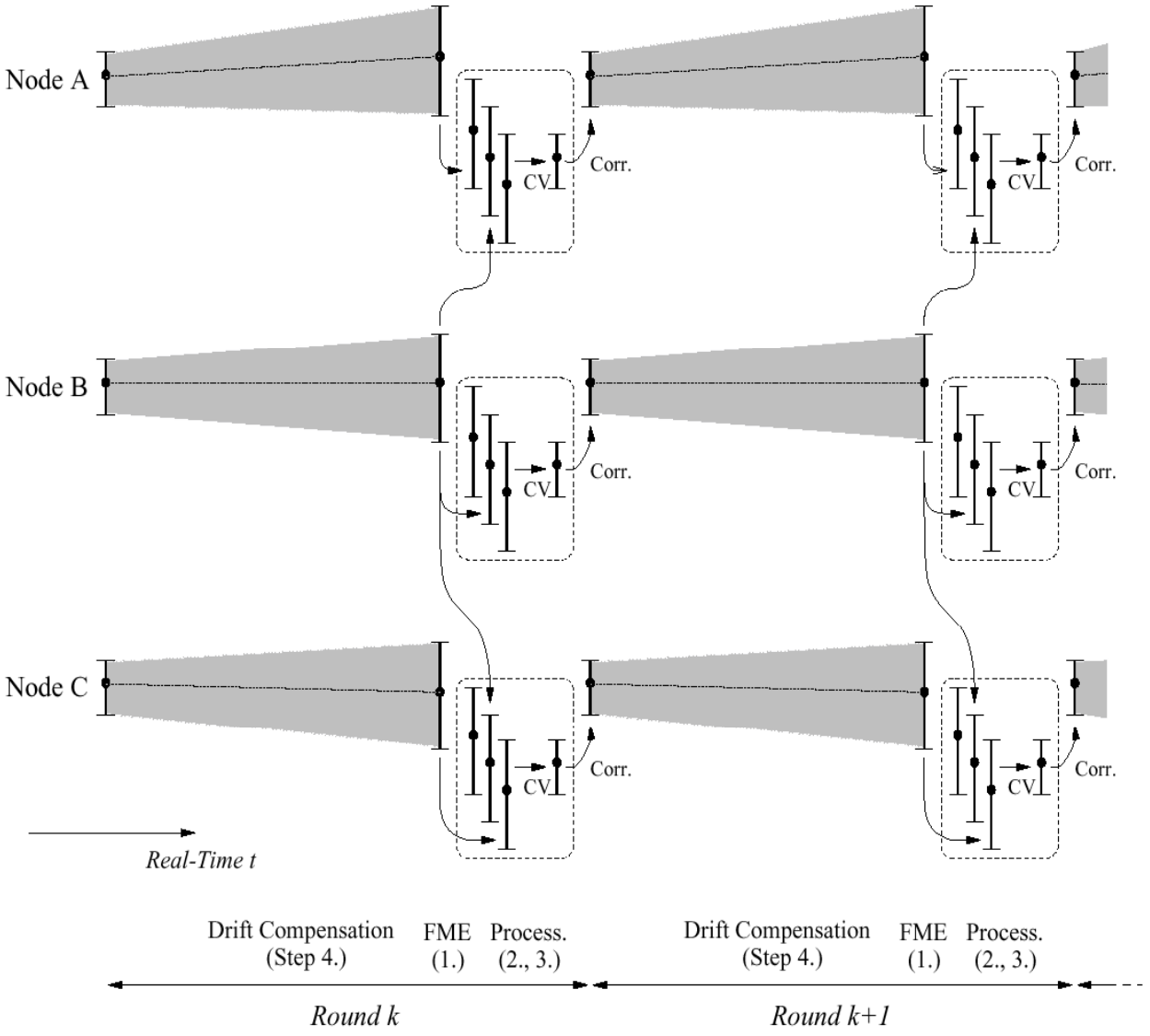
Interval Based Clock Sync.



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Syn1588® Adder Based Clock Structure